4

OPERATIONAL AMPLIFIER APPLICATIONS

4.1 INTRODUCTION

We have already discussed the electronics of op-amp, its dc and ac characteristics, parameter limitations and various configurations. Now we take a look at the applications of an op-amp. As we shall see, op-amp has countless applications and forms the basic building block of linear and non-linear analog systems. In linear circuits, the output signal varies with the input signal in a linear manner. Some of the linear applications discussed in this chapter are: adder, subtractor, voltage to current converter and current to voltage converter, instrumentation amplifier, analog computation, power amplifier etc.

There is another class of circuits with highly non-linear input to output characteristics. Rectifier, peak detector, clipper, clamper, sample and hold circuit, log and antilog amplifier, multiplier are the various non-linear circuits discussed. These non-linear circuits are very useful in industrial instrumentation, communication and general signal processing.

4.2 BASIC OP-AMP APPLICATIONS

Scale Changer/Inverter

In the basic inverting amplifier of Fig. 4.1, if the ratio $R_f/R_1 = K$, where K is a real constant, then the closed loop gain $A_{CL} = -K$. The circuit thus could be used to multiply by a constant factor if R_f and R_1 are selected as precision resistors. For $R_f = R_1$, $A_{CL} = -1$ and the circuit is called an inverter, i.e., the output is 180° out of phase with respect to input though the magnitudes are same.

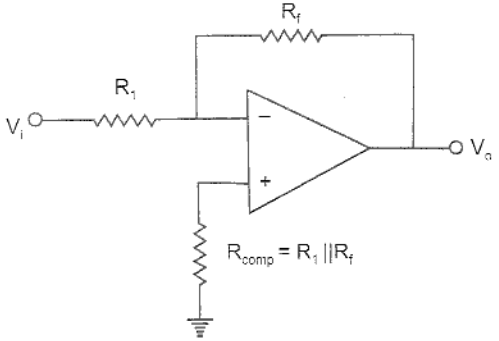


Fig. 4.1 Scale changer for ($R_f/R_1 = K$) and phase inverter for ($R_f/R_1 = 1$)

Summing Amplifier

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. An inverting summer or a non-inverting summer may be obtained as discussed now.

Inverting Summing Amplifier

A typical summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in Fig. 4.2 (a). The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$ and $R_i = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

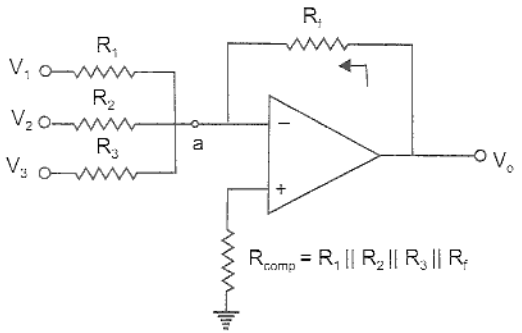


Fig. 4.2 (a) Inverting summing amplifier

The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0$$

or,
$$V_o = -\left(\frac{R_f}{R_1}V_1 + \frac{R_f}{R_2}V_2 + \frac{R_f}{R_3}V_3\right) \tag{4.1}$$

Thus the output is an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$, we have

$$V_o = -(V_1 + V_2 + V_3) \tag{4.2}$$

in which case the output V_o is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f$$

in which case

$$V_o = -\left(\frac{V_1 + V_2 + V_3}{3}\right) \tag{4.3}$$

Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current compensating resistor R_{comp} should be provided as discussed in Sec. 3.2.1. To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \,||\, R_2 \,||\, R_3$. Therefore, $R_{comp} = R_i \,||\, R_f = R_1 \,||\, R_2 \,||\, R_3 \,||\, R_f$.

Example 4.1

Design an adder circuit using an op-amp to get the output expression as

$$V_o = -(0.1\ V_1 + V_2 + 10\ V_3)$$

where V_1, V_2, and V_3 are the inputs.

Solution

The output in Fig. 4.2 (a) is

$$V_o = -[(R_f/R_1)V_1 + (R_f/R_2)V_2 + (R_f/R_3)V_3]$$

say $R_f = 10\ k\Omega,\ R_1 = 100\ k\Omega,\ R_2 = 10\ k\Omega,\ R_3 = 1\ k\Omega$

Then the desired output expression is obtained.

Non-inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier of Fig. 4.2 (b). Let the voltage at the (–) input terminal be V_a. The voltage at (+) input terminal will also be V_a. The nodal equation at node 'a' is given by

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

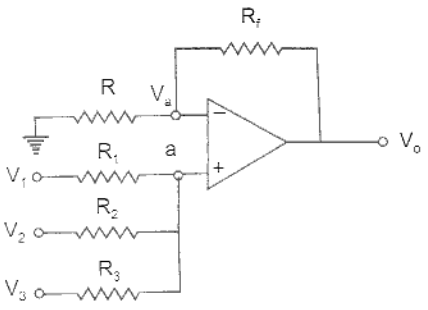


Fig. 4.2 (b) Non-inverting summing amplifier

from which we have,

$$V_a = \frac{\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3}}{\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_3}} \tag{4.4}$$

The op-amp and two resistors R_f and R constitute a non-inverting amplifier with

$$V_o = \left(1 + \frac{R_f}{R}\right) V_a \tag{4.5}$$

Therefore, the output voltage is,

$$V_o = \left(1 + \frac{R_f}{R}\right) \frac{\left(\dfrac{V_1}{R_1} + \dfrac{V_2}{R_2} + \dfrac{V_3}{R_3}\right)}{\dfrac{1}{R_1} + \dfrac{1}{R_2} + \dfrac{1}{R_3}} \tag{4.6}$$

which is a non-inverted weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1 + V_2 + V_3$

Subtractor

A basic differential amplifier can be used as a subtractor as shown in Fig. 4.3 (a). If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V_{o1} due to V_1 alone, make $V_2 = 0$. Then the circuit of Fig. 4.3 (a) becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

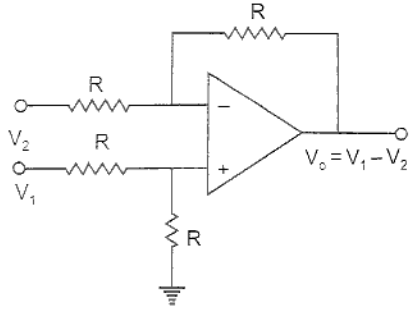


Fig. 4.3 (a) Op-amp as subtractor

$$V_{o1} = \frac{V_1}{2}\left(1 + \frac{R}{R}\right) = V_1 \tag{4.7}$$

Similarly the output V_{o2} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{o2} = -V_2 \tag{4.8}$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{o1} + V_{o2} = V_1 - V_2 \tag{4.9}$$

Adder-Subtractor

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in Fig. 4.3 (b).

The output voltage V_o can be obtained by using superposition theorem. To find output voltage V_{o1} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero. The simplified circuit is shown in Fig. 4.3 (c). This is the circuit of an inverting amplifier and its output voltage is,

$$V_{o1} = -\frac{R}{R/2}\frac{V_1}{2} = -V_1 \tag{4.10}$$

(by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage V_{o2} due to V_2 alone is,

$$V_{o2} = -V_2 \tag{4.11}$$

Now, the output voltage V_{o3} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero. The circuit now becomes a non-inverting amplifier as shown in Fig. 4.3 (d). The voltage V_a at the non-inverting terminal is

$$V_a = \frac{R/2}{R + R/2} V_3 = V_3/3 \tag{4.12}$$

So, the output voltage V_{o3} due to V_3 alone is

$$V_{o3} = \left(1 + \frac{R}{R/2}\right) V_a = 3\left(\frac{V_3}{3}\right) = V_3 \tag{4.13}$$

Similarly, it can be shown that the output voltage V_{o4} due to V_4 alone is

$$V_{o4} = V_4 \tag{4.14}$$

Thus, the output voltage V_o due to all four input voltages is given by

$$\begin{aligned} V_o &= V_{o1} + V_{o2} + V_{o3} + V_{o4} \\ &= -V_1 - V_2 + V_3 + V_4 \\ &= (V_3 + V_4) - (V_1 + V_2) \end{aligned} \tag{4.15}$$

So, the circuit is an adder-subtractor.

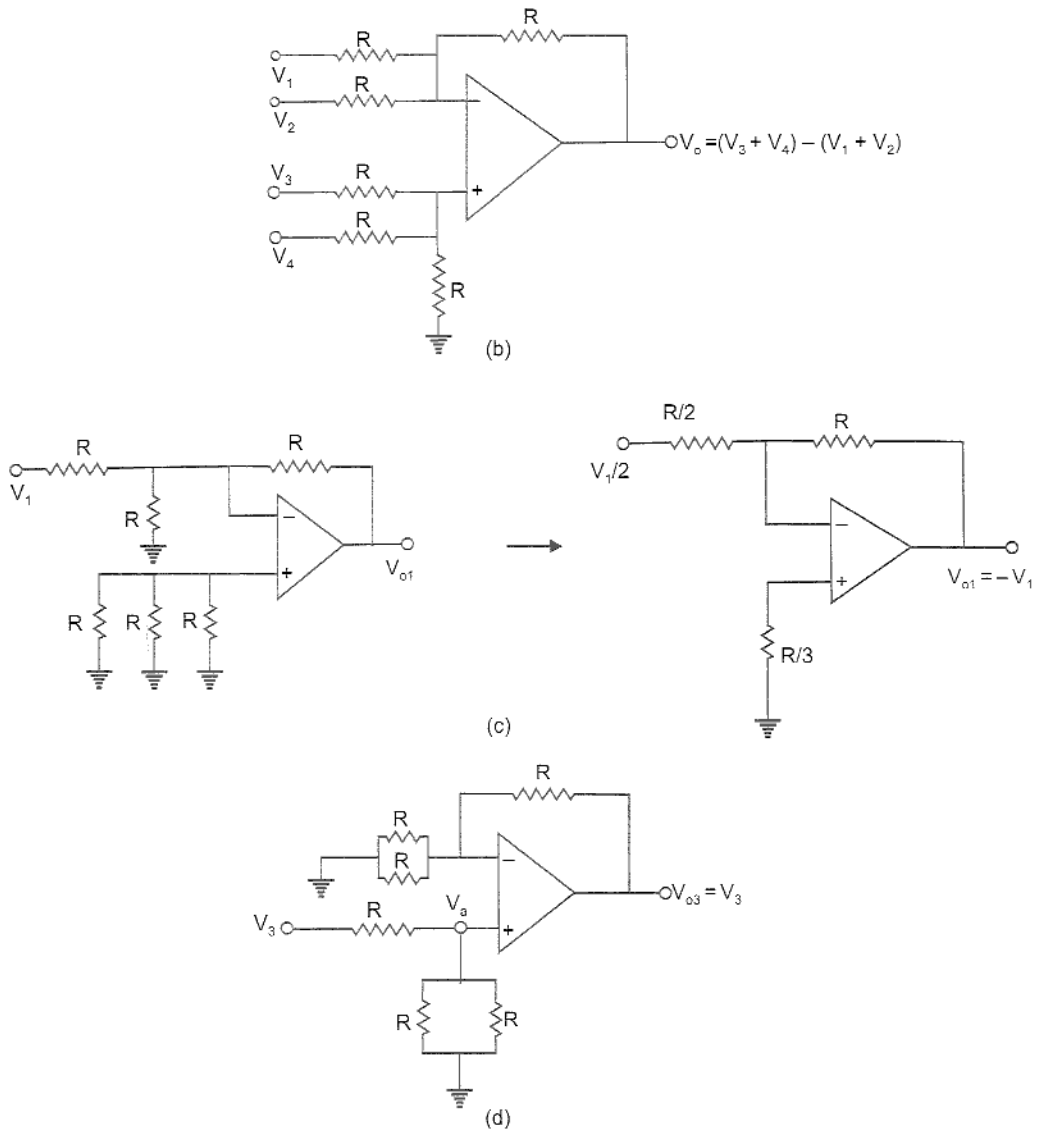


Fig. 4.3 (b) Op-amp adder-subtractor, (c) Simplifier circuit for $V_2 = V_3 = V_4 = 0$, (d) Simplified circuit for $V_1 = V_2 = V_4 = 0$

Example 4.2

Find V_o for the adder-subtractor shown in Fig. 4.4 (a).

Solution

The negative sum is obtained by setting $V_3 = V_4 = 0$. Thus,

$$V_o' = -\frac{50}{40} V_1 - \frac{50}{25} V_2$$

$$= -1.25V_1 - 2V_2$$

Now set $V_1 = V_2 = 0$ to find the output voltage due to V_3 and V_4. The voltage V_+ at the (+) input terminal due to V_3 and V_4 can be found by using superposition theorem as shown in Fig. 4.4 (b) as

$$V_+ = \frac{12}{10+12} V_3 + \frac{7.5}{20+7.5} V_4$$

or, $$V_+ = 0.545 V_3 + 0.273 V_4$$

The output voltage V_o'' due to V_3 and V_4 now can be determined from the equivalent circuit of Fig. 4.4 (c) as

$$V_o'' = \left(1 + \frac{R'}{R}\right) V_+$$

Here $$R' = 50 \text{ k}\Omega \text{ and } R = 40 \,||\, 25 = 15.38 \text{ k}\Omega$$

Therefore, $$V_o'' = \frac{50 + 15.38}{15.38} (0.545 V_3 + 0.273 V_4)$$

$$= 2.32 V_3 + 1.16 V_4$$

The total output voltage V_o is given by

$$V_o = V_o' + V_o'' = -1.25 V_1 - 2.0 V_2 + 2.32 V_3 + 1.16 V_4$$

Putting the value of V_1, V_2, V_3 and V_4, we get

$$V_o = -1.25 \times 2 - 2.0 \times 3 + 2.32 \times 4 + 1.16 \times 5$$

$$= -2.5 - 6.0 + 9.28 + 5.80 = 6.58 \text{ V}$$

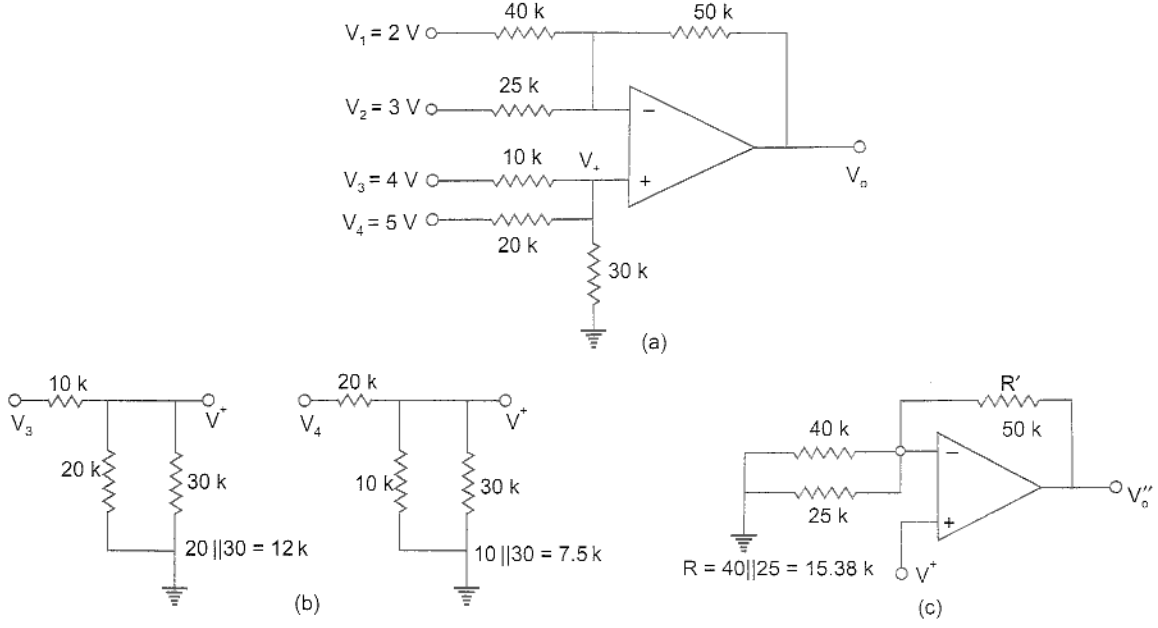


Fig. 4.4 (a) Circuit for Example 4.2 (b-c) Equivalent circuit

4.3 INSTRUMENTATION AMPLIFIER

In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. These physical quantities are usually measured with the help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are:

(i) high gain accuracy
(ii) high CMRR
(iii) high gain stability with low temperature coefficient
(iv) low dc offset
(v) low output impedance

There are specially designed op-amps such as μA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD620, AD624 by Analog Devices, LM-363.XX (XX→10,100,500) by National Semiconductor and INA101,104, 3626, 3629 by Burr-Brown.

Consider the basic differential amplifier as shown in Fig. 4.5 (a). It can be easily seen that the output voltage V_o is given by,

$$V_o = -\frac{R_2}{R_1}V_2 + \frac{1}{1+\frac{R_3}{R_4}}V_1\left(1+\frac{R_2}{R_1}\right) \qquad \left[V^+ = \frac{R_4}{R_3+R_4}V_1\right]$$

or,
$$V_o = -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}}\left(\frac{R_1}{R_2}+1\right)V_1\right] \tag{4.16}$$

For $R_1/R_2 = R_3/R_4$, we obtain

$$V_o = \frac{R_2}{R_1}(V_1 - V_2) \tag{4.17}$$

In the circuit of Fig. 4.5 (a), source V_1 sees an input impedance = $R_3 + R_4$ (= 101 kΩ) and the impedance seen by source V_2 is only R_1 (1 kΩ). This low impedance may load the signal source heavily. Therefore, high resistance buffer is used proceeding each input to avoid this loading effect as shown in Fig. 4.5 (b).

The op-amps A_1 and A_2 have differential input voltage as zero. For $V_1 = V_2$, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R' the non-inverting amplifier A_1 acts as voltage follower, so its output $V_2' = V_2$. Similarly op-amp A_2 acts as voltage follower having output $V_1' = V_1$. However, if $V_1 \neq V_2$, current flows in R and R', and $(V_2' - V_1') > (V_2 - V_1)$. Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of Fig. 4.5 (a). The output voltage V_o can be calculated as follows:

The voltage at the (+) input terminal of op-amp A_3 is $\frac{R_2 V_1'}{R_1+R_2}$. Using superposition theorem,

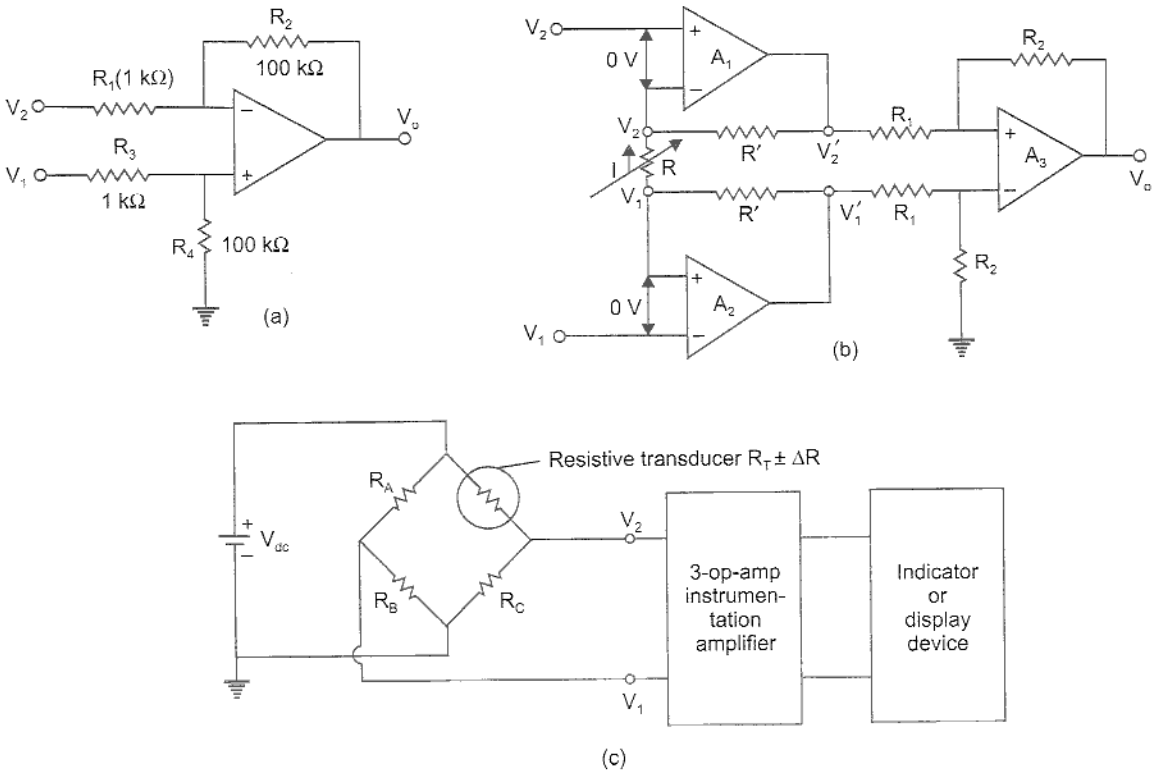


Fig. 4.5 (a) Differential amplifier using single op-amp, (b) An improved instrumentation amplifier, (c) Instrumentation amplifier using transducer bridge

we have,

$$V_o = -\frac{R_2}{R_1} V_2' + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1 + R_2}\right)$$

$$= \frac{R_2}{R_1}\left(V_1' - V_2'\right) \tag{4.18}$$

Since, no current flows into op-amp, the current I flowing (upwards) in R is $I = (V_1 - V_2)/R$ and passes through the resistor R'.

$$V_1' = R'I + V_1 = \frac{R'}{R}(V_1 - V_2) + V_1 \tag{4.19}$$

and

$$V_2' = -R'I + V_2 = -\frac{R'}{R}(V_1 - V_2) + V_2 \tag{4.20}$$

Putting the values of V_1' and V_2' in Eq. (4.18), we obtain,

$$V_o = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

or, $$V_o = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2) \quad (4.21)$$

In Eq. (4.21), if we choose $R_2 = R_1 = 25\ \text{k}\Omega$ (say) and $R' = 25\ \text{k}\Omega$; $R = 50\ \Omega$, then a gain of $\left(1 + 2 \times \frac{25\ \text{k}\Omega}{50\ \Omega}\right) = 1001$ can be achieved. The difference gain of this instrumentation amplifier can be varied by replacing the resistance R by a potentiometer in Fig. 4.5 (b). The resistance R, however should never be made zero, as this will make the gain infinity. To avoid such a situation, in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.

Figure 4.5 (c) shows a differential instrumentation amplifier using transducer bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured. The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1 = V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

There are a number of practical applications of instrumentation amplifier with the transducer bridge, such as temperature indicator, temperature controller, light intensity meter to name a few.

Instrumentation Amplifier IC - AD620

The pin configuration of a low cost instrumentation amplifier IC-AD620 is shown in Fig. 4.5 (d) (i). The AD620 requires only one external resistor, R_G to set gains from 1 to 1000. The relationship between gain and R_G as given by the manufacturer is

$$\text{Gain} = 1 + \left(\frac{49{,}400}{R_G}\right) \quad (4.22)$$

The value of R_G required for obtaining gain values of 1, 10, 100 and 1000 are shown in Fig. 4.5 (d) (ii).

As an application of IA, consider the circuit shown in Fig. 4.5 (d) (iii), where we have to measure V_{CE} of a CE amplifier. The usual method of measuring V_{CE} will be to first measure collector voltage, V_C (w.r.t. ground), then measure emitter voltage, V_E (w.r.t. ground) and then calculate the difference. If, however, terminals C and E are connected to the input terminals of AD620 and R_G is kept open, then the gain of IA is

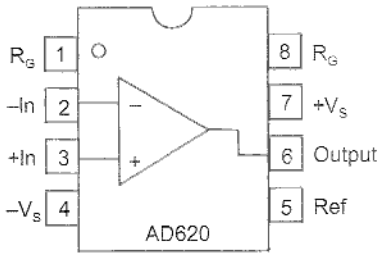
$$\text{Gain} = 1 + \frac{49{,}400}{\infty}$$

$$= 1.$$

The output voltage, V_o at pin 6 will now simply be,

$$V_o = 1(V_C - V_E)$$

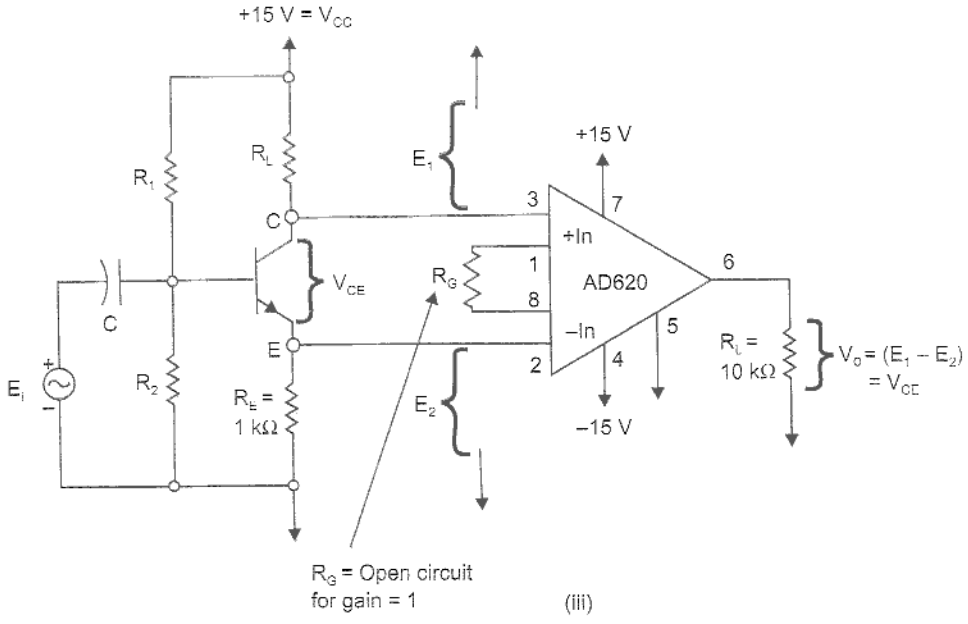
$$= V_{CE}$$



(i)

Gain	R_G
1	∞
10	5.489 kΩ
100	499 Ω
1000	49.5 Ω

(ii)



(iii)

Fig. 4.5 (d) (i) Pin configuration of AD620 (ii) Values of R_G for different gains (iii) Use of AD620 to measure a floating differential voltage

4.4 AC AMPLIFIER

The inverting and non-inverting op-amp amplifier configurations discussed earlier, respond to both ac and dc signals. However, if one wants to get the ac frequency response of an op-amp or if the ac input signal is superimposed with dc level, it becomes essential to block the dc component. This is achieved by using an AC amplifier with a coupling capacitor. AC amplifiers are of inverting and non-inverting type.

Inverting AC Amplifier

The circuit is shown in Fig. 4.6 (a). The capacitor C blocks the dc component of the input and together with the resistor R_1 sets the lower 3 dB frequency of the amplifier.

Since node 'a' is at virtual ground, the output voltage V_o (as a function of complex variables) is given by,

$$V_o = -IR_f = \frac{V_i}{R_1 + 1/sC} R_f \qquad (4.23)$$

Therefore,

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}\frac{s}{s + 1/R_1C} \tag{4.24}$$

It is seen from Eq. (4.24) that the lower 3dB frequency is,

$$f_L = \frac{1}{2\pi R_1 C} \tag{4.25}$$

In the mid-band range of frequencies, capacitor C behaves as a short circuit and therefore, Eq. (4.24) becomes,

$$A_{CL} \approx -\frac{R_f}{R_1} \tag{4.26}$$

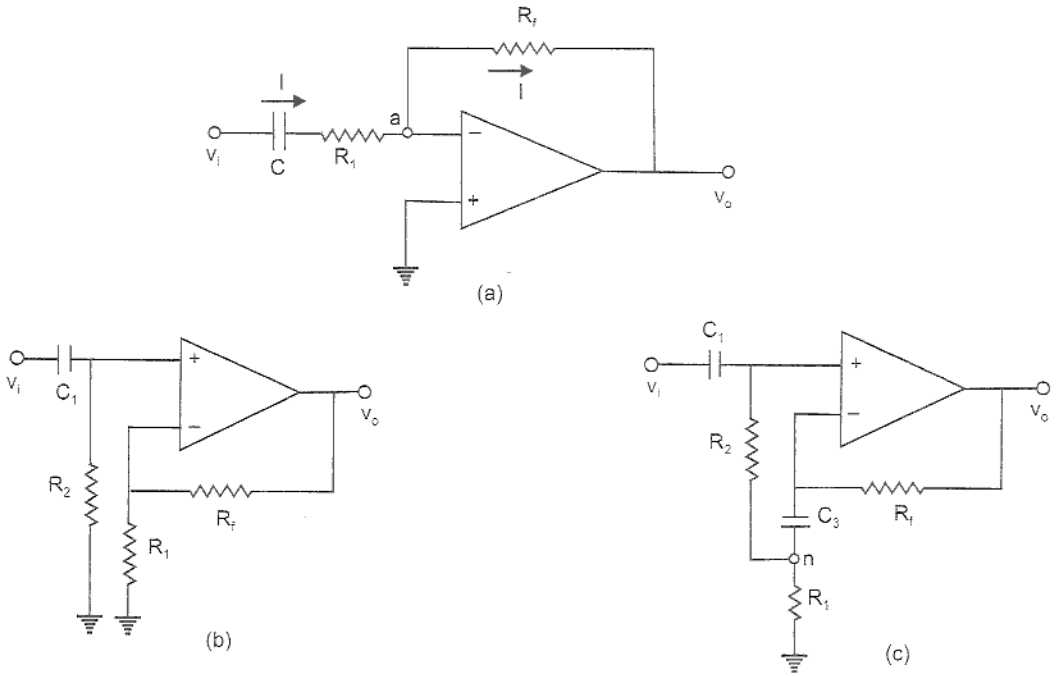


Fig. 4.6 (a) Inverting ac amplifier, (b) Non-inverting ac amplifier, (c) High input impedance non-inverting ac amplifier

Non-inverting AC Amplifier

The circuit is shown in Fig. 4.6 (b). Here a resistor R_2 is added to provide a dc return to ground. However, this reduces the overall input impedance of the amplifier, which now becomes approximately R_2. This problem of low input impedance is eliminated by connecting a capacitor C_3 as in Fig. 4.6 (c). Capacitor C_3 is large enough to act as short circuit to ac signals. The non-inverting terminal and the node 'n' will be almost at the same potential so that R_2 carries almost no current. Hence the circuit will have an extremely high input impedance.

AC Voltage Follower

The circuit of a practical ac voltage follower is shown in Fig. 4.7. The circuit is used as a buffer to connect a high impedance signal source to a low impedance load which may even be capacitive. The capacitor C_1 and C_2 are chosen high so that they are short circuit at all frequencies of operation. Resistors R_1 and R_2 provide a path for dc input current into the non-inverting terminal. C_2 acts as a bootstrapping capacitor and connects the resistance R_1 to the output terminal for ac operation. Hence the input resistance that the source sees is approximately $R_1/(1 - A_{CL})$ [from Miller's theorem], where A_{CL} is the gain of the voltage follower which is close to unity (0.9997). Thus very high input impedance can be obtained.

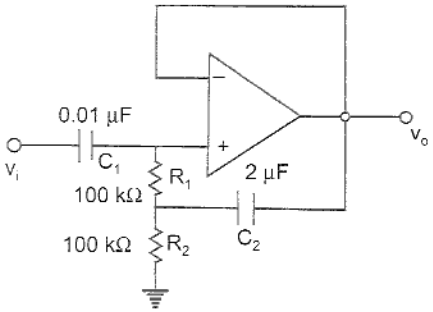


Fig. 4.7 AC voltage follower

4.5 V TO I AND I TO V CONVERTER

Voltage to Current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuits possible.

V-I Converter with floating load
V-I Converter with grounded load

Figure 4.8 (a) shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is v_i, therefore,

$$v_i = i_L R_1 \text{ (as } I_B = 0)$$

or,
$$i_L = \frac{v_i}{R_1} \tag{4.27}$$

That is the input voltage v_i is converted into an output current of v_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

A voltage-to-current converter with grounded load is shown in Fig. 4.8 (b). Let v_1 be the voltage at node 'a'. Writing KVL, we get

$$i_1 + i_2 = i_L \tag{4.28}$$

or,
$$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L$$

or,
$$v_i + v_o - 2v_1 = i_L R$$

Therefore,
$$v_1 = \frac{v_i + v_o - i_L R}{2} \tag{4.29}$$

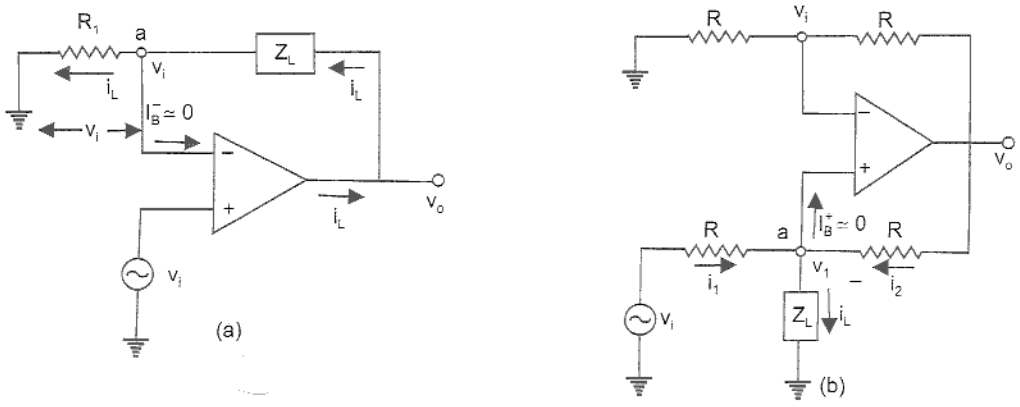


Fig. 4.8 Voltage to current converter with (a) Floating load, (b) Grounded load

Since the op-amp is used in non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The output voltage is,

$$v_o = 2\,v_1 = v_i + v_o - i_L R$$

that is,

$$v_i = i_L R$$

or,

$$i_L = \frac{v_i}{R} \tag{4.30}$$

As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

Current to Voltage Converter (Transresistance Amplifier)

Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo-device can be measured.

Figure 4.9 shows an op-amp used as I to V converter. Since the (–) input terminal is at virtual ground, no current flows through R_s and current i_s flows through the feedback resistor R_f. Thus the output voltage $v_o = -i_s R_f$. It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the op-amp. This means that μA741 (I_B = 3 nA) can be used to detect lower currents. The resistor R_f is sometimes shunted with a capacitor C_f to reduce high frequency noise and the possibility of oscillations.

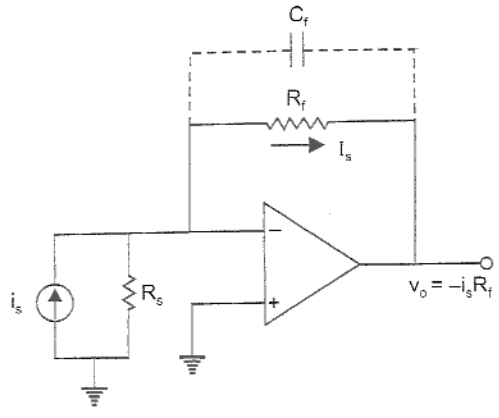


Fig. 4.9 Current to voltage converter

4.6 OP-AMP CIRCUITS USING DIODES

The major limitation of ordinary diode is that it cannot rectify voltages below V_γ (~0.6 V), the cut-in voltage of the diode. A circuit that acts like an ideal diode can be designed by placing a diode in the feedback loop of an op-amp as in Fig. 4.10 (a). Here the cut-in voltage is divided by the open loop gain A_{OL} (~10^4) of the op-amp so that V_γ is virtually eliminated. When the input $v_i > V_\gamma/A_{OL}$ then v_{oA}, the output of the op-amp exceeds V_γ and the diode D conducts. Thus the circuit acts like a voltage follower for input $v_i > V_\gamma/A_{OL}$ (i.e., $0.6/10^4 = 60$ μV) and the output v_o follows the input voltage v_i during the positive half cycle as shown in Fig. 4.10 (b). When v_i is negative or less than V_γ/A_{OL}, the diode D is ***off*** and no current is delivered to the load R_L except for small bias current of the op-amp and the reverse saturation current of the diode. This circuit is called the precision diode and is capable of rectifying input signals of the order of millivolt. Some typical applications of a precision diode discussed are:

Half-wave rectifier
Full-wave rectifier
Peak-value detector
Clipper
Clamper

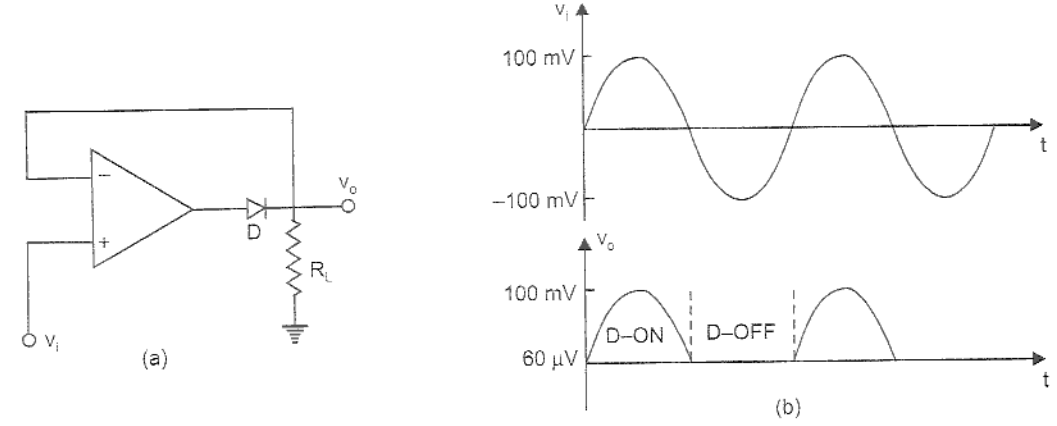


Fig. 4.10 (a) Precision diode, (b) Input and output waveforms

4.6.1 Half-Wave Rectifier

An inverting amplifier can be converted into an ideal half-wave rectifier by adding two diodes as shown in Fig. 4.11 (a). When v_i is positive, diode D_1 conducts causing v_{OA} to go to negative by one diode drop (~0.6 V). Hence diode D_2 is reverse biased. The output voltage v_o is zero, because, for all practical purposes, no current flows through R_f and the input current flows through D_1.

For negative input, i.e., $v_i < 0$, diode D_2 conducts and D_i is ***off***. The negative input v_i forces the op-amp output v_{OA} positive and causes D_2 to conduct. The circuit then acts like an inverter for $R_f = R_1$ and output v_o becomes positive.

The input, output waveforms are shown in Fig. 4.11 (b). The op-amp in the circuit of Fig. 4.11 (a) must be a high speed op-amp since it alternates between open loop and closed loop operations. The principal limitation of this circuit is the slew rate of the op-amp. As the input passes through zero, the op-amp output v_{oA} must change from 0.6 V to –0.6 V or vice-versa as quickly as possible in order to switch over the conduction from one diode to the other. The circuit of Fig. 4.11 (a) provides a positive ouput. However, if both the diodes are reversed, then only positive input signal is transmitted and gets inverted. The circuit, then provides a negative output.

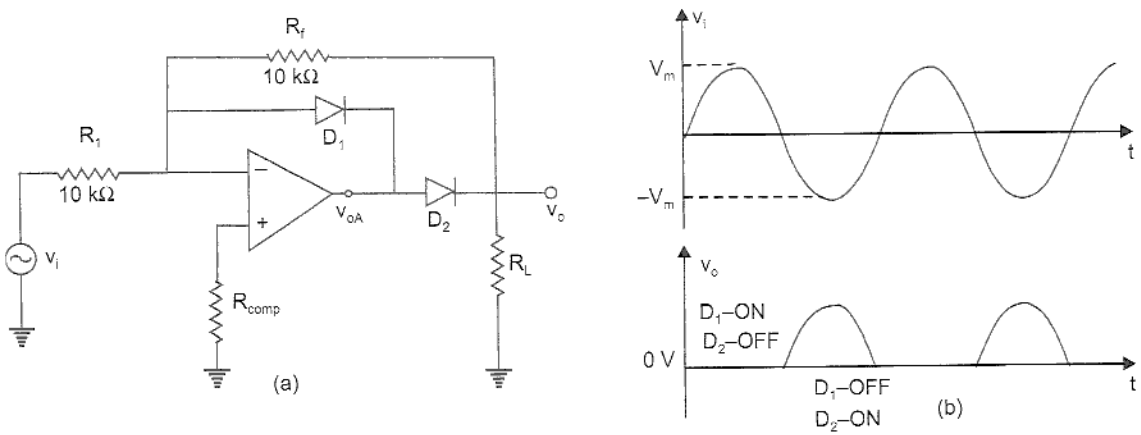


Fig. 4.11 (a) Ideal half-wave rectifier, (b) Input/output waveforms

4.6.2 Full-Wave Rectifier

A full-wave rectifier or absolute value circuit is shown in Fig. 4.12 (a). For positive input, i.e. $v_i > 0$, diode D_1 is ***on*** and D_2 is ***off***. Both the op-amps A_1 and A_2 act as inverter as shown in equivalent circuit in Fig. 4.12 (b). It can be seen that $v_o = v_i$.

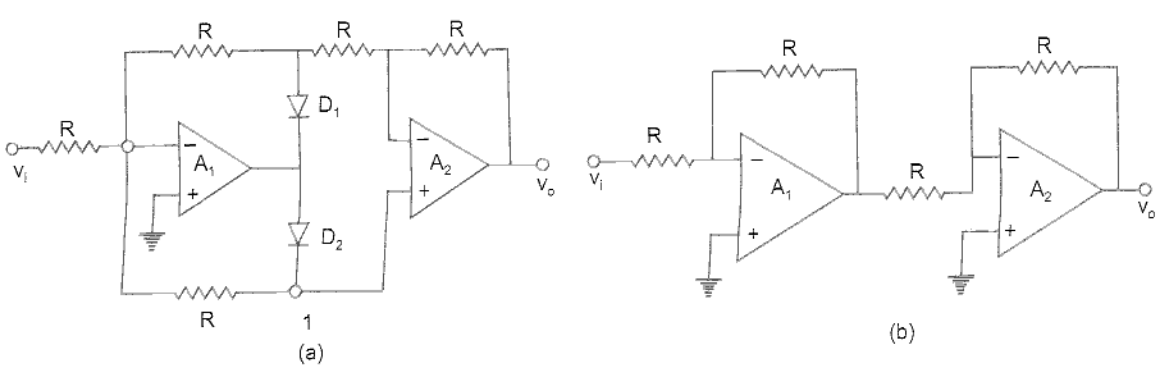


Fig. 4.12 (a) Precision full wave rectifier, (b) Equivalent circuit for $v_i > 0$; D_1 is on and D_2 is OFF; op-amp A_1 and A_2 operate as inverting amplifier

For negative input, i.e. $v_i < 0$, diode D_1 is ***off*** and D_2 is ***on***. The equivalent circuit is shown in Fig. 4.12 (c). Let the output voltage of op-amp A_1 be v. Since the differential input to A_2 is zero, the inverting input terminal is also at voltage v.

KCL at node 'a' gives

$$\frac{v_i}{R} + \frac{v}{2R} + \frac{v}{R} = 0$$

or

$$v = -\frac{2}{3} v_i \tag{4.31}$$

The equivalent circuit of Fig. 4.12 (c) is a non-inverting amplifier as shown in Fig. 4.12 (d). The output v_o is,

$$v_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3} v_i\right) = v_i \tag{4.32}$$

Hence for $v_i < 0$, the output is positive. The input and output waveforms are shown in Fig. 4.12 (e). The circuit is also called an absolute value circuit as output is positive even when input is negative. For example, the absolute value of $|+2|$ and $|-2|$ is $+2$ only. It is possible to obtain negative outputs for either polarity of input simply by reversing the diodes.

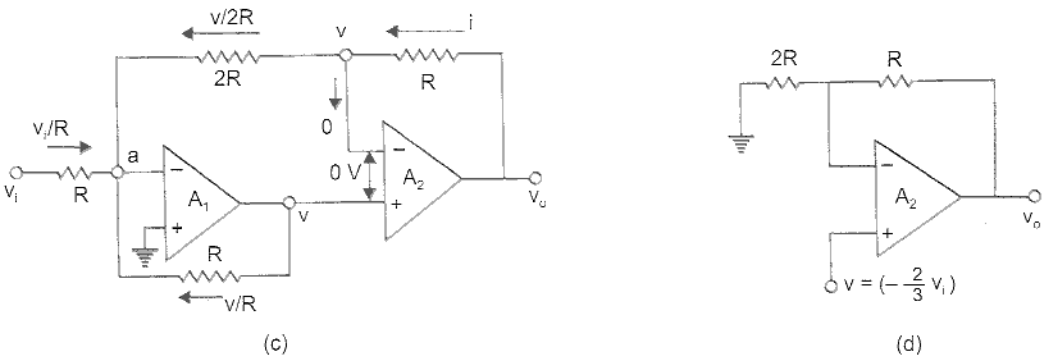


Fig. 4.12 (c) Equivalent circuit for $v_i < 0$, (d) Equivalent circuit of (c)

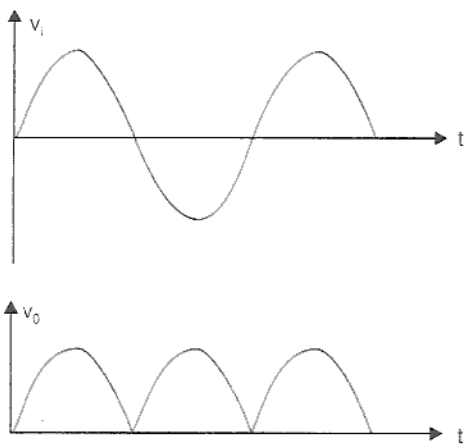


Fig. 4.12 (e) Input and output waveforms

4.6.3 Peak Detector

The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value (almost indefinitely) on a capacitor. If a higher peak signal value comes along, this new value is stored. The highest peak value is stored until the capacitor is discharged.

Consider the circuit of Fig. 4.13 (a). When input v_i exceeds v_c, the voltage across the capacitor, the diode D is forward biased and the circuit becomes a voltage follower. Consequently, the output voltage v_o follows v_i as long as v_i exceeds v_c. When v_i drops below v_c, the diode becomes reverse-biased and the capacitor holds the charge till input voltage again attains a value greater than v_c. Figure 4.13 (b) shows the voltage waveshape for the positive peak detector. It may be noted that the peak at time t' is missed, the reason is obvious. The circuit can be reset, that is, capacitor voltage can be made zero by connecting a low leakage MOSFET switch across the capacitor. The circuit can be modified to hold the lowest or most negative voltage of a signal by reversing the diode. Peak detectors find application in test and measurement instrumentation as well as in amplitude modulation (AM) communication.

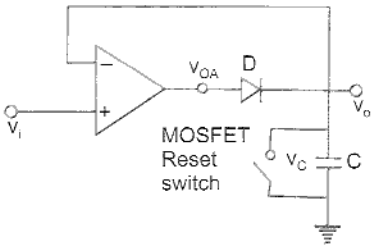


Fig. 4.13 (a) Positive peak detector

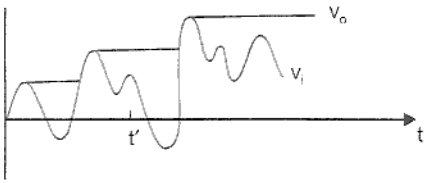


Fig. 4.13 (b) Output v_o corresponding to arbitrary input v_i

4.6.4 Clipper

A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired output waveform.

Figure 4.14 (a) shows a positive clipper. The clipping level is determined by the reference voltage V_{ref} and could be obtained from the positive supply voltage V^+. The input and output waveforms are shown in Fig. 4.14 (b). It can be seen that the portion of the output voltage for $v_o > V_{ref}$ are clipped off.

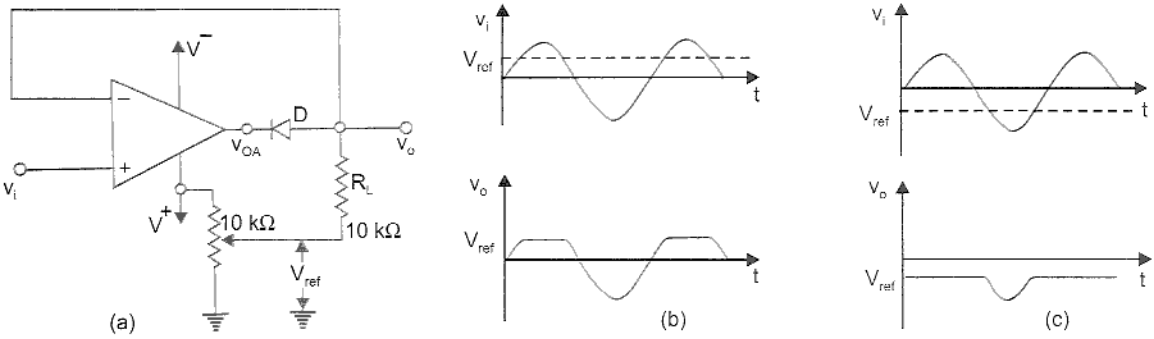


Fig. 4.14 (a) Positive clipper circuit; Input and output waveforms for (b) Positive V_{ref} (c) Negative

For input voltage $v_i < V_{ref}$, diode D conducts. The op-amp works as a voltage follower and output v_o follows input v_i till $v_i \leq V_{ref}$. When v_i is greater than V_{ref}, the output v_{oA} of the op-amp is large enough of drive D into cut-off. The op-amp operates in the open-loop and output voltage $v_o = V_{ref}$. However, if V_{ref} is made negative, then the entire output waveform above V_{ref} will get clipped off as shown in Fig. 4.14 (c).

The positive clipper of Fig. 4.14 (a) can be easily converted into a negative clipper by simply reversing diode D and changing the polarity of the reference voltage V_{ref} as shown in Fig. 4.15 (a). The negative clipper clips off the negative parts of the input signal below the reference voltage. The circuit diagram of a negative clipper and the expected waveforms for negative V_{ref} and positive V_{ref} are shown in Fig. 4.15 (b and c).

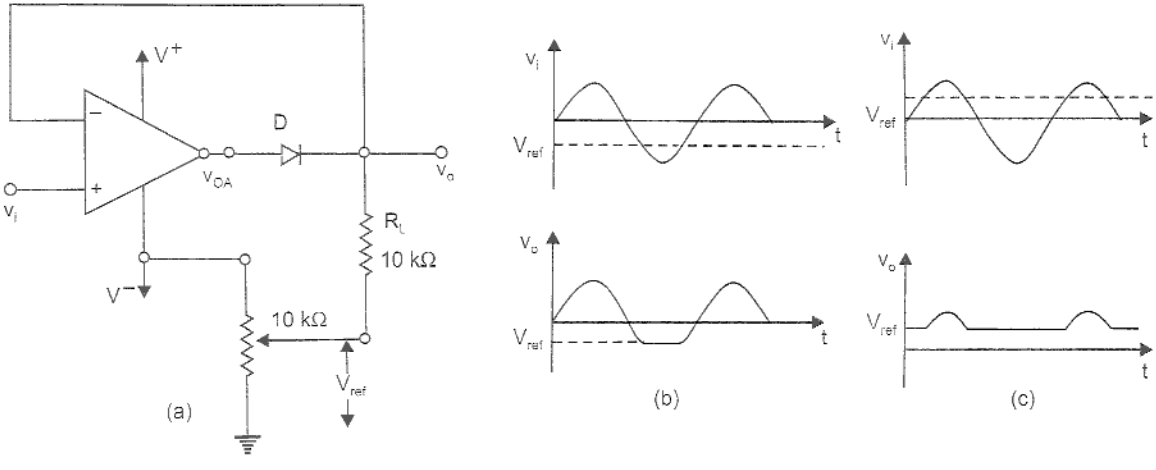


Fig. 4.15 (a) Negative clipper circuit (b, c) Input-output waveforms for negative and positive V_{ref}

4.6.5 Clamper

The clamper is also known as dc inserter or restorer. The circuit is used to add a desired dc level to the output voltage. In other words, the output is clamped to a desired dc level. If the clamped dc level is positive, it is called positive clamper. Similarly if the clamped dc level is negative, the clamper is called negative clamper.

Figure 4.16 (a) shows a clamper with a variable positive dc voltage applied at the (+) input terminal. This circuit clamps the peaks of the input waveform and therefore is also called a peak clamper. The output voltage in the circuit is the net result of ac and dc input voltages applied to the (–) and (+) input terminals respectively. Let us first see the effect of V_{ref} applied at the (+) input terminal. For positive V_{ref}, the voltage v' is also positive, so that the diode D is forward biased. The circuit operates as a voltage follower and therefore output voltage $v_o = + V_{ref}$.

Now consider the ac input signal $v_i = V_m \sin \omega t$ applied at the (–) input terminal. During the negative half cycle of v_i, diode D conducts. The capacitor C_1 charges through diode D to the negative peak voltage V_m. However, during the positive half cycle of v_i, diode D is reverse

biased. The capacitor retains its previous voltage V_m. Since this voltage V_m is in series with the ac input signal, the output voltage now will be $v_i + V_m$. The total output voltage is, therefore, $V_{ref} + v_i + V_m$. The input and output waveforms are shown in Fig. 4.16 (b). It is possible to obtain negative peak clamping by reversing the diode D and using a negative reference voltage $-V_{ref}$. The expected waveforms are shown in Fig. 4.16 (c). The resistor R is used for protecting the op-amp against excessive discharge currents from capacitor C_1 especially when the dc supply voltages are switched off.

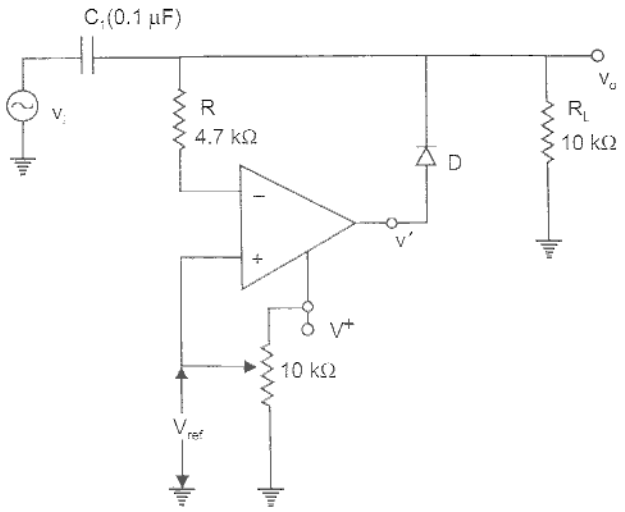


Fig. 4.16 (a) Peak clamper circuit

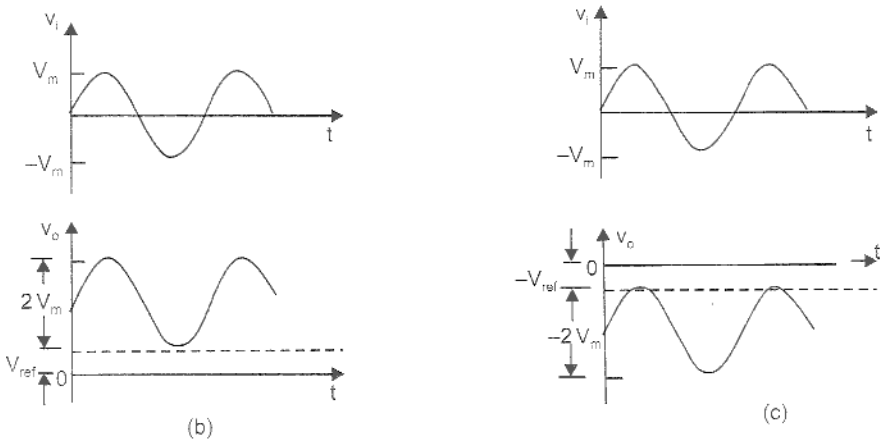


Fig. 4.16 (b) Waveforms for $+V_{ref}$, (c) Waveforms for $-V_{ref}$

4.7 SAMPLE AND HOLD CIRCUIT

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in Fig. 4.17 (a). The n-channel E-MOSFET works as a switch and is controlled by the control voltage v_c and the capacitor C stores the charge. The analog signal v_i to be sampled is applied to the drain of E-MOSFET and the control voltage v_c is applied to its gate. When v_c is positive, the E-MOSFET turns ***on*** and the capacitor C charges to the instantaneous value of input v_i with a time constant $[(R_o + r_{DS}$

(*on*)] C. Here R_o is the output resistance of the voltage follower A_1 and r_{DS} (*on*) is the resistance of the MOSFET when *on*. Thus the input voltage v_i appears across the capacitor C and then at the output through the voltage follower A_2. The waveforms are as shown in Fig. 4.17 (b).

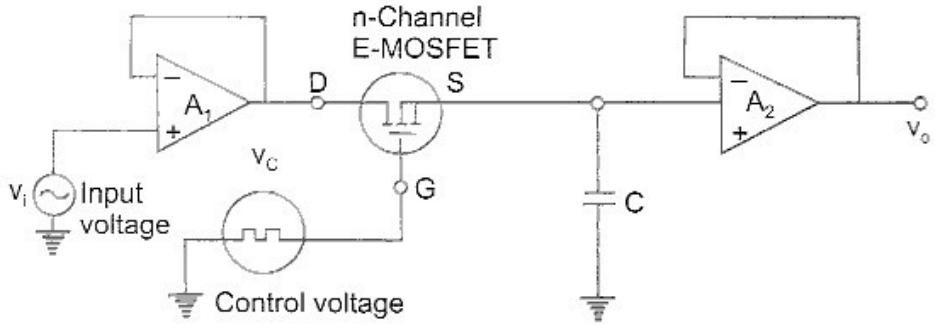
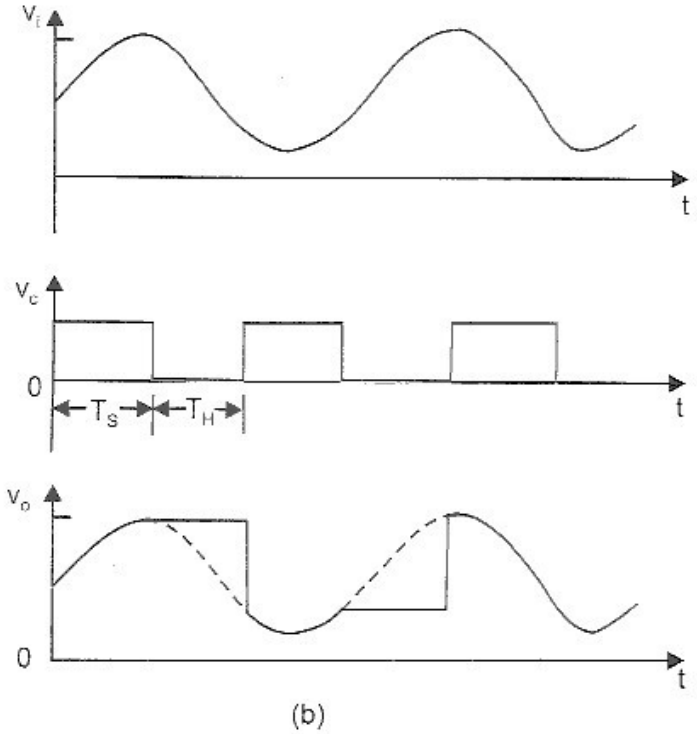


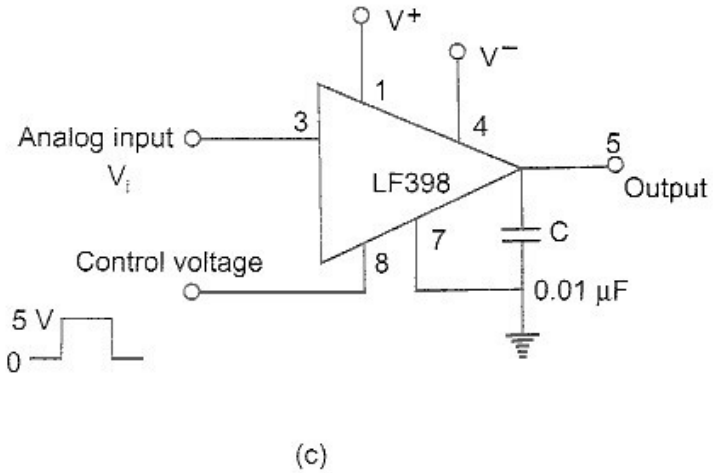
Fig. 4.17 (a) Sample and hold circuit

During the time when control voltage v_c is zero, the E-MOSFET is *off*. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it. The time period T_S, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period T_H of v_c during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge.

Specially designed sample and hold ICs of make Harris semiconductor HA2420, National semiconductor such as LF198, LF398 are also available. A typical connection diagram of the LF398 is shown in Fig. 4.17 (c). It may be noted that the storage capacitor C is connected externally.



(b)



(c)

Fig. 4.17 (b) Input and output waveforms, (c) Typical connection diagram

4.8 LOG AND ANTILOG AMPLIFIER

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or sinh x. These can be performed continuously with log-amps. One would like to have direct dB display on digital voltmeter and spectrum analyser. Log-amp can easily perform this function. Log-amp can also be used to compress the dynamic range of a signal.

Log Amplifier

The fundamental log-amp circuit is shown in Fig. 4.18 (a) where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s (e^{qV_E/kT} - 1) \qquad (4.33)$$

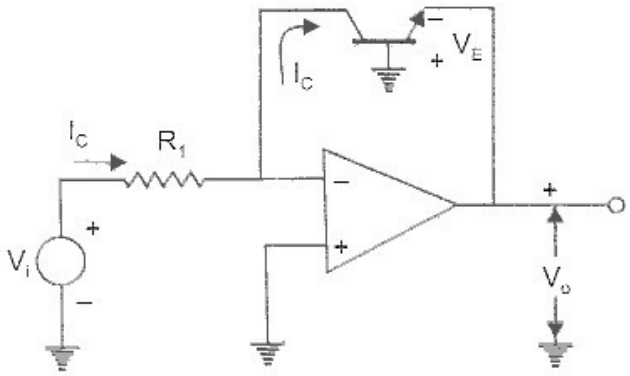


Fig. 4.18 (a) Fundamental log-amp circuit

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_s (e^{qV_E/kT} - 1) \qquad (4.34)$$

where I_s = emitter saturation current $\approx 10^{-13}$ A
k = Boltzmann's Constant
T = absolute temperature (in K)

Therefore, $$\frac{I_C}{I_s} = (e^{qV_E/kT} - 1) \qquad (4.35)$$

or, $$e^{qV_E/kT} = \frac{I_C}{I_s} + 1$$

$$\approx \frac{I_C}{I_s} \qquad [\text{as } I_s \approx 10^{-13} \text{ A}, I_C >> I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right) \qquad (4.36)$$

Also in Fig. 4.18 (a),

$$I_C = \frac{V_i}{R_1}$$

$$V_E = -V_o$$

so, $$V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \qquad (4.37)$$

where $V_{ref} = R_1 I_s$

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find $\log_{10}$ by proper scaling

$$\log_{10} X = 0.4343 \ln X \tag{4.38}$$

The circuit, however, has one problem. The emitter saturation current I_s varies from transistor to transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig. 4.18 (b). The input is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

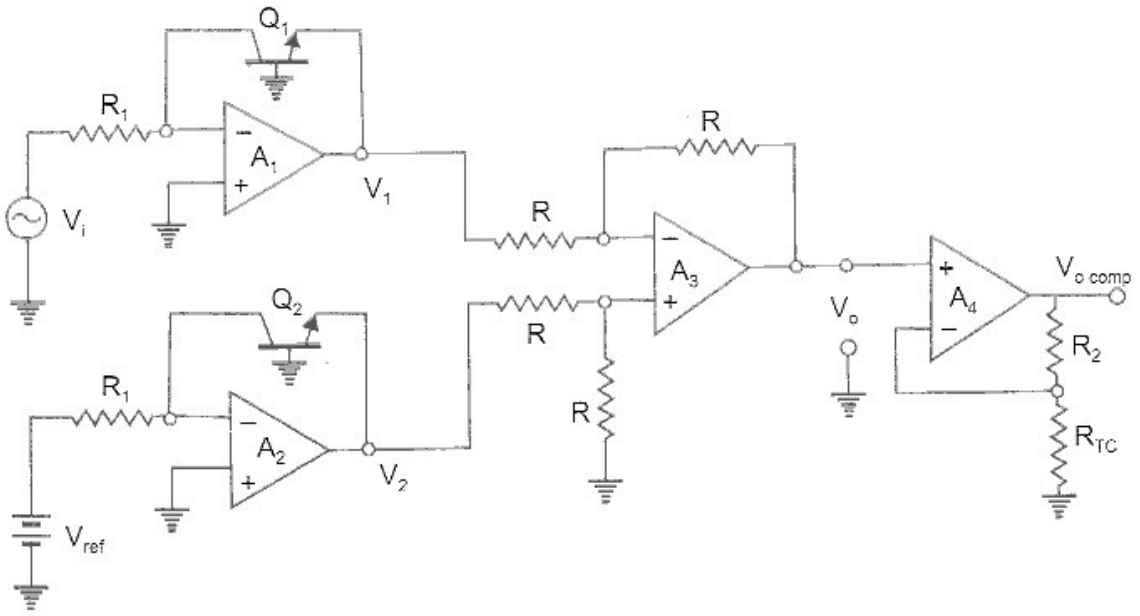


Fig. 4.18 (b) Log-amp with saturation current and temperature compensation

Assume, $$I_{s1} = I_{s2} = I_s \tag{4.39}$$

and then, $$V_1 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) \tag{4.40}$$

and $$V_2 = -\frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.41}$$

Now, $$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right] \tag{4.42}$$

or, $$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.43}$$

Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q}\ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.44}$$

where R_{TC} is a temperature-sensitive resistance with a positive coefficient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.

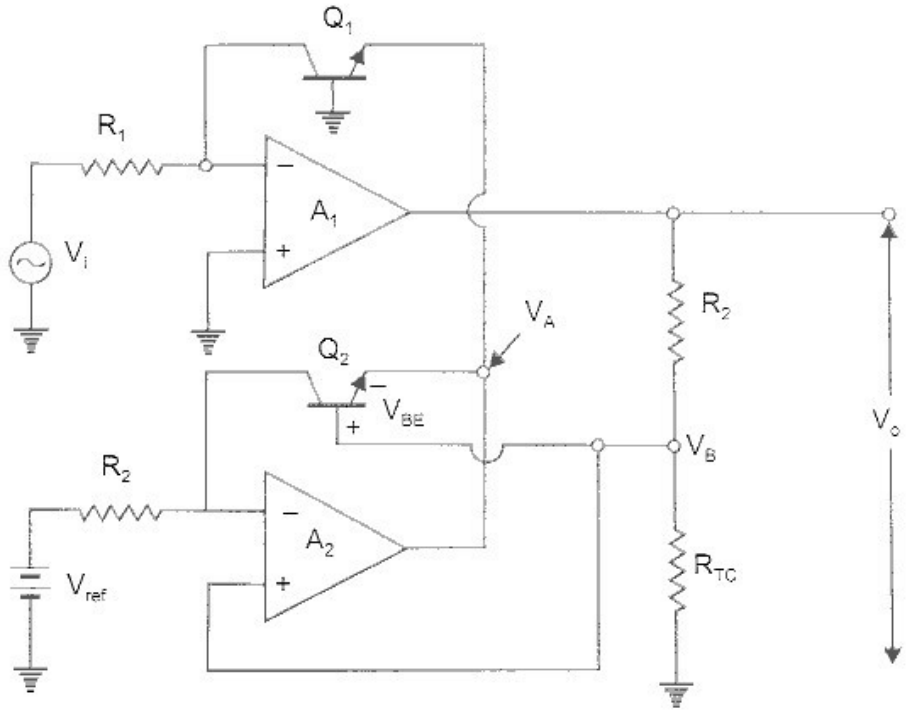


Fig. 4.18 (c) Log-amp using two op-amps only

The circuit in Fig. 4.18 (b) requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output (with an inversion) can be obtained by the circuit of Fig. 4.18 (c) using two op-amps only.

Antilog Amplifier

The circuit is shown in Fig. 4.19. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\ B\text{–}E} = \frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.45}$$

and

$$V_{Q2\ B\text{–}E} = \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.46}$$

Since the base of Q_1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{–}E} = -\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.47}$$

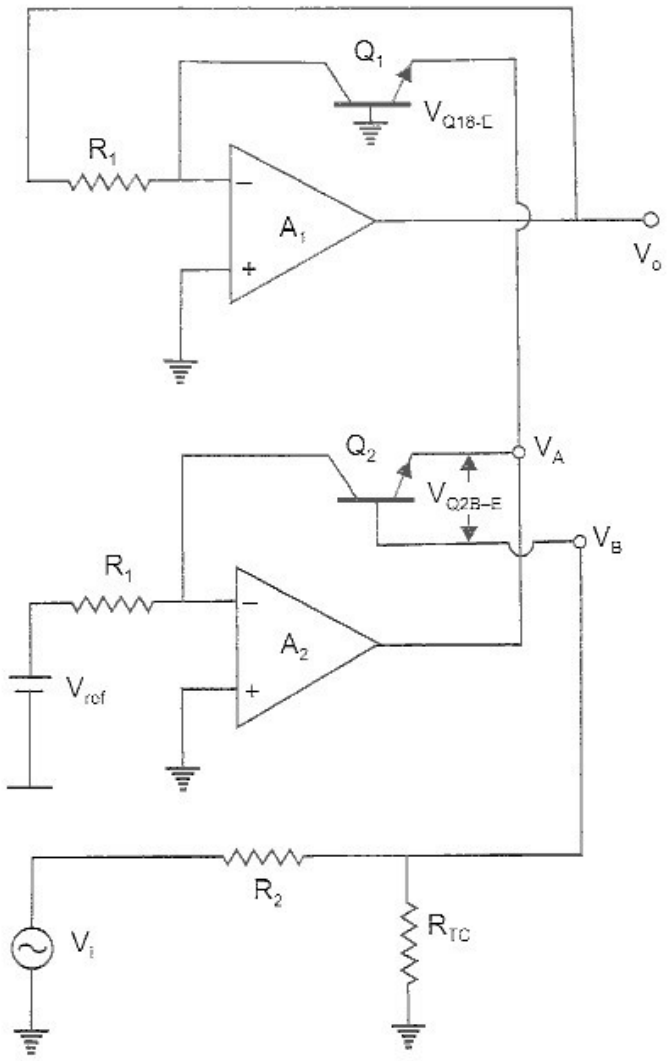


Fig. 4.19 Antilog amplifier

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i \tag{4.48}$$

The voltage at the emitter of Q_2 is

$$V_{Q2\ B\text{-}E} = V_B + V_{Q2\ E\text{-}B}$$

or,
$$V_{Q2\ B\text{-}E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.49}$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\ B\text{-}E}$$

or,
$$-\frac{kT}{q} \ln \frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}} V_i - \frac{kT}{q} \ln \frac{V_{ref}}{R_1 I_s} \tag{4.50}$$

or,
$$\frac{R_{TC}}{R_2 + R_{TC}} V_i = -\frac{kT}{q} \left(\ln \frac{V_o}{R_1 I_s} - \ln \frac{V_{ref}}{R_1 I_s}\right)$$

or, $$-\frac{q}{kT}\frac{R_{TC}}{R_2+R_{TC}}V_i = \ln\left(\frac{V_o}{V_{ref}}\right) \quad (4.51)$$

Changing natural log, i.e., ln to $\log_{10}$ using Eq. (4.38) we get

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right)V_i = 0.4343\times\ln\left(\frac{V_o}{V_{ref}}\right) \quad (4.52)$$

or, $$-K'V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

or, $$\frac{V_o}{V_{ref}} = 10^{-K'V_i}$$

or, $$V_o = V_{ref}(10^{-K'V_i}) \quad (4.53)$$

where $$K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2+R_{TC}}\right) \quad (4.54)$$

Hence an increase of input by one volt causes the output to decrease by a decade. The 755 log/antilog amplifier IC chip is available as a functional module which may require some external components also to be connected to it.

4.9 MULTIPLIER AND DIVIDER

Analog Multiplier

There are a number of applications of analog multipliers such as (i) frequency doubling (ii) measurement of real power (iii) detecting phase-angle difference between two signals of equal frequency (iv) multiplying two signals (v) dividing one signal by another (vi) taking square root of a signal (vii) squaring a signal.

A basic multiplier schematic symbol is shown in Fig. 4.20 (a). Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}. Thus output voltage is a scaled version of x and y inputs. The output voltage is given by

$$v_o = \frac{v_x v_y}{V_{ref}} \quad (4.55)$$

Normally, V_{ref} is internally set to 10 volts. So,

$$v_o = \frac{v_x v_f}{10}$$

As long as

$$v_x < V_{ref}$$

and $$v_y < V_{ref}$$

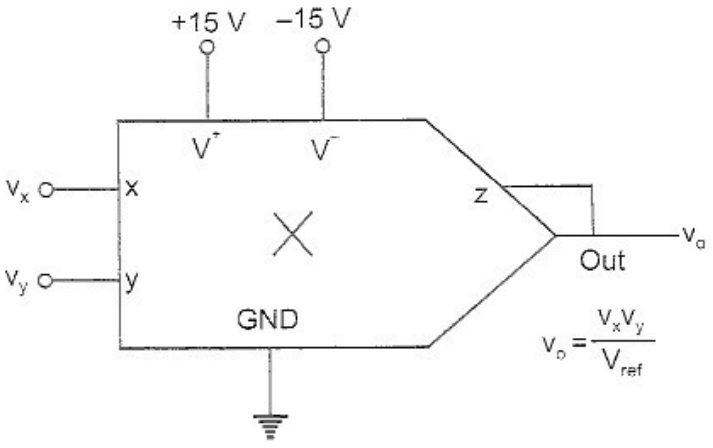


Fig. 4.20 (a) Multiplier schematic symbol

the output of the multiplier will not saturate. Power supply voltage can range from ±8 V to ±18 V. Usually, multipliers are designed for the same type of power supplies as used for op-amps, namely ±15 V.

If both inputs are positive, the IC is said to be a one quadrant multiplier as shown in Fig. 4.20 (b). A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative Fig. 4.20 (c). If both inputs may be either positive or negative, the IC is called a four quadrant multiplier Fig. 4.20 (d).

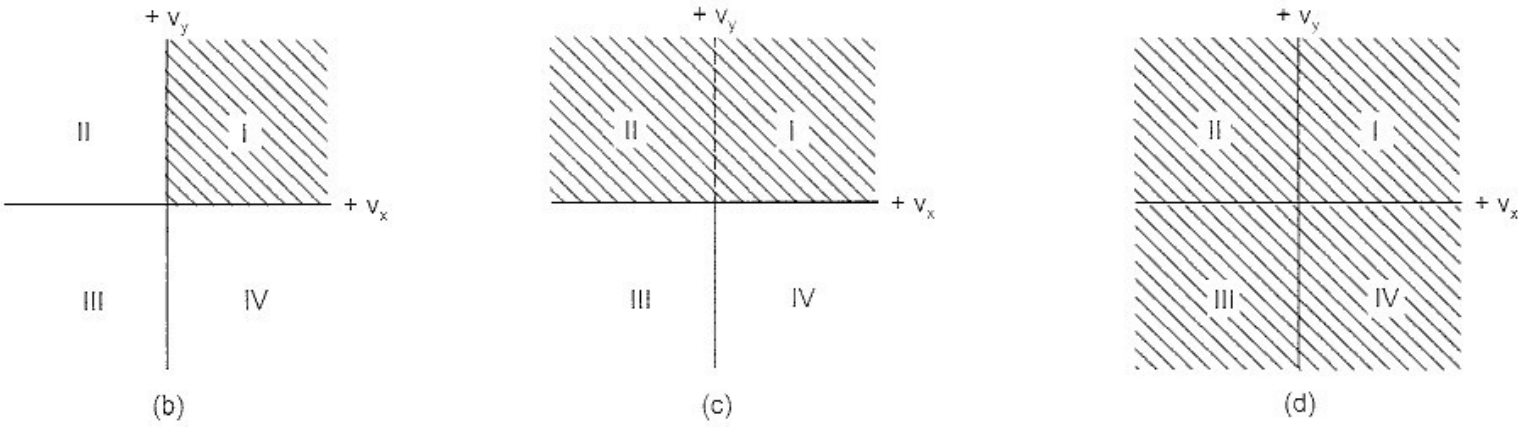


Fig. 4.20 (b) One quadrant multiplier, (c) Two quadrant multiplier (d) Four quadrant multiplier

There can be several ways to make a circuit which will multiply according to Eq. (4.55). One commonly used technique is log-antilog method. The log-antilog method relies on the mathematical relationship that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers.

$$\ln v_x + \ln v_y = \ln (v_x v_y) \tag{4.56}$$

Figure 4.20 (e) is a block diagram of a log-antilog multiplier IC. Log-amps require the input and reference voltages to be of the same polarity. This restricts log-antilog multipliers to one quadrant operation. A technique that provides four quadrant multiplication is transconductance multiplier. Some of the multiplier IC chips available are AD533, AD534, AD633. We now discuss few applications of multiplier IC.

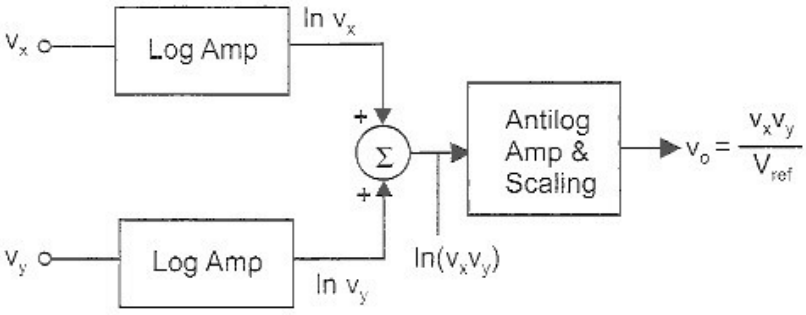


Fig. 4.20 (e) Block diagram of a log-antilog multiplier

Frequency Doubling

The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure *real* power.

Let $$v_x = V_x \sin \omega t \tag{4.57}$$

$$v_y = V_y \sin (\omega t + \theta) \tag{4.58}$$

where θ is the phase difference between the two signals. Applying these two signals to the inputs of a four quadrant multiplier will yield an output as,

$$v_o = \frac{V_x \sin \omega t \, V_y \sin(\omega t + \theta)}{V_{ref}} \tag{4.59}$$

$$= \frac{V_x V_y}{V_{ref}} \sin \omega t (\sin \omega t \cos \theta + \sin \theta \cos \omega t)$$

$$= \frac{V_x V_y}{V_{ref}} (\sin^2 \omega t \cos \theta + \sin \theta \sin \omega t \cos \omega t)$$

But $\sin^2 a = 1 - \cos^2 a$

and $\cos 2a = 2 \cos^2 a - 1$

so $\cos^2 a = \frac{1}{2} + \left(\frac{1}{2}\right) \cos 2a$

$$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a = \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a$$

so $$v_o = \frac{V_x V_y}{V_{ref}} \left[\cos \theta \left(\frac{1}{2} - \left(\frac{1}{2}\right) \cos 2 \omega t \right) + \sin \theta \sin \omega t \cos \omega t \right] \tag{4.60}$$

But, $\sin a \cos a = \left(\frac{1}{2}\right) \sin 2a$

Hence, $$v_o = \frac{V_x V_y}{2 V_{ref}} (\cos \theta - \cos \theta \cos 2\omega t + \sin \theta \sin 2\omega t)$$

or, $$v_o = \frac{V_x V_y}{2V_{ref}} \cos \theta + \frac{V_x V_y}{2V_{ref}} (\sin \theta \sin 2 \omega t - \cos \theta \cos 2 \omega t) \tag{4.61}$$

The first term is a DC and is set by the magnitude of the signals and their phase difference. The second term varies with time, but at twice the frequency of the inputs (2ω).

The circuit works as an ideal doubler if same frequency is applied to both the inputs. For example if

$$v_x = V_x \sin \omega t$$

and $$v_y = V_y \sin \omega t$$

Then $$V_o = \frac{V_x V_y}{V_{ref}} \sin^2 \omega t$$

$$= \frac{V_x V_y}{V_{ref}} \left(1 - \frac{\cos 2 \omega t}{2}\right)$$

The output thus contains a dc term and a negative cosine wave of double frequency. The dc term can be easily removed by using a 1-μF coupling capacitor between load and the output terminal.

Squarer Circuit

The basic multiplier of Fig. 4.20 (a) can be used to square any positive or negative number provided the number can be represented by a voltage between 0 to V_{ref}. The voltage v_i representing the number is connected to both the inputs as shown in Fig. 4.20 (f).

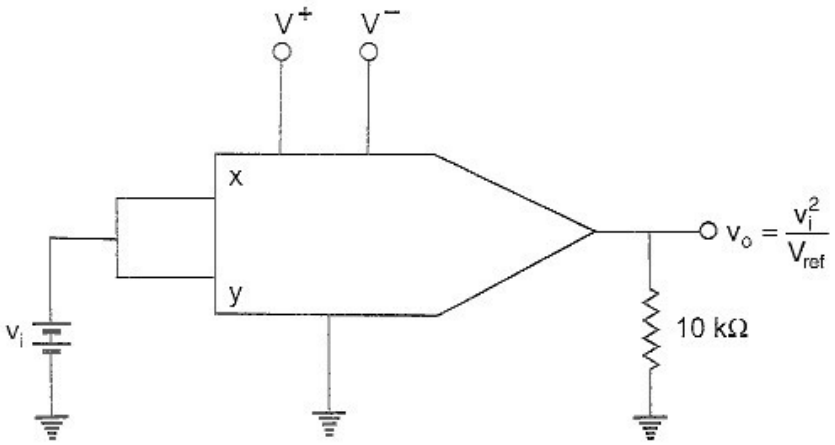


Fig. 4.20 (f) Squarer Circuit

It is possible to square a sinewave voltage too. In Fig. 4.20 (f), if a sinewave voltage $v_i = V_m \sin\omega t$ is applied to both the inputs, then the output voltage, v_o is given by

$$v_o = \frac{v_i^2}{V_{ref}}$$

For $v_i = 5 \sin 2\pi \times 10^4 t$ and $V_{ref} = 10$ V,

$$v_o = \frac{5^2}{10} (\sin 2\pi \times 10^4 t)^2$$

$$= 2.5 \left[\frac{1}{2} - \frac{1}{2}\cos 2\pi \times 2 \times 10^4 t\right] = 1.25 - 1.25 \cos 2\pi \times 2 \times 10^4 t$$

The output contains a dc term and frequency is doubled.

Phase Angle Detection

If the input signals applied to a multiplier are

$$v_x = V_{mx} \sin\omega t \quad (4.62(a))$$

$$v_y = V_{my} \sin(\omega t + \theta) \quad (4.62(b))$$

Then, $$v_o = \frac{V_{mx} V_{my}}{V_{ref.}} \sin\omega t \sin(\omega t + \theta) \quad (4.63(a))$$

$$= \frac{V_{mx} V_{my}}{V_{ref.}} \times \frac{1}{2} [\cos\theta - \cos(2\omega t + \theta)] \quad (4.63(b))$$

The phase difference θ between the two input signals can be calculated from the dc component in the output voltage V_o. That is,

$$V_{o,\,dc} = \frac{V_{mx} V_{my}}{2V_{ref.}} \times \cos\theta \quad (4.64)$$

Divider

Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider in Fig. 4.20 (g) with input signals v_z and v_x as dividend and divisor respectively, is given by

$$v_o = -V_{ref}\frac{v_z}{v_x} \qquad (4.65(a))$$

The result can be derived as follows. The op-amp's inverting terminal is at virtual ground. Therefore,

$$I_z = I_A$$

and

$$I_z = \frac{v_z}{R}$$

The output voltage V_A of the multiplier is determined by the multiplication of v_x and v_y

$$V_A = \frac{v_x v_y}{V_{ref}} = \frac{v_x v_o}{V_{ref}} \qquad (4.65(b))$$

Again $V_A = -I_A R$

so, $$I_A = -V_A/R = -\frac{v_x v_o}{V_{ref} R} \qquad (4.66(a))$$

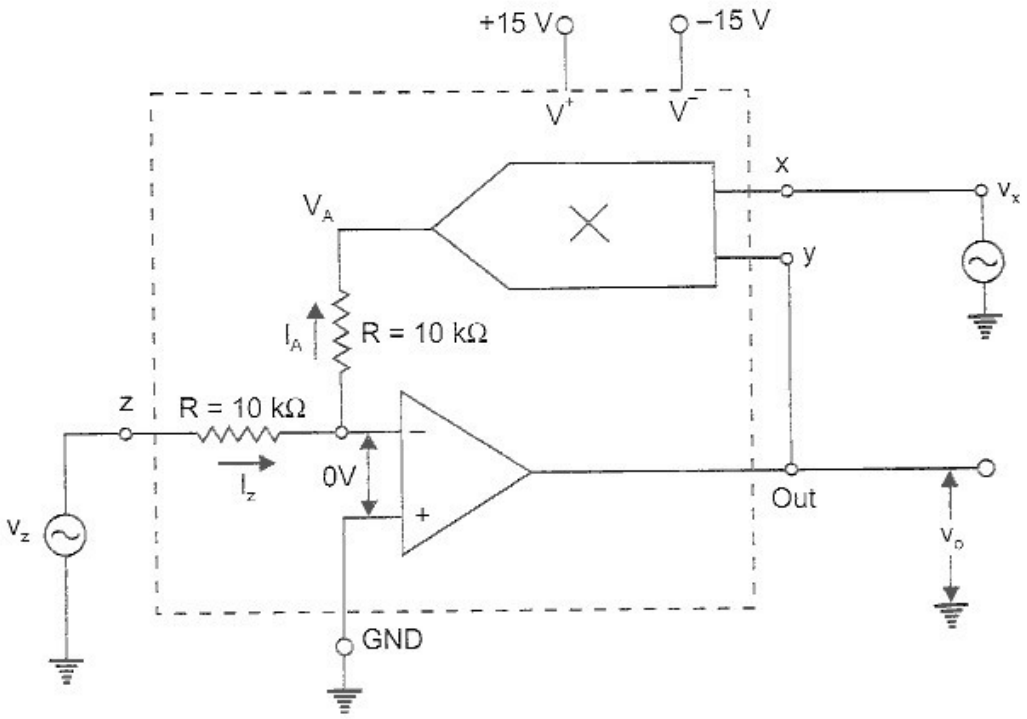


Fig. 4.20 (g) Multiplier IC configured as divider

As, $I_z = I_A$

so, $$I_z = -\frac{v_x v_o}{V_{ref} R}$$

and

$$v_z = I_z R = -\frac{v_x v_o}{V_{ref}}$$

or, $$v_o = -V_{ref}\frac{v_z}{v_x} \qquad (4.66(b))$$

Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

Finding Square Roots

A divider circuit can be used to find square roots by connecting both the inputs of the multiplier to the output of an op-amp as shown in Fig. 4.20 (h).

In Fig. 4.20 (h)

$$V_A = \frac{V_o^2}{V_{ref}}$$

and $V_A = -V_{in}$

So $V_o^2 = -V_{in} V_{ref}$

or $$V_o = \sqrt{V_{ref} |V_{in}|} \qquad (4.67)$$

(taking magnitude only)

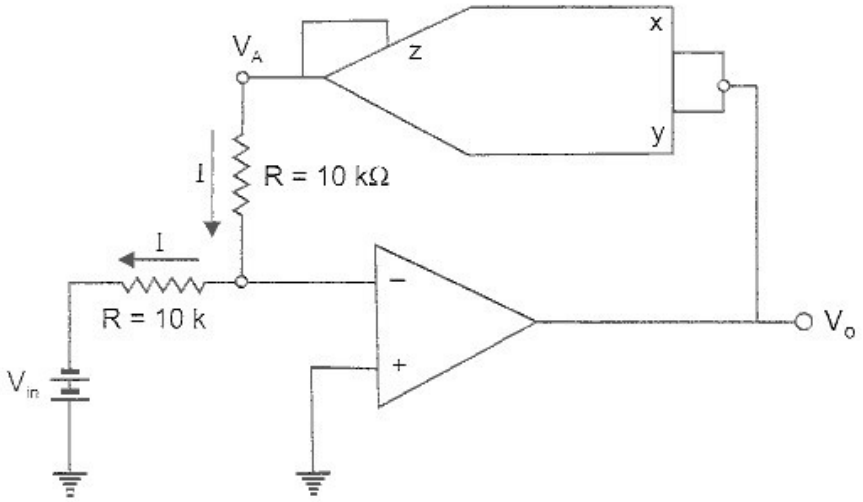


Fig. 4.20 (h) Finding square roots

Thus, output V_o is proportional to square root of magnitude of V_{in}. Note that V_{in} must be negative or else op-amp will saturate. The range of V_{in} lies between –1 and –10 V.

4.10 DIFFERENTIATOR

One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform. A differentiator circuit is shown in Fig. 4.21 (a).

Analysis

The node N is at virtual ground potential i.e., $v_N = 0$. The current i_C through the capacitor is,

$$i_C = C_1 \frac{d}{dt}(v_i - v_N) = C_1 \frac{dv_i}{dt} \qquad (4.68)$$

The current i_f through the feedback resistor is v_o/R_f and there is no current into the op-amp. Therefore, the nodal equation at node N is,

$$C_1 \frac{dv_i}{dt} + \frac{v_o}{R_F} = 0$$

from which we have

$$\boxed{v_o = -R_F C_1 \frac{dv_i}{dt}} \qquad (4.69)$$

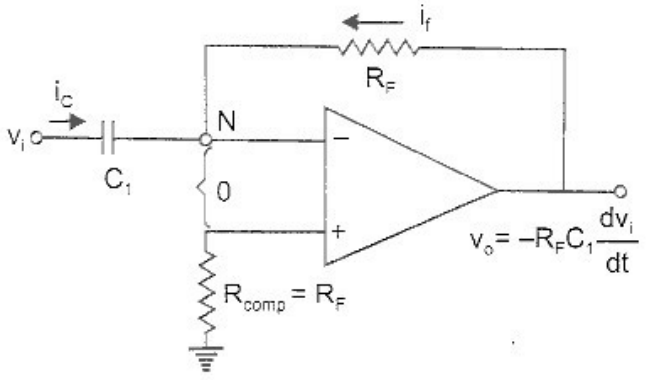


Fig. 4.21 (a) Op-amp differentiator

Thus the output voltage v_o is a constant $(-R_F C_1)$ times the derivative of the input voltage v_i and the circuit is a differentiator. The minus sign indicates a 180° phase shift of the output waveform v_o with respect to the input signal.

The phasor equivalent of Eq. (4.69) is, $V_o(s) = -R_F C_1 s V_i(s)$ where V_o and V_i is the phasor representation of v_o and v_i. In steady state, put $s = j\omega$. We may now write the magnitude of gain A of the differentiator as,

$$|A| = \left| \frac{V_o}{V_i} \right| = |-j\omega R_F C_1| = \omega R_F C_1 \tag{4.70}$$

From Eq. (4.70), one can draw the frequency response of the op-amp differentiator. Equation (4.70) may be rewritten as

$$|A| = \frac{f}{f_a}$$

where

$$f_a = \frac{1}{2\pi R_F C_1} \tag{4.71}$$

At $f = f_a$, $|A| = 1$, i.e., 0 dB, and the gain increases at a rate of +20 dB/decade. Thus at high frequency, a differentiator may become unstable and break into oscillation. There is one more problem in the differentiator of Fig. 4.21 (a). The input impedance (i.e., $1/\omega C_1$) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

Practical Differentiator

A practical differentiator of the type shown in Fig. 4.21 (b) eliminates the problem of instability and high frequency noise.

The transfer function for the circuit in Fig. 4.21 (b) is given by,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_F}{Z_1} = -\frac{s R_F C_1}{(1 + s R_F C_F)(1 + s C_1 R_1)} \tag{4.72}$$

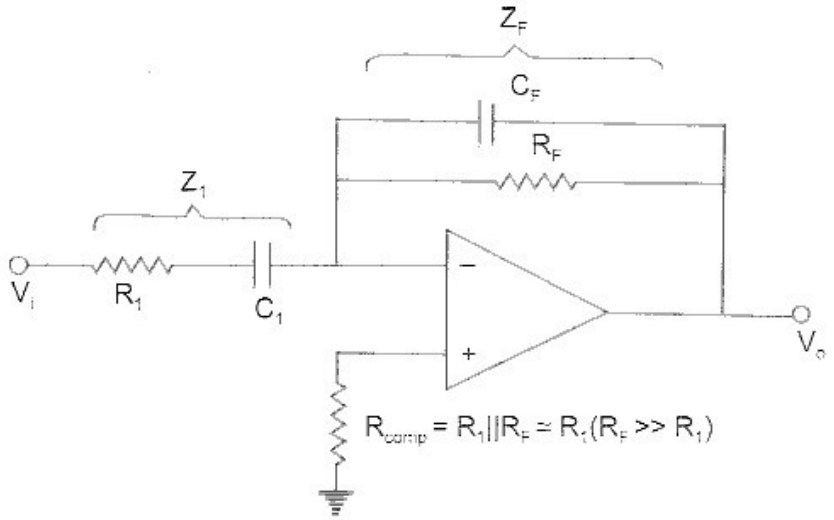


Fig. 4.21 (b) Practical differentiator

For $R_F C_F = R_1 C_1$, we get

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_F C_1}{(1+sR_1 C_1)^2} = -\frac{sR_F C_1}{\left(1+j\dfrac{f}{f_b}\right)^2} \tag{4.73}$$

where, $$f_b = \frac{1}{2\pi R_1 C_1} \tag{4.74}$$

From Eq. (4.73), it is evident that the gain increases at +20 dB/decade for frequency $f < f_b$ and decreases at –20 dB/decade for $f > f_b$ as shown by dashed lines in Fig. 4.21 (c). This 40 dB/decade change in gain is caused by $R_1 C_1$ and $R_F C_F$ factors. For the basic differentiator of Fig. 4.21 (a), the frequency response would have increased continuously at the rate of +20 dB/decade even beyond f_b causing stability problem at high frequency. Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems. The value of f_b should be selected such that,

$$f_a < f_b < f_c$$

where f_c is the unity gain-bandwidth of the op-amp in open-loop configuration.

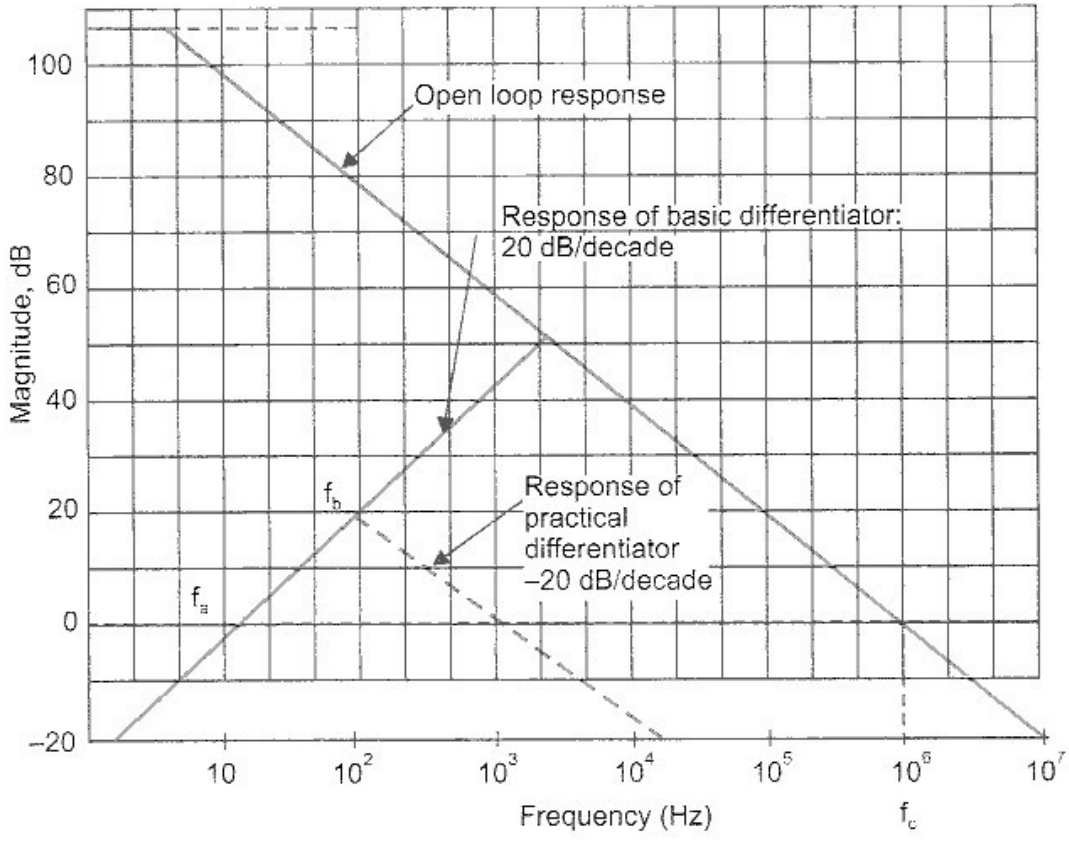


Fig. 4.21 (c) Frequency response

For good differentiation, one must ensure that the time period T of the input signal is larger than or equal to $R_F C_1$, that is,

$$T \geq R_F C_1 \tag{4.75}$$

It may be noted that for $R_F C_1$ much greater than $R_1 C_1$ or $R_F C_F$, Eq. (4.72) is reduced to, $V_o/V_i = -sR_F C_1$, that is, the expression of the output voltage remains the same as in the case of an ideal differentiator as

$$v_o = -R_F C_1 \frac{dv_i}{dt} \tag{4.76}$$

A resistance R_{comp} $(= R_1 \,||\, R_F)$ is normally connected to the (+) input terminal to compensate for the input bias circuit.

A good differentiator may be designed as per the following steps:

1. Choose f_a equal to the highest frequency of the input signal. Assume a practical value of C_1 (<1 μF) and then calculate R_F.
2. Choose $f_b = 10\, f_a$ (say). Now calculate the values of R_1 and C_F so that $R_1C_1 = R_FC_F$.

Example 4.3

(a) Design an op-amp differentiator that will differentiate an input signal with f_{max} = 100 Hz.
(b) Draw the output waveform for a sine wave of 1 V peak at 100 Hz applied to the differentiator.
(c) Repeat part (b) for a square wave input.

Solution

(a) Select, $f_a = f_{max} = 100 \text{ Hz} = \dfrac{1}{2\pi R_F C_1}$ [from Eq. (4.71)]

Let $C_1 = 0.1\ \mu\text{F}$,

then $R_F = \dfrac{1}{2\pi (10^2)(10^{-7})} = 15.9\ \text{k}\Omega$

Now choose $f_b = 10 f_a = 1\ \text{kHz} = \dfrac{1}{2\pi R_1 C_1}$ [from Eq. (4.74)]

Therefore, $R_1 = \dfrac{1}{2\pi (10^3)(10^{-7})} = 1.59\ \text{k}\Omega$

Since $R_F C_F = R_1 C_1$,

we get, $C_F = \dfrac{1.59 \times 10^3 \times 10^{-7}}{15.9 \times 10^3} = 0.01\ \mu\text{F}$

(b) $v_i = 1 \sin 2\pi(100)t$

From Eq. (4.69),

$$v_o = -R_f C_1 \frac{dv_i}{dt} = -(15.9\ \text{k}\Omega)\ (0.1\ \mu\text{F})\ \frac{d}{dt}[(1\ \text{V}) \sin (2\pi)(10^2)\, t]$$

$$= -(15.9\ \text{k}\Omega)\ (0.1\ \mu\text{F})\ (2\pi)\ (10^2) \cos [(2\pi)\ (10^2)t] = -0.999 \cos [2\pi\ (10^2)t]$$

$$= -\ 1 \cos [(2\pi)\ (10^2)\, t]$$

The input and output waveforms are shown in Fig. 4.22 (a).

(c) For a square wave input, say 1 V peak and 1 KHz, the output waveform will consist of positive and negative spikes of magnitude V_{sat} which is approximately 13 V for ± 15 V op-amp power supply.

During the time periods for which input is constant at ±1 V, the differentiated output will be zero. However, when input transits between ±1 V levels, the slope of the input is infinite for an ideal square wave. The output, therefore, gets clipped to about ± 13V for a ±15 V op-amp power supply as shown in Fig. 4.22 (b).

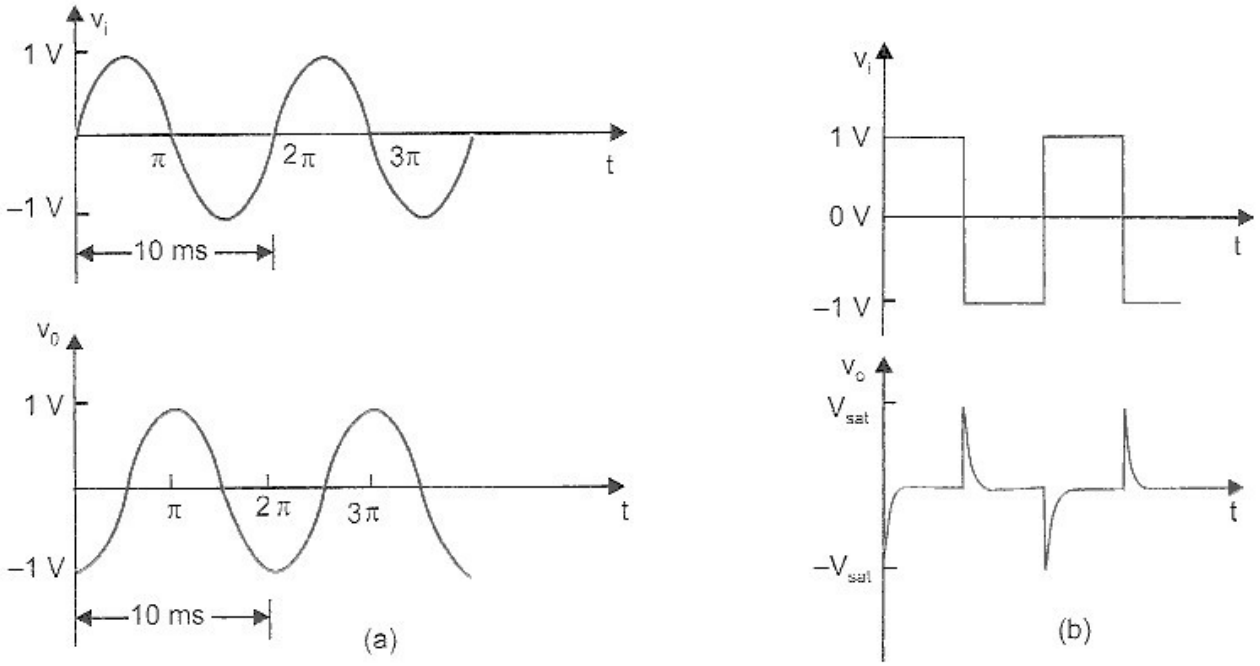


Fig. 4.22 (a) Sine-wave input and cosine output, (b) Square wave input and spike output

4.11 INTEGRATOR

If we interchange the resistor and capacitor of the differentiator of Fig. 4.21 (a), we have the circuit of Fig. 4.23 (a) which as we will see, is an integrator. The nodal equation at node N is,

$$\frac{v_i}{R_1} + C_F \frac{dv_o}{dt} = 0 \qquad (4.77)$$

or, $$\frac{dv_o}{dt} = -\frac{1}{R_1 C_F} v_i$$

Integrating both sides, we get

$$\int_0^t dv_o = -\frac{1}{R_1 C_F} \int_0^t v_i \, dt$$

$$v_o(t) = -\frac{1}{R_1 C_F} \int_0^t v_i(t)\, dt + v_o(0) \qquad (4.78)$$

where $v_o(0)$ is the initial output voltage.

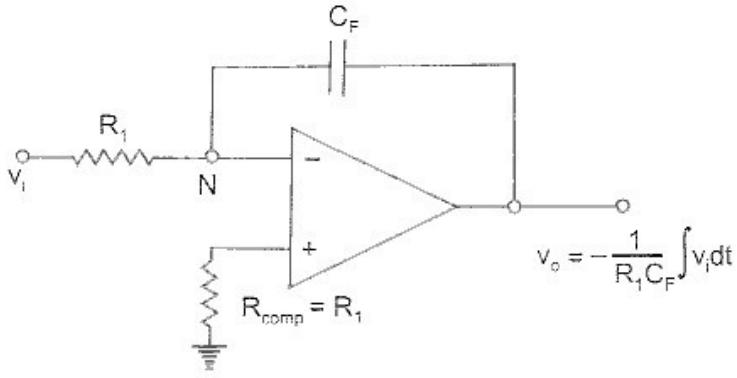


Fig. 4.23 (a) Op-amp integrator

The circuit, thus provides an output voltage which is proportional to the time integral of the input and R_1C_F is the time constant of the integrator. It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is also known as an inverting integrator. A resistance, $R_{comp} = R_1$ is usually connected to the (+) input terminal to minimize the effect of input bias current.

A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However, in the op-amp integrator of Fig. 4.23, by Miller's theorem, the effective input capacitance becomes $C_F(1 - A_v)$ where A_v is the gain of the op-amp. The gain A_v is infinite for an ideal op-amp, so the effective time constant of the op-amp integrator becomes very large which results in perfect integration.

The operation of the integrator can also be studied in the frequency domain. In phasor notation, Eq. (4.78) can be written as

$$V_o(s) = -\frac{1}{sR_1C_F}V_i(s) \tag{4.79}$$

In steady state, put $s = j\omega$ and we get

$$V_o(j\omega) = -\frac{1}{j\omega R_1C_F}V_i(j\omega) \tag{4.80}$$

So, the magnitude of the gain or integrator transfer function is

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1C_F}\right| = \frac{1}{\omega R_1C_F} \tag{4.81}$$

The frequency response (or Bode Plot) of this basic integrator is shown in Fig. 4.23 (b). The Bode plot is a straight line of slope –6B/octave (or equivalently –20 dB/decade). The frequency f_b in Fig. 4.23 (b) is the frequency at which the gain of the integrator is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1C_F}$$

It can further be seen from Eq. (4.81) that at $\omega = 0$, the magnitude of the integrator transfer function is infinite. At dc, the capacitor C_F behaves as an open circuit and there is no negative feedback. The op-amp thus operates in open loop, resulting in an infinite gain. In practice, of course, output never becomes infinite, rather the output of the amplifier saturates at a voltage close to the op-amp positive or negative power supply depending on the polarity of the input dc signal.

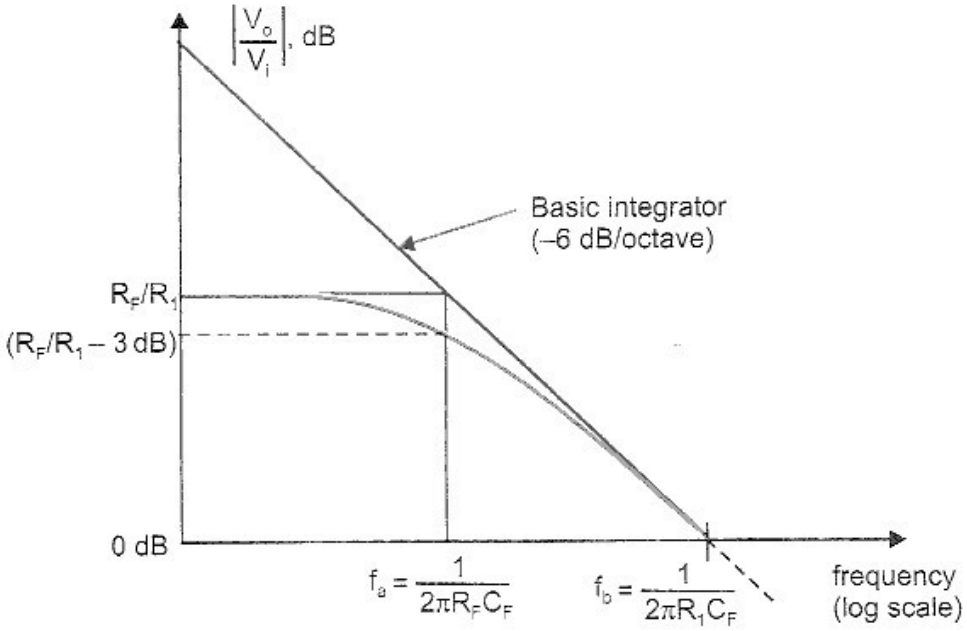


Fig. 4.23 (b) Frequency response of a basic and Lossy integrator

As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc ($\omega \cong 0$), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

Practical Integrator Circuit (Lossy Integrator)

The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance R_F as shown in Fig. 4.23 (c). The parallel combination of R_F and C_F behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called a lossy integrator. The resistor R_F limits the low frequency gain to $-R_F/R_1$ (generally $R_F = 10\,R_1$) and thus provides dc stabilization.

Analysis

The nodal equation at the inverting input terminal of the op-amp of Fig. 4.23 (c) is,

$$\frac{V_i(s)}{R_1} + s\,C_F\,V_o(s) + \frac{V_o(s)}{R_F} = 0 \tag{4.82}$$

from which we have,

$$V_o(s) = -\frac{1}{sR_1C_F + R_1/R_F}\,V_i(s) \tag{4.83}$$

If R_F is large, the lossy integrator approximates the ideal integrator. For $s = j\omega$, magnitude of the gain of lossy integrator is given by

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R_1^2 C_F^2 + R_1^2/R_F^2}} = \frac{R_F/R_1}{\sqrt{1+(\omega R_F C_F)^2}} \tag{4.84}$$

The Bode plot of the lossy integrator is also shown in Fig. 4.23 (b). At low frequencies gain is constant at R_F/R_1. The break frequency ($f = f_a$) at which the gain is 0.707 (R_F/R_1) (or – 3dB below its value of R_F/R_1) is calculated from Eq. (4.84) as

$$\sqrt{1+(\omega R_F C_F)^2} = \sqrt{2}$$

Solving for $f = f_a$, we get

$$f_a = \frac{1}{2\pi R_F C_F} \tag{4.85}$$

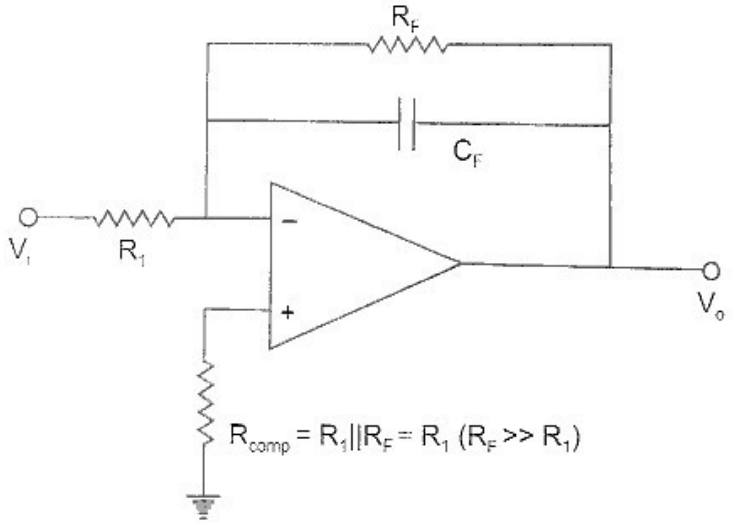


Fig. 4.23 (c) Practical or lossy integrator circuit

This is a very important frequency. It tells us where the useful integration range starts. If the input frequency is lower than f_a the circuit acts like a simple inverting amplifier and no integration results. At input frequency equal to f_a, 50% accuracy results. The practical thumb rule is that if the input frequency is 10 times f_a, than 99% accuracy can result.

Initial Conditions

An integrator must also be provided with an external circuit to introduce initial conditions as shown in Fig. 4.24. When ganged switch S is in position 1, the input is zero and the capacitor is charged to the voltage V almost instantaneously* setting an initial condition of $v_o(0) = V$. When the switch S is in position 2, the amplifier is connected as in integrator and its output will be V plus a constant $-1/R_1 C_F$ times the time integral of the input voltage v_i. The capacitor C_F should have very low leakage and is usually a Teflon, Polystyrene or Mylar dielectric with typical capacitance value ranging from 0.001 to 10 μF is used.

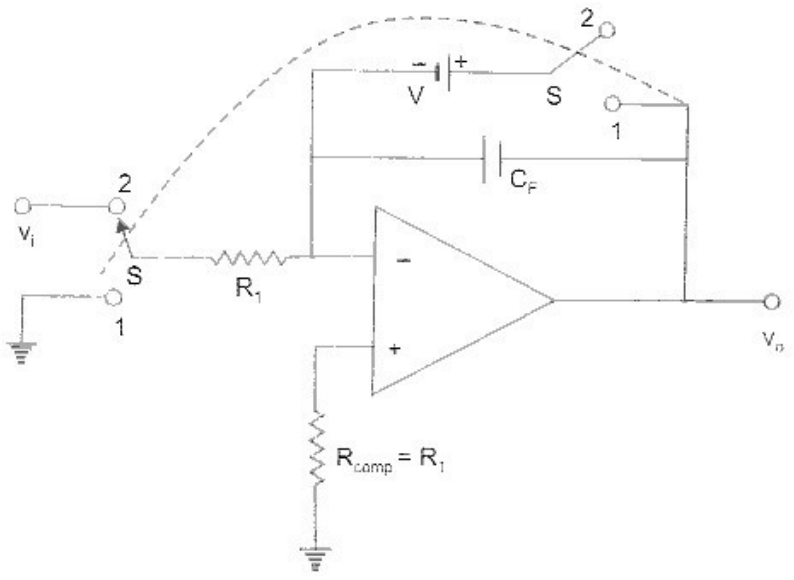


Fig. 4.24 Integrator circuit showing initial condition

Example 4.4

Consider the lossy integrator shown in Fig. 4.23 (c). For the component values. $R_1 = 10\ \text{k}\Omega$, $R_F = 100\ \text{k}\Omega$, $C_F = 10\ \text{nF}$, determine the lower frequency limit of integration and study the response for the inputs (i) sine wave, (ii) step input (iii) square wave.

Solution

For the given component values, the lower frequency limit of integration f_a is

$$f_a = \frac{1}{2\pi R_F C_F} = \frac{1}{2\pi \times 100\ \text{k}\Omega \times 10\ \text{nF}} = 159\ \text{Hz}$$

For 99% accuracy, the input frequency should be at least one decade above f_a i.e., 1.59 kHz. Accurate integration can be achieved beyond this frequency. However, there is an upper limit up to which circuit will integrate and it is determined by the frequency response of op-amp. However, as input frequency is increased, the output amplitude reduces as the gain of the integrator falls at a rate of 6 dB/octave.

(i) Sine wave input: For an input of 1 V peak sine wave at 5 kHz, the output v_o is

$$v_o(t) = -\frac{1}{R_1 C_F}\int v_i(t)\,dt = -\frac{1}{10\ \text{k}\Omega \times 10\ \text{nF}}\int 1 \sin(2\pi\ \ 5000\,t)\,dt$$

$$= -10^4 \int \sin(2\pi\ \ 5000\,t)\,dt = -\frac{10^4}{2\pi\ 5000}\left[-\cos(2\pi\ \ 5000\,t)\right]$$

$$= 0.318\ \cos\ (2\pi\ 5000\ t)$$

The output is a cosine wave with a peak amplitude of 0.318 V only as shown in Fig. 4.25 (a). If the frequency of the input is raised by a factor of 10 to 50 kHz, the output would be a cosine wave of frequency 50 kHz but with an amplitude of 31.8 mV only.

*In about four time constant, that is, 4 $R_o C_f$ where R_o is the small internal resistance of the voltage source V.