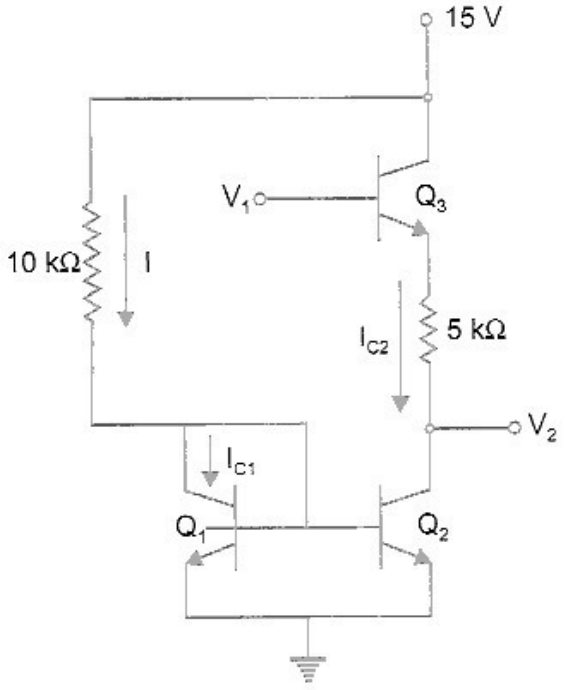

Fig. 2.31 Circuit of Example 2.16

$$V_1 - V_2 = V_{BE3} + I_{C2} \times 5\ \text{k}\Omega = 0.7\text{V} + 1.43 \times 5\ \text{k}\Omega = 7.85\ \text{V}.$$

2.4.8 Output Stage

The function of the last stage, that is, the output stage in an op-amp is to supply the load current and provide a low impedance output. It should also provide a large output voltage saving, ideally the total supply voltage i.e., $V_{CC} + V_{EE}$. A simple output stage consists of two complimentary transistors Q_1 (*npn*) and Q_2 (*pnp*) connected as emitter followers as shown in Fig. 2.32 (a). It can be seen that for v_i positive, transistor Q_1 is ***on*** and supplies current to load R_L. And, if v_i is negative, Q_1 is cut off and Q_2 acts as a sink to remove current from the load R_L. There is, however, a limitation in this circuit. The output voltage v_o remains

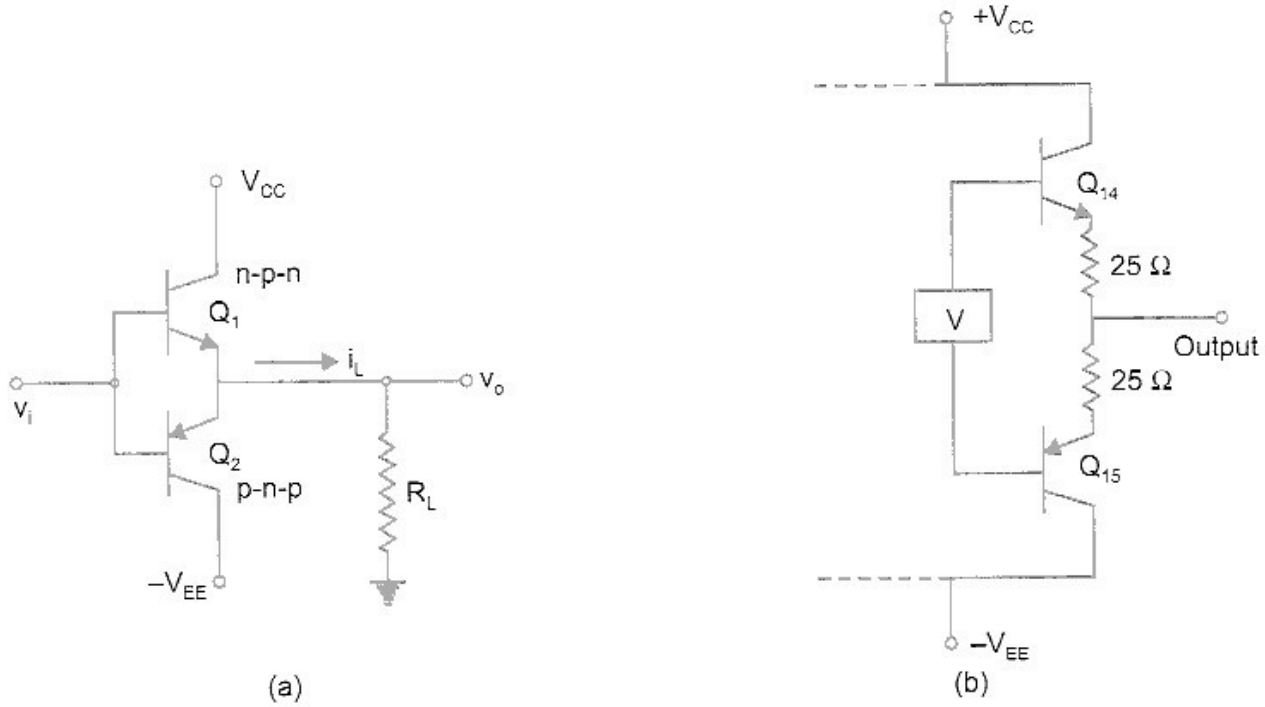

Fig. 2.32 (a) A complementary emitter follower output stage (b) Output stage of μA741

zero until the input v_i exceeds V_{BE} (cut in) = 0.5 V. This is called cross-over distortion. It can be eliminated by applying a bias voltage V slightly greater than 2 $V_{BE\,(cut\ in)}$ = 1 V between the two bases, so that a small current flows in the transistors even in the quiescent state. The output stage of μA741 op-amp is shown in Fig. 2.32 (b). The block marked V is the V_{BE} multiplier of the type shown in Fig. 2.30 (d). It is designed to supply a voltage of about 1 V between the bases of the complementary pair of transistors Q_{14} and Q_{15}. The small emitter resistors (25 Ω) stabilize the quiescent base current.

2.5 EXAMPLES OF IC OP-AMPS

We are now in a position to analyse the complete circuit of commercially available op-amps. Two such IC op-amps discussed are Motorola MC 1530 and Fairchild μA741.

2.5.1 Motorola MC1530 Op-Amp

The circuit of MC 1530 is shown in Fig. 2.33. It is easily seen that the circuit consists of four stages. Transistors Q_2 and Q_3 form the first diff-amp stage driven by the constant current source Q_1. The output of the first diff.-amp drives the second diff.-amp formed by Q_4 and Q_5. The single ended output of the second diff-amp drives the level shifter Q_6 (emitter follower). Q_7 and diode D_3 forms another constant current source of the type shown in Fig. 2.15. The diode connected transistor Q_1 of Fig. 2.15 is shown by diode D_3 here. The output stage of MC1530 uses Q_8, Q_9 and Q_{10} where Q_9 and Q_{10} are in totem-pole configuration.

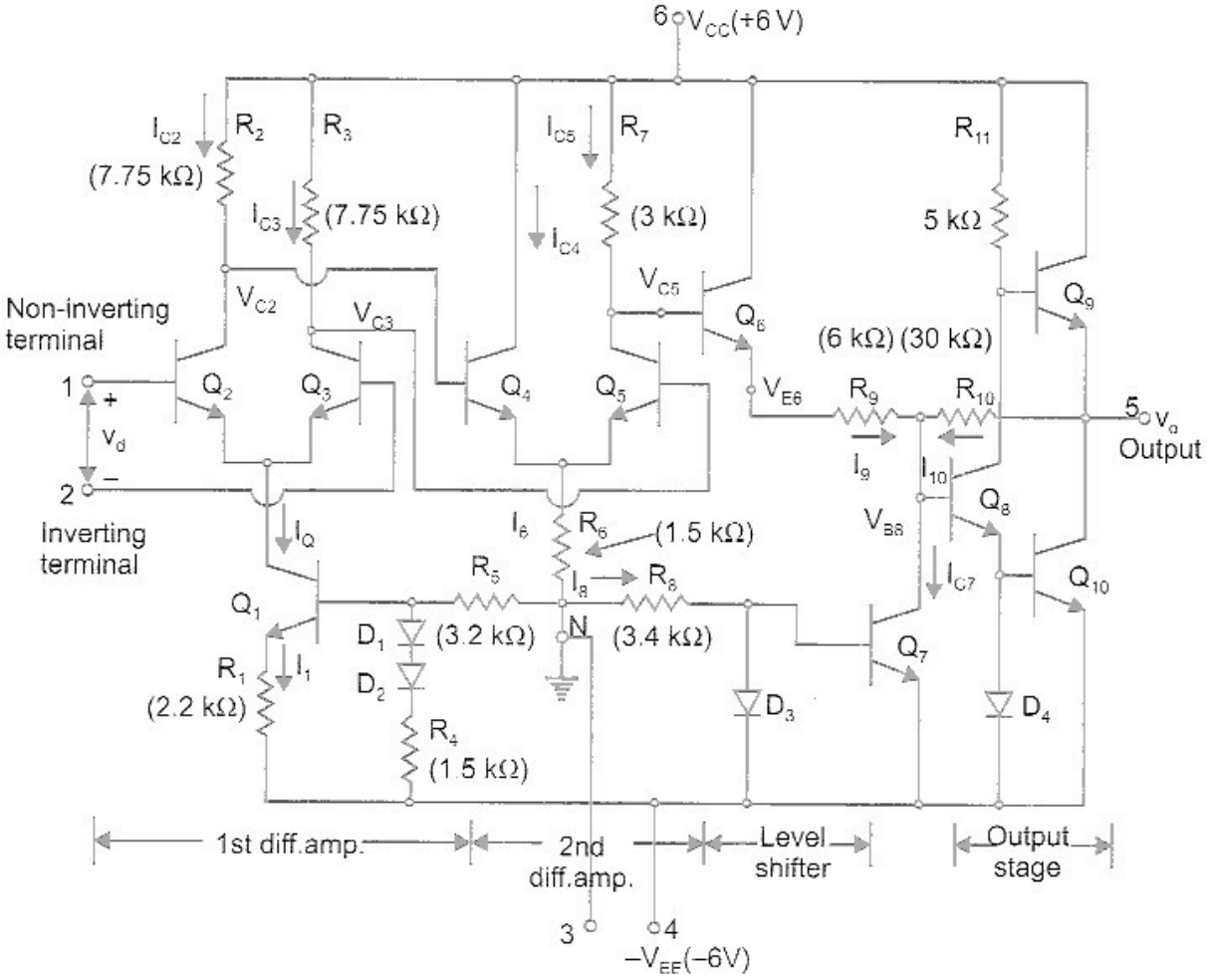

Fig. 2.33 Internal circuit of Motorola MC 1530

Example 2.17

From the circuit of Fig. 2.33 calculate,

(1) The collector current in each transistor and the output voltage under quiescent conditions.

(2) The open loop voltage gain.

Assume $h_{fe} = 100$ and $V_{BE} = V_D = 0.7$ V.

Solution

(1) The d.c. analysis is performed by assuming that both the inverting and non-inverting terminals are at ground potential. To determine the collector current in Q_2 and Q_3, first calculate the constant current I_Q. If the base current of Q_1 is neglected, then $I_Q = I_1$. The voltage V_{BN1} at the base of transistor Q_1 with respect to ground N is written using voltage divider rule as,

$$V_{BN1} = \frac{[-V_{EE} + V_D + V_D]\,R_5}{R_1 + R_5}$$

$$= \frac{(-6\text{ V} + 1.4\text{ V})\,(3.2\text{ k}\Omega)}{1.5\text{ k}\Omega + 3.2\text{ k}\Omega} = -3.13\text{ V}$$

$$I_1 = \frac{V_{EE} + V_{BN1} - V_{BE1}}{R_1} = \frac{6\text{ V} - 3.13\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} = 0.986\text{ mA}$$

So $I_Q = 0.986$ mA

Under dc conditions, half of the I_Q flows through each of transistors Q_2 and Q_3. Therefore, $I_{C2} = I_{C3} = I_{Q2} = 0.493$ mA. The voltage at the collector of Q_2 and Q_3 is,

$$V_{C2} = V_{C3} = V_{CC} - R_2 I_{C2} = 6\text{ V} - (7.75\text{ k}\Omega)\,(0.493\text{ mA}) = 2.18\text{ V}$$

So the voltage at the base of Q_4 and Q_5 is 2.18 V. The dc voltage at the emitter of Q_4 is,

$$V_{E4} = V_{C2} - V_{BE4} = 2.18\text{ V} - 0.7\text{ V} = 1.48\text{ V}.$$

So,

$$I_6 = \frac{V_{E4}}{R_6} = \frac{1.48\text{ V}}{1.5\text{ k}\Omega} = 0.987\text{ mA}.$$

This current divides equally in transistors Q_4 and Q_5, so that

$$I_{C4} = I_{C5} = \frac{I_6}{2} = 0.494\text{ mA}$$

$$V_{C5} = V_{CC} - I_{C5} R_7 = 6\text{ V} - (0.494\text{ mA})\,(3\text{ k}\Omega) = 4.52\text{ V}$$

$$V_{E6} = V_{C5} - V_{BE6} = 4.52\text{ V} - 0.7\text{ V} = 3.82\text{ V}$$

Transistor Q_7 along with diode D_3 forms a current mirror of the type shown in Fig. 2.15. Hence,

$$I_{C7} = I_8 = \frac{V_{EE} - V_{D3}}{3.4} = 1.56\text{ mA}.$$

To calculate the current I_9, first calculate the voltage at the base of Q_8,

$$V_{B8} = V_{BE8} + V_{D4} - V_{EE} = 0.7\text{ V} + 0.7\text{ V} - 6\text{ V} = -4.60\text{ V}$$

$$I_9 = \frac{V_{E6} - V_{B8}}{R_9} = \frac{3.82\text{ V} + 4.6\text{ V}}{6\text{ k}\Omega} = 1.40\text{ mA}$$

$$I_{10} = I_{C7} - I_9 = 1.56\text{ mA} - 1.40\text{ mA} = 0.16\text{ mA}$$

The voltage V_o at the output terminal is,

$$V_o = I_{10}R_{10} + V_{B8} = (0.16\text{ mA})\ (30\text{ k}\Omega) - 4.60\text{ V} = 0.20\text{ V}$$
$$\simeq 0\text{ V (as expected)}$$

(2) In order to calculate the overall voltage gain, we first calculate the voltage gain of the differential amplifier stages. For this we must know the ac emitter resistance h_{ie} of the transistor used.

$$h_{ie} = \frac{h_{fe}V_T}{|I_C|}$$

where V_T is the volt equivalent of temperature = 26 mV at room temperature.

Since $I_{C2} = I_{C3} = I_{C4} = I_{C5} \simeq 0.5\text{ mA}$

So $$h_{ie} = \frac{(100)(26\text{ mV})}{0.5\text{ mA}} = 5.2\text{ k}\Omega$$

Since emitter of Q_4–Q_5 is at ground potential under ac operation the input resistance h_{ie} of Q_4 and Q_5 is effectively in parallel to collector circuit load (R_2 and R_3) of first diff-amp. The effective load of Q_2 and Q_3 is

$$R_{L2} = R_{L3} = 7.75\text{ k}\Omega \,||\, 5.2\text{ k}\Omega = 3.12\text{ k}\Omega$$

The output of the first stage is double ended, its differential gain is given by Eq. (2.53) as

So, $$A_{V1} = \frac{v_{C3} - v_{C2}}{v_d} = \frac{h_{fe}R_{L2}}{h_{ie}} = \frac{100\text{ Ÿ }3.12\text{ k}\Omega}{5.2\text{ k}\Omega} = 60$$

For the second stage, $h_{fe} = 100$, $h_{ie} = 5.2\text{ k}\Omega$ and load $R_7 = 3\text{ k}\Omega$ (neglecting loading on Q_5 of the emitter follower Q_6). The output of the second stage is single ended, so its differential gain is,

$$A_{V2} = \frac{v_{C5}}{v_{C3}} = -\frac{1}{2}\frac{h_{fe}R_7}{h_{ie}} = -\frac{100 \times 3\text{ k}\Omega}{2 \times 5.2\text{ k}\Omega} = -28.9$$

The third stage is the emitter follower, so, $A_{V3} \simeq 1$

The last output stage uses voltage shunt feedback network R_9–R_{10},

so $$A_{V4} \simeq \frac{R_{10}}{R_9} = -\frac{30}{6} = -5$$

Hence the overall op-amp gain is,

$$A_V = (60)\ (-28.9)\ (-5) = 8670$$

2.5.2 741 Op-Amp

741 Op-amp has become an industry standard today. The pin configuration and the complete schematic circuit diagram for 741 op-amp is shown in Fig. 2.34 (a) and (b) respectively. Since this circuit is quite complex compared to MC1530, only the qualitative analysis is taken up.

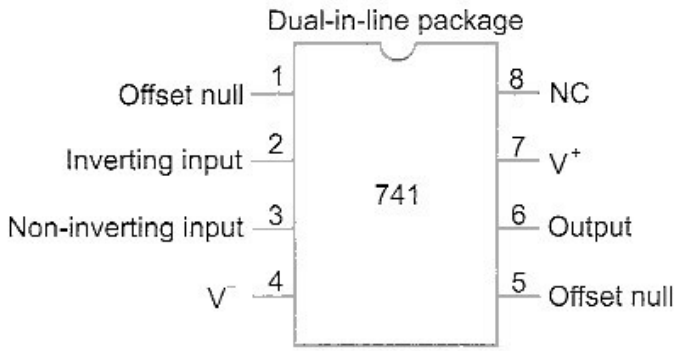

Fig. 2.34 (a) Pin configuration

In understanding an op-amp circuit as complex as this (24 transistors), first we identify the stages which provide signal gain. The input stage diff-amp consists of transistors Q_1–Q_3 and Q_2–Q_4. Transistors Q_{16} and Q_{17} provide the second stage voltage gain. Transistors Q_1Q_3 and Q_2Q_4 are in cascode (CE-CB) configuration. Two transistors in series (Q_1 feeds Q_3) provide high gain per stage needed to achieve the adequate open-loop gain in a two stage amplifier. The transistors Q_5, Q_6 and Q_7 form the active load for Q_3 and Q_4. Transistors Q_5 and Q_6 also function as a differential amplifier for the external offset nulling signal. The emitter current of transistors Q_5 and Q_6 can be controlled by varying a 10 kΩ potentiometer that is externally connected between offset null terminals as shown by dotted line in Fig. 2.34 (b). Bias currents for the input stage are provided by a complicated arrangement of current mirror pairs. Q_{12} generates a current in Q_{11}. This current is reflected over to Q_{10} (though reduced because of the emitter feedback due to R_4). This, in turn, generates a series current in Q_9 which is reflected across another mirror pair to Q_8. The bias current of Q_3 and Q_4 is effectively driven by the mirror pair Q_{10} and Q_{11}. The output of the first diff.-amp is taken at the junction of Q_4 and Q_6 (point X) which acts as a complementary symmetry amplifier. The output at this point is proportional to the differential input signal. The output is now amplified by the second stage consisting of transistor Q_{16} and Q_{17} in Darlington connection.

The output of common-collector-amplifier formed by Q_{16} and R_9 drives the CE-amplifier composed of Q_{17}, R_8 and a constant current load Q_{13}. The output of CE-amplifier is a bias source for transistors Q_{18} and Q_{19}. Transistors Q_{12} and Q_{13} form a current mirror and supply current to transistors Q_{17}, Q_{18} and Q_{19}. The network consisting of transistors Q_{18}, Q_{19} and R_{10} is a fixed voltage level shifter shifting the voltage output of Q_{17} by a fixed amount on its way to the output complementary stage formed by Q_{14} and Q_{20}. The level shifter network is designed to bias the output stage in the linear region. The transistors Q_{18} and Q_{19} also separate the bases of Q_{14} and Q_{20} by two diode drops and thus temperature compensate currents in Q_{14} and Q_{20}. Transistor Q_{22} performs two functions. It serves as a buffer between Q_{17} and Q_{20} and also provides a negative feedback to Q_{16}. The final output is taken at the junction of R_6 and R_7. The output complementary pair operates so that depending upon the sign of the output, only one of the transistors Q_{14} or Q_{20} is conducting at any time. With no input signal, both devices are turned off, resulting in a low quiescent current drain in the output stage.

Transistors Q_{15}, Q_{21} and Q_{23} protect the circuit by limiting current to the output complementary stage. If the output (load) current exceeds the safe limit, the voltage drop across R_6 and R_7 increases. This turns on Q_{15} and Q_{21} which in turn makes Q_{23} on. This however shorts out, that is turns off the amplifier Q_{16}–Q_{17}. This reduces the emitter current in Q_{22} and in turn current in Q_{18} and Q_{19}. The reduction in the currents of Q_{18} and Q_{19} lowers the currents in Q_{14} and Q_{20}. The diode-connected transistor Q_{24} is a temperature

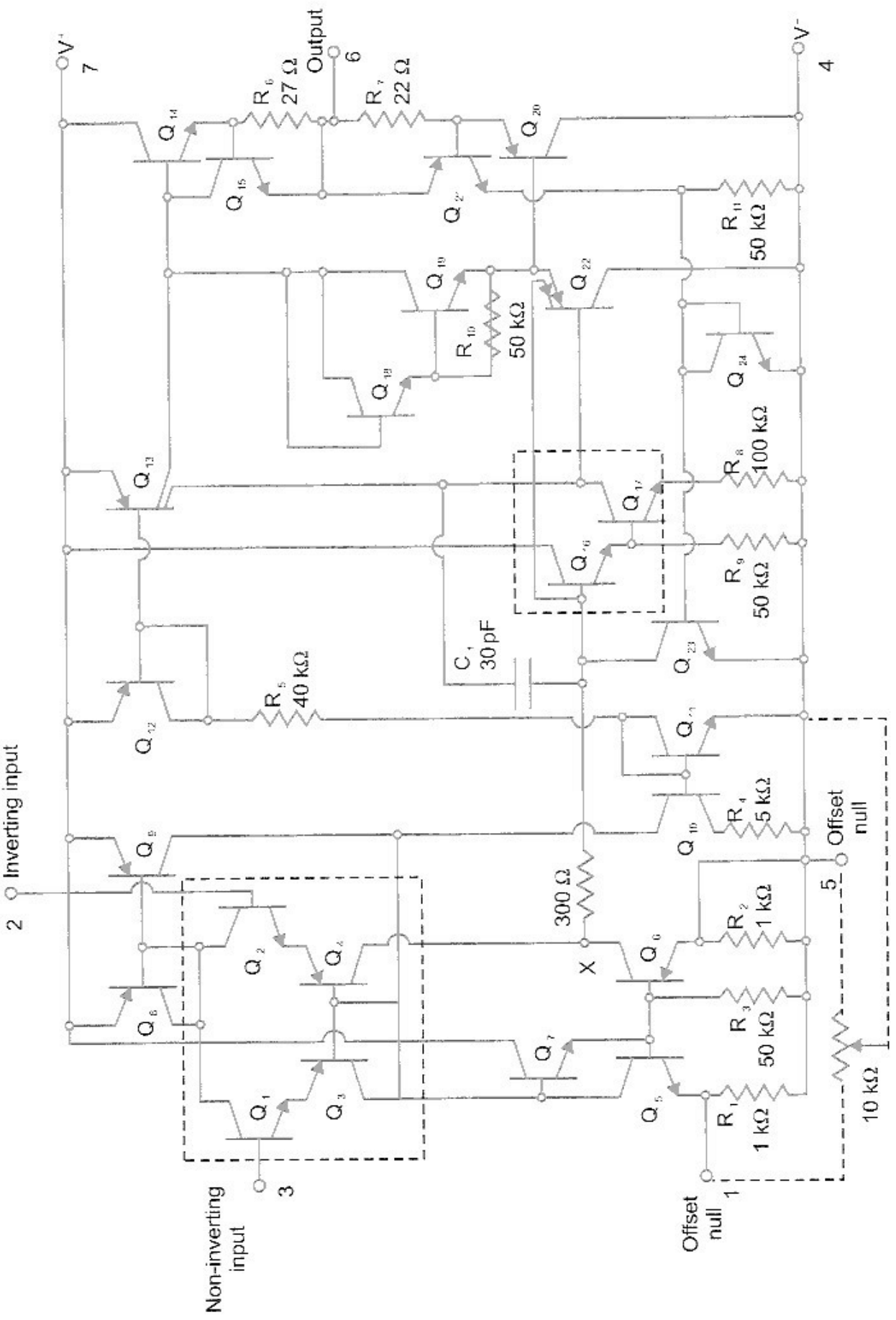

Fig. 2.34 (b) Schematic circuit diagram for 741 op-amp

compensating diode for transistor Q_{23}. Finally the internal 30-pF capacitor provides the high frequency roll-off to stabilize the circuit.

Example 2.18

For the op-amp circuit shown in Fig. 2.35, assume $h_{fe} = 100$, $V_{BE} = 0.7$ V.

(i) Perform the dc analysis. Note that the transistor Q_7 has four times the areas of transistors Q_3 and Q_4.

(ii) Compute the overall voltage gain.

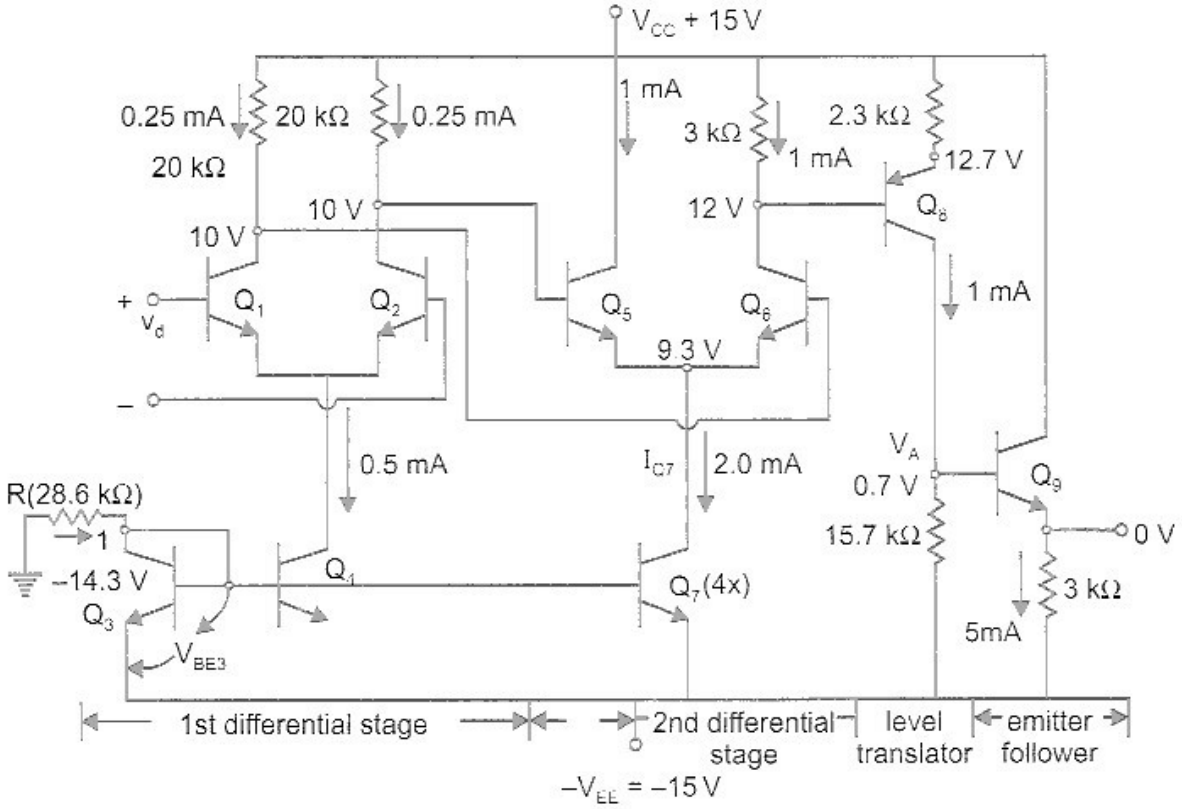

Fig. 2.35 Circuit for Example 2.18

Solution

It can be seen that the circuit has the following four stages:

(i) Dual-input, differential-output

(ii) Dual-input, single-ended output

(iii) Level translator

(iv) Emitter follower.

(i) For **dc analysis**, assume that the input terminals are shorted to ground. The reference current I of the current minor $Q_3 - Q_4$ is obtained as

$$I = \frac{V_{EE} - V_{BE3}}{R} = \frac{15\text{V} - 0.7\text{V}}{28.6\ \text{k}\Omega} = 0.5\ \text{mA}$$

Due to current mirror action,

$$I_{CQ4} = I = 0.5\ \text{mA}$$

and $$I_{CQ1} = I_{CQ2} = I_{CQ4}/2 = 0.25\ \text{mA}$$

Thus, each of Q_1 and Q_2 are biased at 0.25 mA. The collector voltages for Q_1 and Q_2 are

$$V_{CQ1} = V_{CQ2} = V_{CC} - I_{C1}R_{C1} = 15\ \text{V} - 0.25\ \text{mA} \times 20\ \text{k}\Omega = +10\ \text{V}$$

Now, proceeding to the next differential stage, voltage at the emitter of Q_5 and Q_6 will be

$$V_{EQ5} = V_{EQ6} = 10\text{ V} - 0.7\text{ V} = 9.3\text{ V}$$

The differential pair Q_5–Q_6 is biased by the current mirror transistor Q_7. Since the area of Q_7 is 4 times that of Q_3 and Q_4, the transistor Q_7 supplies a current $4 \times 0.5 = 2$ mA.

Thus, collector currents of Q_5 and Q_6 are

$$I_{CQ5} = I_{CQ6} = \frac{I_{Q7}}{2} = 1\text{ mA}$$

Hence, collector voltage of Q_6 is

$$V_{CQ6} = V_{CC} - I_{CQ6}R_{C6} = 15\text{ V} - 1\text{ mA} \times 3\text{ k}\Omega = 12\text{ V}$$

This causes a voltage at the emitter of *pnp* transistor Q_8 at

$$V_{EQ8} = 12.7\text{ V}$$

The emitter current of Q_8 is

$$I_{EQ8} = \frac{15\text{ V} - 12.7\text{ V}}{2.3\text{ k}\Omega} = 1\text{ mA}$$

The voltage V_A at the collector of Q_8 or the base of Q_9 is

$$V_A = -15\text{ V} + 1\text{ mA} \times 15.7\text{ k}\Omega = 0.7\text{ V}$$

Since the emitter of Q_9 will be 0.7 V below the base terminal, the voltage at the output terminal 6 is 0 V as is expected. The emitter current of Q_9 is

$$I_{EQ9} = [0 - (-15\text{V})] / 3\text{ k}\Omega = 5\text{ mA}$$

(ii) **a.c. analysis.** The ac emitter resistance of the transistor Q_1–Q_2 is

$$h_{ie_{(Q_1 - Q_2)}} = \frac{h_{fe}V_T}{|I_C|} = \frac{100 \times 25\text{ mV}}{0.25\text{ mA}} = 10\text{ k}\Omega$$

The ac emitter resistance of transistor Q_5–Q_6 is

$$h_{ie_{(Q_5-Q_6)}} = \frac{100 \times 25\text{ mV}}{1\text{ mA}} = 2.5\text{ k}\Omega$$

Since emitter of (Q_5–Q_6) is at ground potential under ac conditions, the effective load for Q_1–Q_2 is

$$R_{L1} = R_{L2} = 20\text{k}\Omega \,||\, 2.5\text{k}\Omega = 2.2\text{ k}\Omega$$

Voltage gain of the first differential stage is

$$A_{DM1} = \frac{h_{fe}R_{L2}}{h_{ie}} = \frac{100 \times 2.2\text{ k}\Omega}{10\text{ k}\Omega} = 22\text{ k}\Omega$$

Voltage gain of second stage which is differential input, single-ended is

$$A_{DM2} = -\frac{1}{2}\frac{h_{fe}R_{L6}}{h_{ie}}$$

Assuming no loading effect on this stage due to level translator stage,

$$A_{DM2} = -\frac{1}{2} \times \frac{100 \times 3\text{ k}\Omega}{2.5\text{ k}\Omega} = -60\text{ k}\Omega$$

The gain of the level translator stage is

$$A_3 \cong -\frac{R_L}{R_E} = -\frac{15.7\ \text{k}\Omega}{2.3\ \text{k}\Omega} = -6.82\ \text{k}\Omega$$

The last stage is emitter follower, so its voltage gain $A_{V4} \cong 1$

So the overall voltage gain is

$$A_V = (22)\ (-60)\ (-6.82)\ (1) = 9002$$

2.6 FET OPERATIONAL AMPLIFIER

The op-amp circuits discussed so far are bipolar op-amps. Op-amps using field transistors (FETs) in the input stage offer some very significant advantages over bipolar op-amps, especially in areas as input impedance, input bias and offset currents and slewing rate as shown in Table 2.1.

Table 2.1

Parameter	*BJT*	*JFET*	*MOSFET*
Input resistance	kΩ	10^9 Ω (giga-ohms)	10^{12} Ω (tera-ohms)
Input gate current	μA	1 nA	1 pA
Input offset current	20 nA	2 pA	0.5 pA
Slewing rate	1 V/μs	3 V/μs	10 V/μs

FET Differential Amplifier

The circuit of a basic source-coupled differential amplifier using MOSFET is shown in Fig. 2.36. The analysis for finding A_{DM} and A_{CM} is similar to what has been done for BJT differential amplifiers.

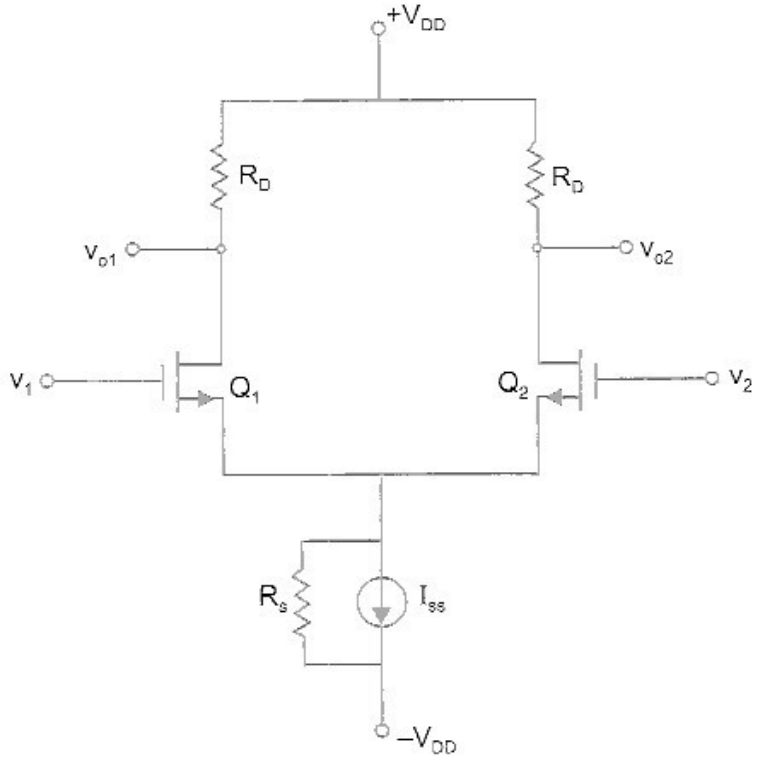

Fig. 2.36 A MOSFET differential amplifier

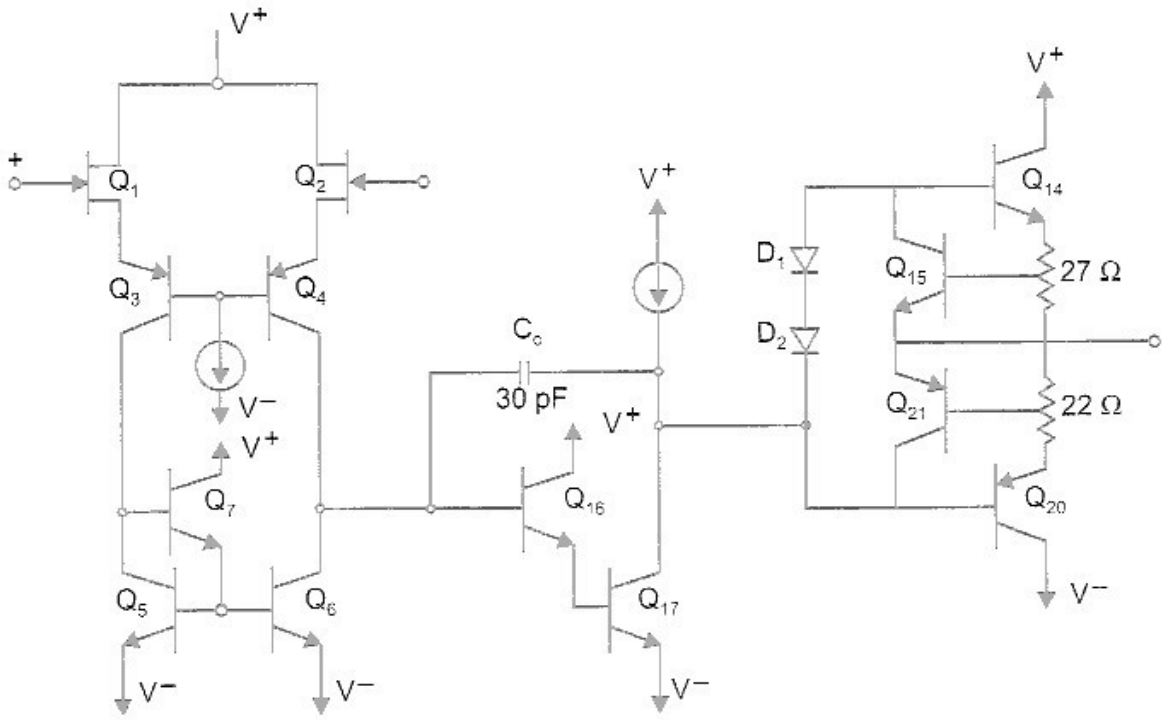

Fig. 2.38 Hybrid JFET-input op-amp LH00 22/42/52 series (National Semiconductor)

MOSFET Op-amps

An interesting example of a monolithic MOSFET op-amp is the CA3130 (RCA) which contains both MOSFETs and bipolar transistors on the same chip. A simplified schematic diagram of this device is shown in Fig. 2.39.

The input stage is a differential amplifier consisting of a pair of p-channel enhancement-mode MOSFETs Q_6 and Q_7. This differential amplifier is biased by a 200 μA MOSFET current source, and it drives a current mirror active load using Q_9 and Q_{10}. Resistors R_5 and R_6 (1 kΩ) in the active load circuit are used together with an externally connected potentiometer (across pins 1 and 5) for offset voltage nulling. The quiescent voltage drop across these resistors in 100 μA × 1 kΩ = 100 mV, so that a ±100 mV offset adjustment range is available. Diodes D_5 and D_8 are connected between the input terminal to protect the thin gate oxide of the input MOSFETs against excessive voltage spikes and static electricity discharge, which could cause breakdown of the oxide layer and result in irreversible damage to the transistors. The voltage gain of this first stage is only about 5, due to low transfer conductance of the MOSFETs.

The second stage consists of a bipolar transistor Q_{11} connected as a common-emitter amplifier, with a 200 μA MOSFET current source serving as the active load. As a result of the high dynamic impedance seen looking into the MOSFET output stage, the voltage gain of the second stage is very large (≈6000). The output stage is a complementary pair of MOSFETs (CMOS) with Q_8 being the PMOS and Q_{12} being the NMOS transistor. The use of CMOS pair in the output stage provides significantly low drainage of current from the power supply.

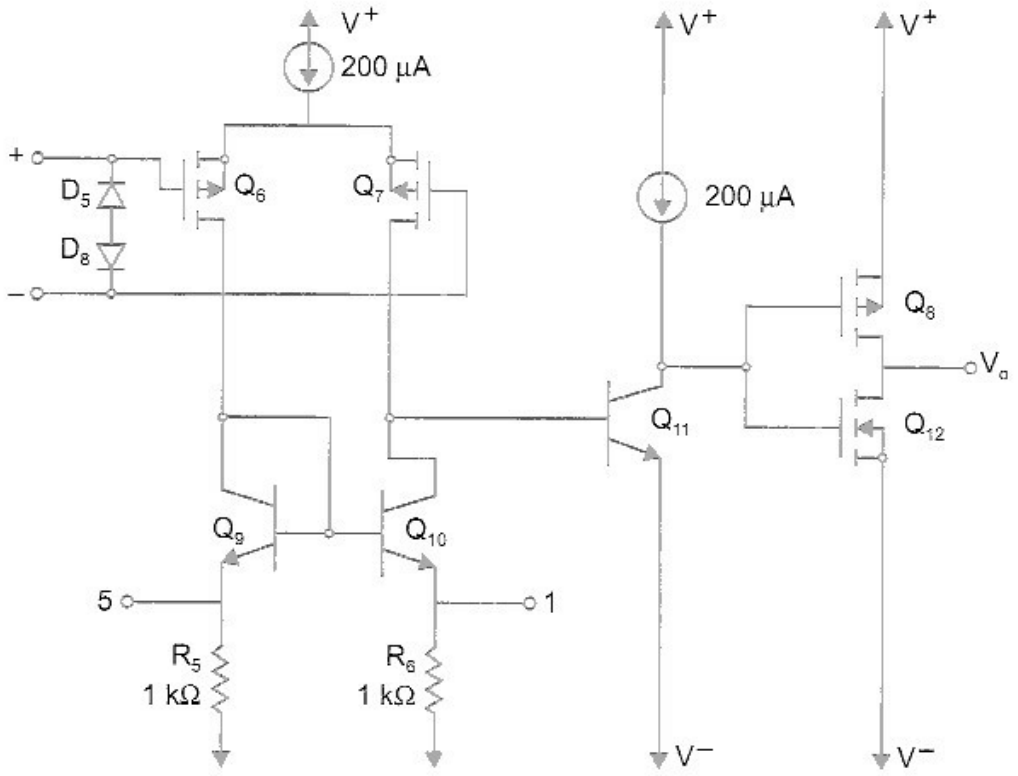

Fig. 2.39 MOSFET-input CMOS output op-amp: CH3130 (RCA Corporation) a simplified schematic diagram

SUMMARY

1. An op-amp is available in three types of IC packages: metal can, dual-in-line and flat pack.
2. There are five basic terminals: two input terminals, one output terminal and two supply terminals.
3. In open loop mode, the output of the op-amp is at positive or negative saturation level. It does not operate linearly in this mode.
4. Negative feedback stabilizes the gain. Two feedback connections used are: inverting amplifier and non-inverting amplifier.
5. A special case of non-inverting amplifier is the voltage follower.
6. A differential amplifier amplifies the difference between two input signals.
7. An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.
8. For proper operation of the differential amplifier, matched components must be used. The diff-amp can be biased by using emitter bias (a combination of R_E and V_{EE}), a constant current bias or a current mirror.
9. A current mirror can be used as an active load because it has high ac resistance.
10. MOSFET op-amps offer very high input resistance (10^{12} Ω), low input current (~ 1 pA) and high slewing rate (~10 V/μs).

REVIEW QUESTIONS

2.1. What is an op-amp?
2.2. What are the different linear IC packages?
2.3. A 741 op-amp is available in a 14-pin dual-in-line package. What is the terminal number for (i) inverting input (ii) non-inverting input (iii) output?
2.4. Explain with figures how two supply voltages V^+ and V^- are obtained from a single supply.
2.5. List six characteristics of an ideal op-amp.
2.6. Explain the meaning of open loop and closed loop operation of an op-amp.
2.7. Name the type of the feedback used if an external component is connected between the output terminal and the inverting input.
2.8. What is the input impedance of a non-inverting op-amp amplifier?
2.9. If the open loop gain of an op-amp is very large, does the closed loop gain depend upon the external components or the op-amp?
2.10. What is a practical op-amp? Draw its equivalent circuit.
2.11. Define common mode rejection ratio.
2.12. Explain why CMRR $\rightarrow \infty$ for an emitter coupled differential amplifier when $R_E \rightarrow \infty$.
2.13. Why is R_E replaced by a constant current bias circuit in a diff-amp?
2.14. List and explain the function of all the basic building blocks of an op-amp.
2.15. Explain methods for increasing the input resistance of an op-amp.
2.16. Explain the difference between constant current bias and current mirror.
2.17. Explain why active load is used?
2.18. What is a V_{BE} multiplier?
2.19. What is cross-over distortion and how it is eliminated?
2.20. Why is cascode configuration used in an op-amp?
2.21. Why are FET op-amps better than BJT op-amps?
2.22. What is meant by a BIMOS or BIFET amplifier?

PROBLEMS

2.1. In an op-amp of Fig. 2.4 (a), $v_2 = 0$. What must be the voltage at v_1 to give an output of 5 V if $A_{OL} = 50000$?
2.2. Design an inverting amplifier with a gain of –5 and an input resistance of 10 kΩ.
2.3. Design a non-inverting amplifier with a gain of 10.
2.4. For the circuit shown in Fig. P. 2.4, calculate the range of gain and input impedance.
2.5. Calculate the exact closed loop gain of the inverting amplifier of Fig. 2.5 (b) if $A_{OL} = 200{,}000$, $R_i = 2$ MΩ and $R_o = 75\Omega$.

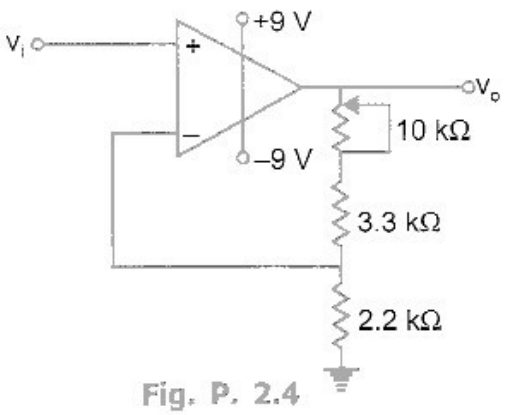

Fig. P. 2.4

2.6. For the circuit shown in Fig. P. 2.6, calculate the expression of v_o/v_i.

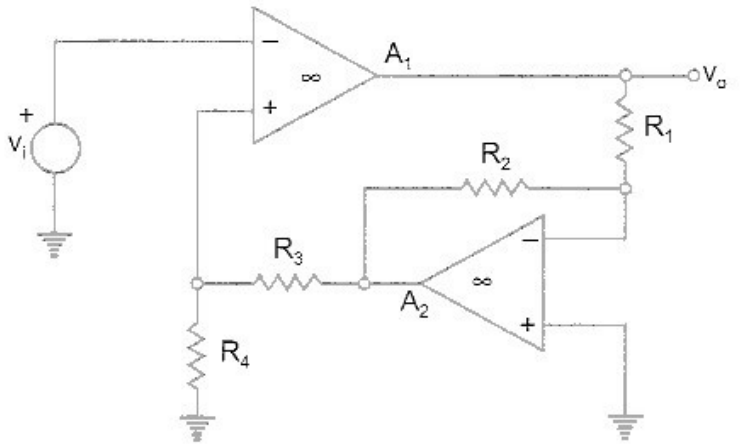

Fig. P. 2.6

2.7. In the circuit of Fig. P. 2.7 if $R_i = \infty$ show that the output admittance Y_{of} is given by

$$Y_{of} = \frac{1}{R_o}\left(1 - A_{OL}\frac{R}{R+R'}\right) + \frac{1}{R+R'}$$

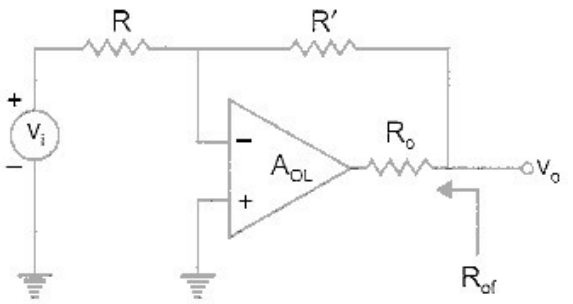

Fig. P. 2.7

2.8. Show that the input impedance for the non-inverting amplifier of Fig. P. 2.8 is

$$R_{if} = R_i\left(1 + \frac{Z_1}{Z_1 + Z_f}\,.\,A_V\right)$$

where R_i the input resistance of op-amp is large and $R_o = 0$ and A_v is the gain without feedback.

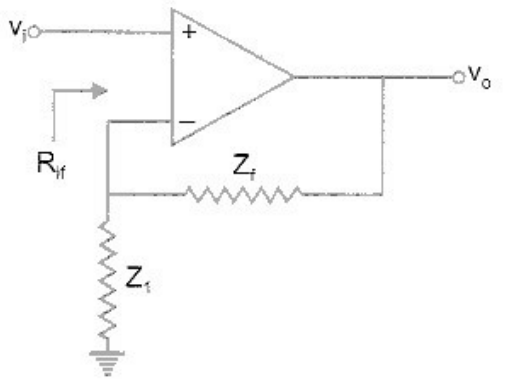

Fig. P. 2.8

2.9. Refer to Fig. P. 2.9

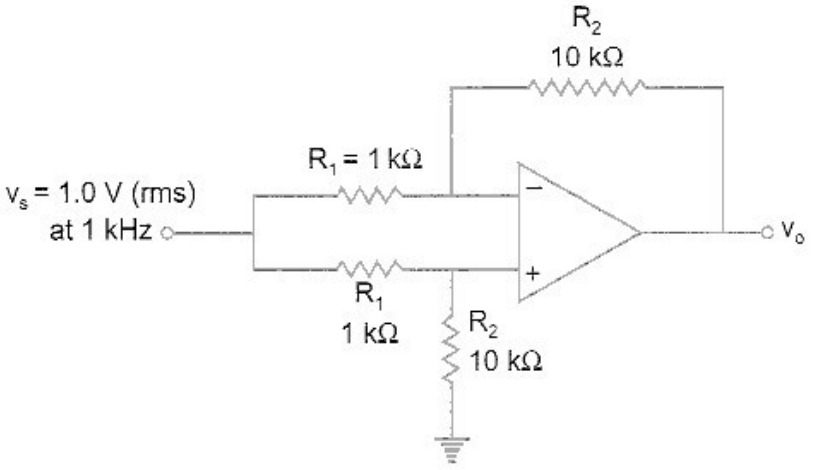

Fig. P. 2.9

(a) Find v_o if CMRR = 100 dB at 1kHz.
(b) Find v_o resulting from 1% mismatches between the two R_1 resistors.
(c) Find v_o resulting from 1% mismatch between two R_2 resistors.

2.10. Derive the expression for the output voltage v_o for the circuit shown in Fig. P. 2.10.

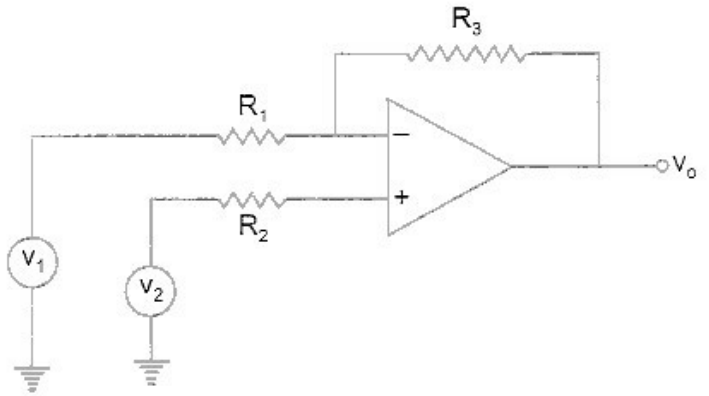

Fig. P. 2.10

2.11. Calculate the output voltage of the circuit in Fig. P. 2.11 if the input signal is a 5.5 mA current.

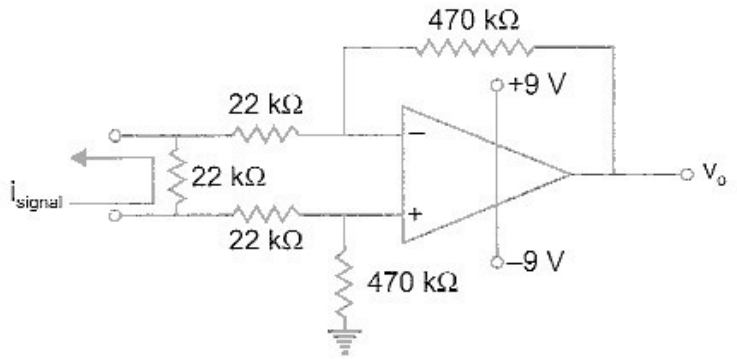

Fig. P. 2.11

2.12. What is the voltage at point A and B for the circuit shown in Fig. P. 2.12 if v_1 = 5 V and v_2 = 5.1 V?

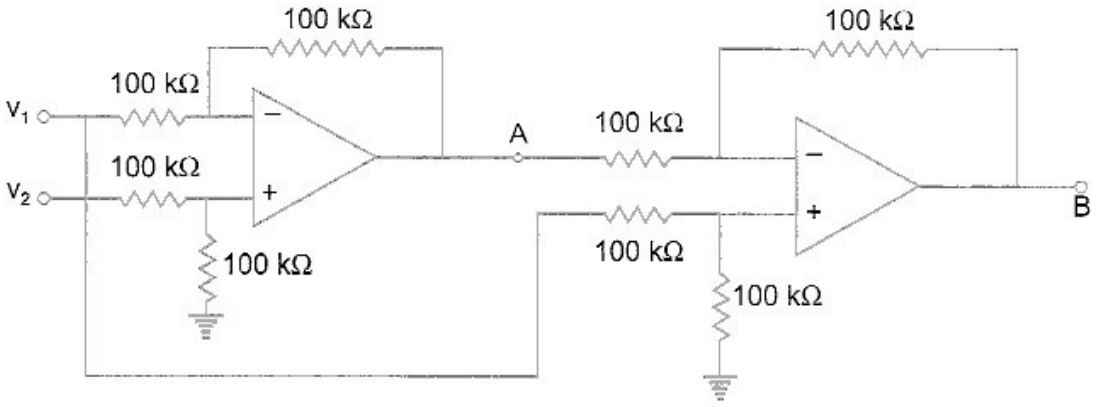

Fig. P. 2.12

2.13. For op-amp, CMRR = 10^5 and differential gain $A_{DM} = 10^5$. Calculate the common mode gain A_{CM} of the op-amp.

2.14. The CMRR of an op-amp is 10^4. Two sets of signals are applied to it. First set is V_1 = + 20 μV and V_2 = – 20 μV and second set is V_1 = 540 μV and V_2 = 500 μV. Calculate the per cent difference in output voltage for the two sets of signals.

2.15. For the current mirror shown in Fig. P. 2.15, determine R so that I_o = 100 μA.

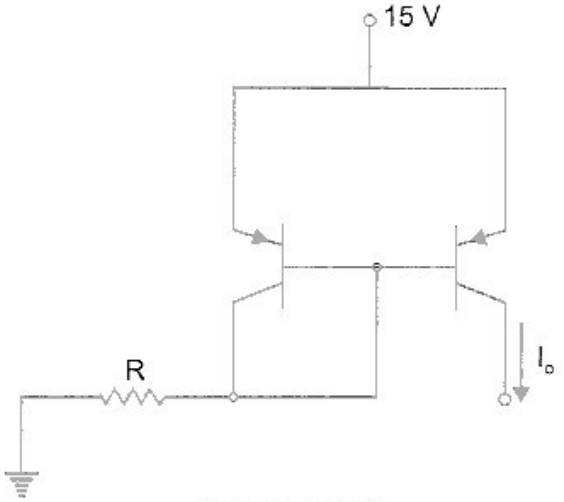

Fig. P. 2.15

2.16. In the circuit of Fig. P. 2.16, I_R = 50 μA, what is the ratio R_1/R_2 needed for I_o = 100 μA?

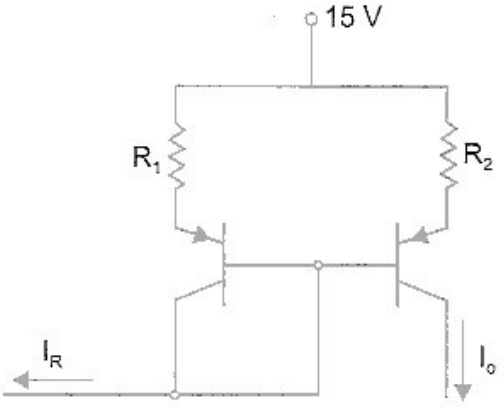

Fig. P. 2.16

2.17. Design a current source for generating I_o = 25 μA. Assume : V_{CC} = 15 V, β = 100.

2.18. For a modified current mirror shown in Fig. P. 2.18, calculate (i) the current through the collector resistor R_C and (ii) the collector current in each transistor. Assume V_{BE} = 0.7 V and β = 100.

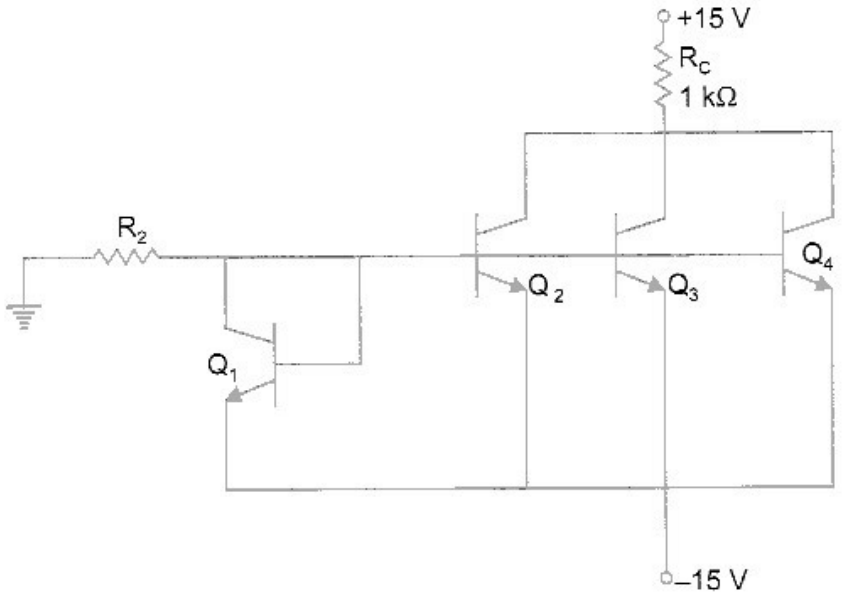

Fig. P. 2.18

2.19. For the circuit of Fig. P. 2.19, show that

$$V_o = (V_Z + V_{BE})\,(1 + R_1/R_2).$$

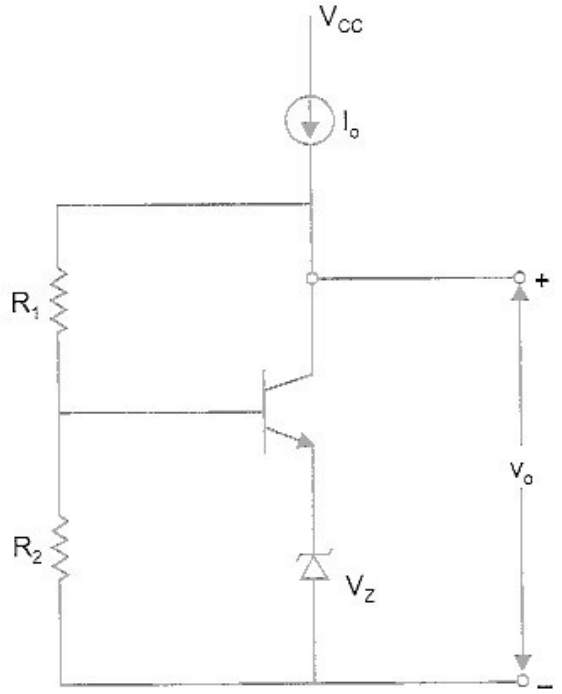

Fig. P. 2.19

2.20. For the simple op-amp shown in Fig. P. 2.20, all *npn* transistors have $\beta = 200$ and all *pnp* transistors have $\beta = 50$. Verify that $v_o = 0$ for $v_1 = v_2 = 0$. The current sources shown are realized by *pnp* current sources.

2.21. For the cascaded differential amplifier shown in Fig. P. 2.21 (i) perform the dc analysis and (ii) calculate the overall voltage gain. Assume $h_{fe} = 100$ $V_{BE} = V_D = 0.7$ V.

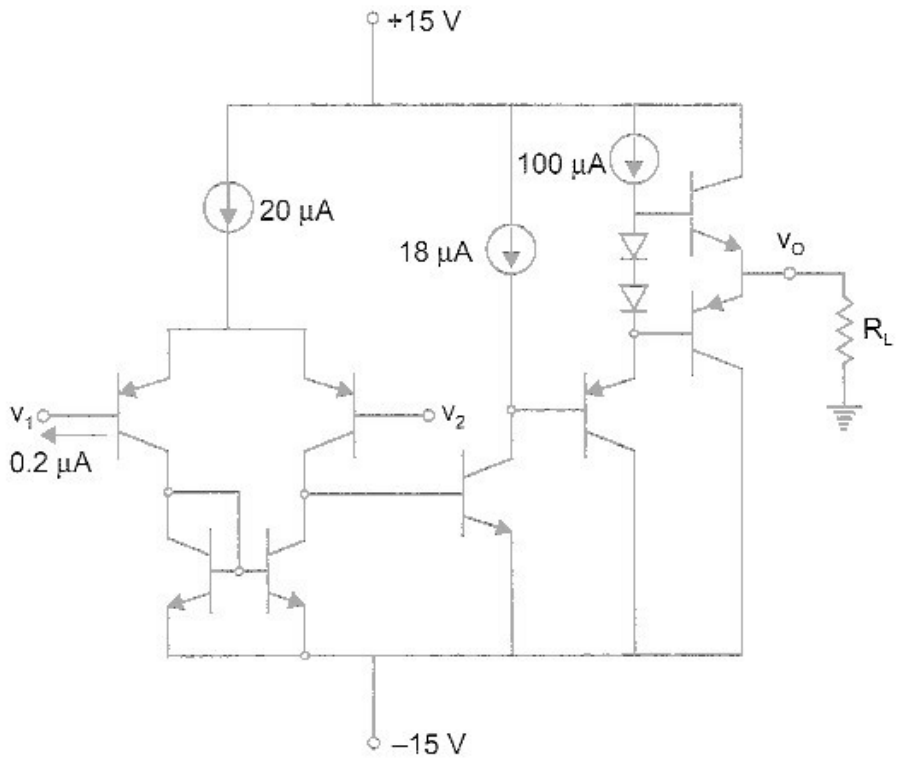

Fig. P. 2.20

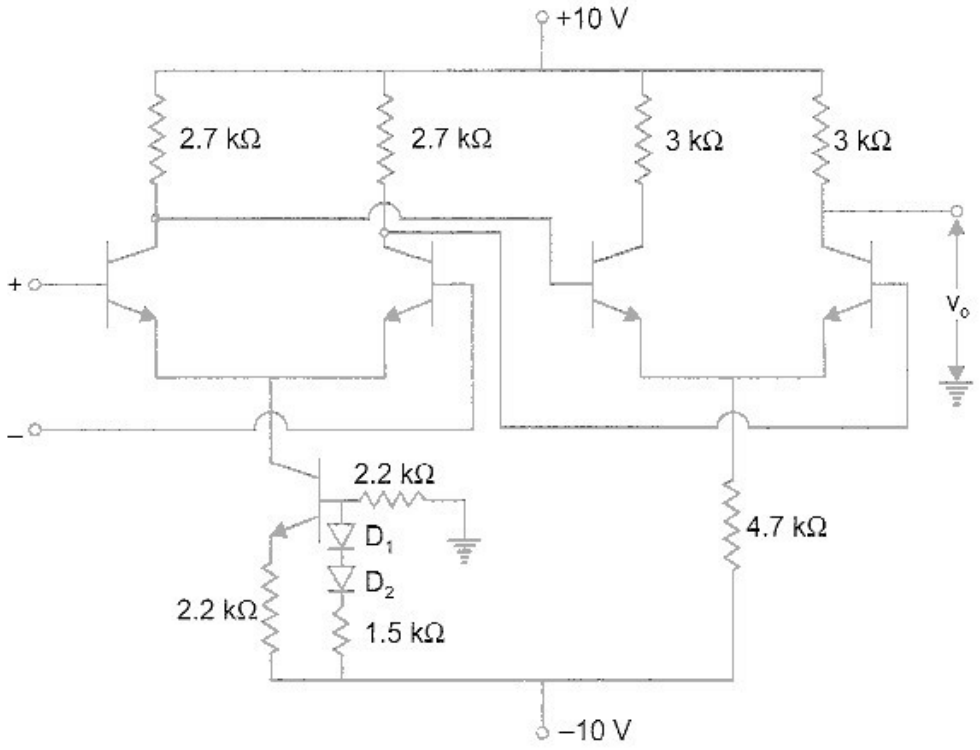

Fig. P. 2.21

EXPERIMENT

To construct and verify experimentally the theoretical closed loop voltage gain using 741 op-amp for the following:

(i) Inverting amplifier
(ii) Non-inverting amplifier
(iii) Voltage follower

PROCEDURE

(1) Connect the op-amp as an inverting amplifier as shown in Fig. E. 2.1(a).

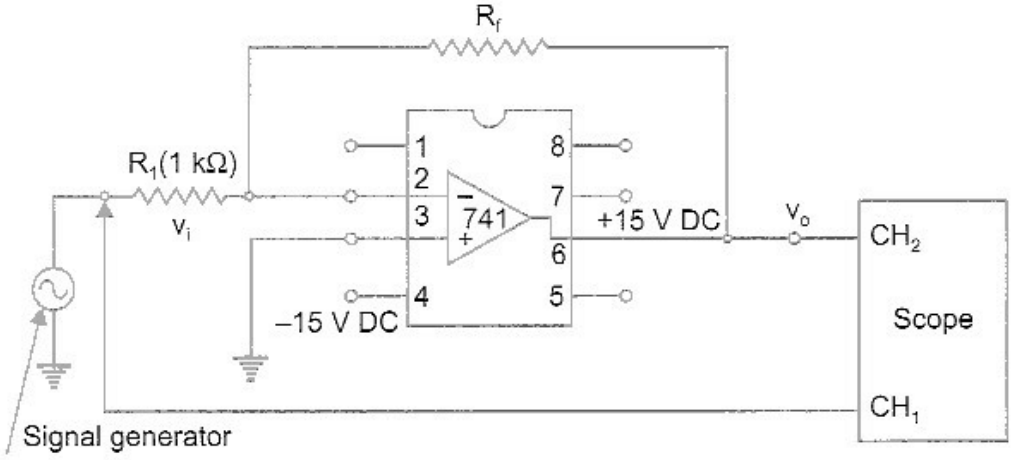

Fig. E. 2.1 (a) Inverting amplifier

(2) Connect a dual channel scope to simultaneously view v_o and v_i. Adjust the signal generator to give 200 mV peak to peak sine wave at 100 Hz. Then measure and record the peak value of v_o for R_f: 1 kΩ, 10 kΩ, 33 kΩ and 100 kΩ. Note the phase of v_o with respect to v_i.

(3) Calculate the theoretical closed loop gain = R_f/R_i for each value of R_f and compare it with the experimental value of v_o/v_i.

(4) Now connect the op-amp as a non-inverting amplifier as shown in Fig. E. 2.1 (b).

(5) Repeat step 2.

(6) Calculate the theoretical gain = $1 + R_f/R_1$ for each value of R_f and compare it with the experimental value of v_o/v_i.

(7) Next make a voltage follower circuit as shown in Fig. E. 2.1. (c).

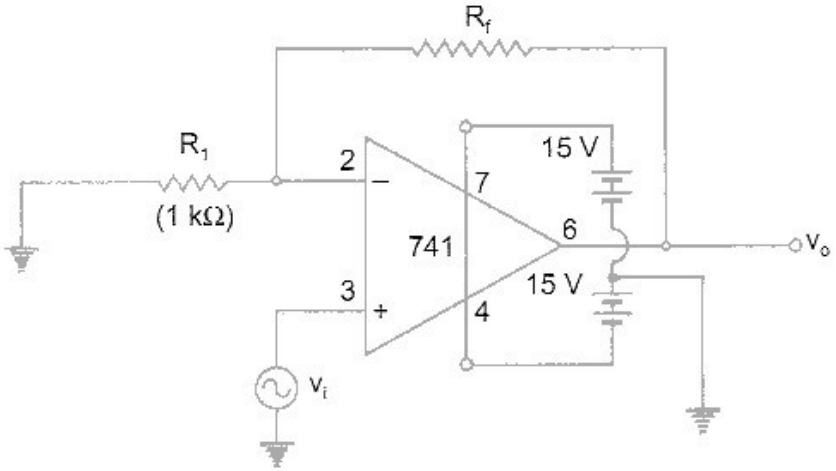

Fig. E. 2.1 (b) Non-inverting amplifier

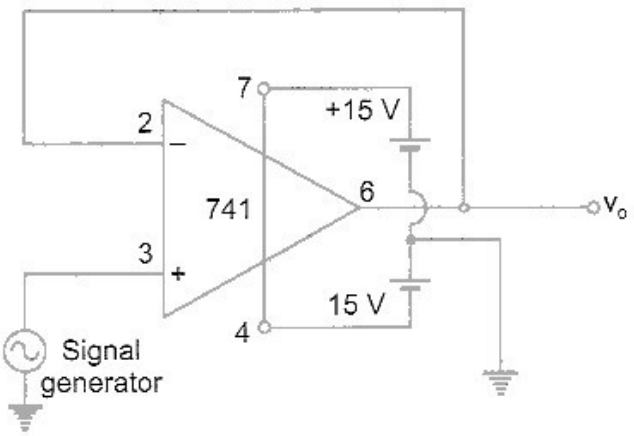

Fig. E. 2.1 (c) Voltage follower

(8) Measure and record the output voltage v_o for different input settings: 2 V peak at 100 Hz, 1 V peak at 500 Hz and 5 V peak at 1 kHz. Note the phase of v_o with respect to v_i in each case.

(9) Verify that the voltage gain of the voltage follower is always equal to 1.

COMPUTER ANALYSIS

Program 2.1

Inverting Op-amp Amplifier

Figure C. 2.1 (a) shows an inverting op-amp amplifier with various terminals numbered for writing the PSPICE program. The PSPICE description is provided in program 2.1 listing. For circuit values of R_1 = 1 kΩ, R_f = 10 kΩ, the gain of the inverting amplifier is

$$A_V = -\frac{R_f}{R_1} = -10$$

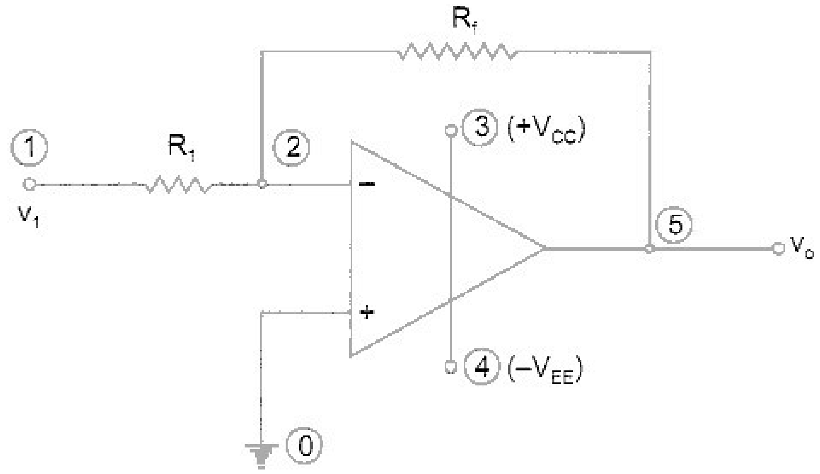

Fig. C. 2.1 (a) Circuit for program 2.1

D.C. Analysis

For input V_1 = 1 V, the output voltage V_o should V_o = − 10 (1 V) = − 10 V.
From the result file, it can be seen that the output V_o at node 5 is − 9.998 V which gives an error or 0.02% only.

Transient Analysis

A sine wave signal of amplitude 0.1 V and frequency 1 kHz is applied at the input terminal. It can be seen from Fig. C. 2.1 (b) that the output is a sine wave of amplitude 1 V, 1 kHz. The output waveform is 180° out of the phase with the input waveform as expected.

Program 2.1: Listing

Inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis

```
  * * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
    R1 1 2 IK
    RF 2 5 10K
*   Op Amp Analysis
    X1 0 2 3 4 5 µA 741
    . LIB EVAL. LIB
*   Power Supplies
    VCC 3 0 DC 12V
    VEE 0 4 DC 12V
```

```
*   Input Signal  Source
    V1 1 0 DC 1V SIN(0  0.1V  1KHZ)
*   Output
    .DC V1  1  1  1
    .TRAN . 5µs 5ms 0ms .01 ms
    .PROBE
    .PRINT DC V(5) V(1)
    END
```

```
  * * * * DC Transfer Curves                                        Temperature = 27.000 DEG C
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
    V1              V(5)            V(1)
    1.000E+00       -9.998E+00      1.000E+00
```

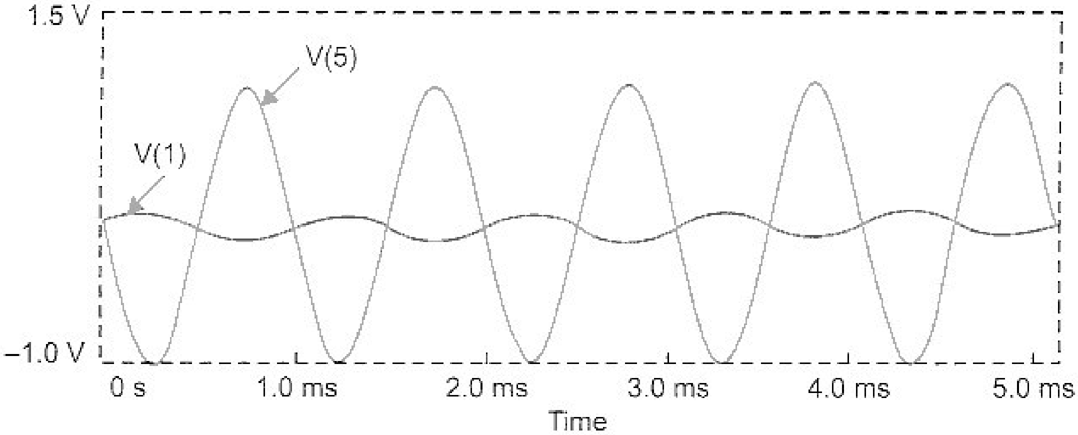

Fig. C. 2.1 (b) Inverting amplifier: Transient analysis (output voltage vs time)

Program 2.2

Non-inverting Op-amp Amplifier

The circuit of a non-inverting op-amp amplifier for writing the PSPICE program is shown in Fig. C. 2.2 (a).

For the circuit values, R_1 = 1 kΩ and R_f = 9 kΩ, the voltage gain is

$$A_V = 1 + \frac{R_f}{R_1} = 1 + \frac{9k\Omega}{1k\Omega} = +10 = 10$$

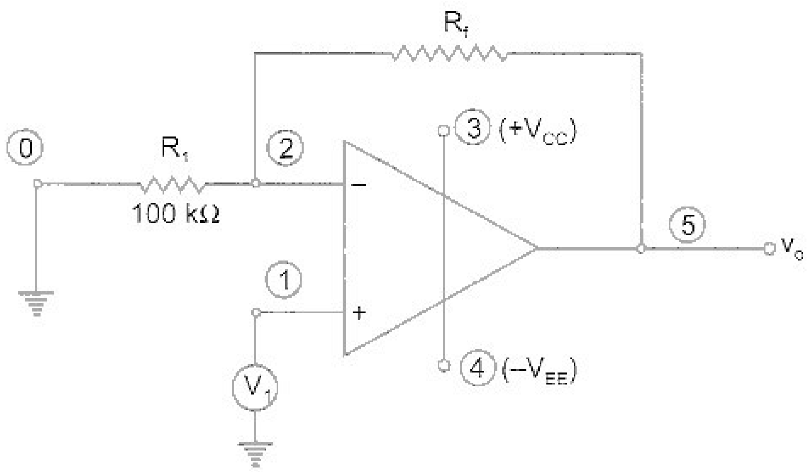

Fig. C. 2.2 (a) Circuit for program 2.2

D.C. Analysis

For input voltage V_1 = 1 V, the output voltage at node 5, V(5) = 10 V

Transient Analysis

For input voltage source of amplitude 0.1 V and frequency 1 kHz, the output voltage has an amplitude 1 V at 1 kHz as shown in Fig. C. 2.2 (b). It may be noted that there is no phase shift for a non-inverting amplifier.

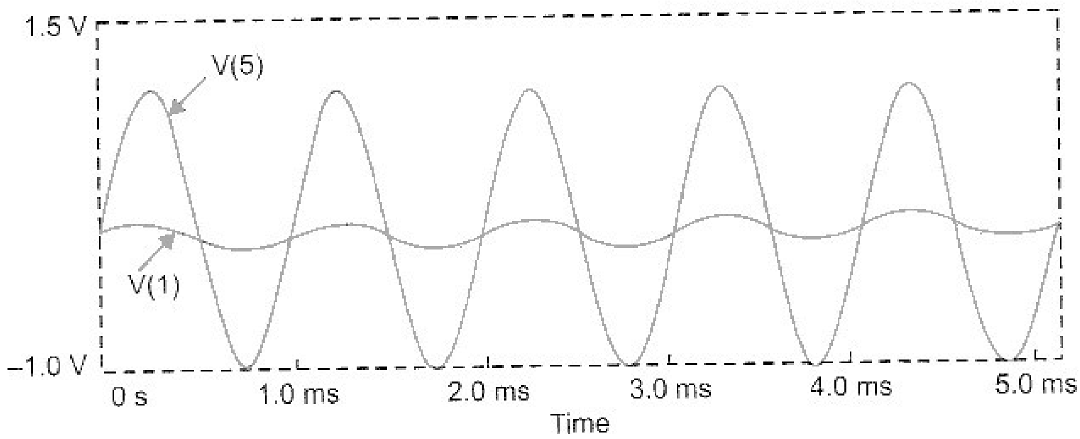

Fig. C. 2.2 (b) Non-inverting amplifier: Transient analysis (Output voltage vs time)

Program 2.2 Listing

Non-inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis

```
  * * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

* * *
    R1  0  2  IK
    RF  2  5  9K
*   Op Amp Analysis
    X1  1  2  3  4  5  µA741
    . LIB  EVAL.LIB
*   Power Supplies
    VCC  3  0  DC  12V
    VEE  0  4  DC  12V
*   Input Signal  Source
    V1  1  0  DC  1V  SIN (0  0.1V  1 KHZ)
*   Output
    .DC  V1  1  1  1
    .TRAN . 5µs 5ms 0ms 0.01 ms
    .PRINT  DC  V(5)  V(1)
    .PROBE
  * * * *      DC Transfer Curves                 Temperature = 27.000 DEG C
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

* * *
          V1                          V(5)                        V(1)
      1.000E+00                   1.000E+01                   1.000E+00
```

Program 2.3 Voltage Follower

The circuit diagram of a voltage follower and its PSPICE description are shown in Fig. C. 2.3 (a) and program 2.3 listing respectively.

The voltage gain for both d.c. and a.c. input is found to be unity and without change in phase as expected. The transient analysis is shown in Fig. C 2.3 (b). It may be noted that waveforms at node 1 and 5 overlap each other indistinguishably.

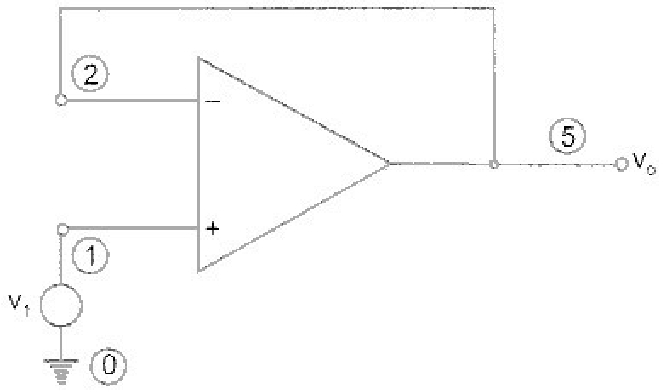

Fig. C. 2.3 (a) Circuit for program 2.3

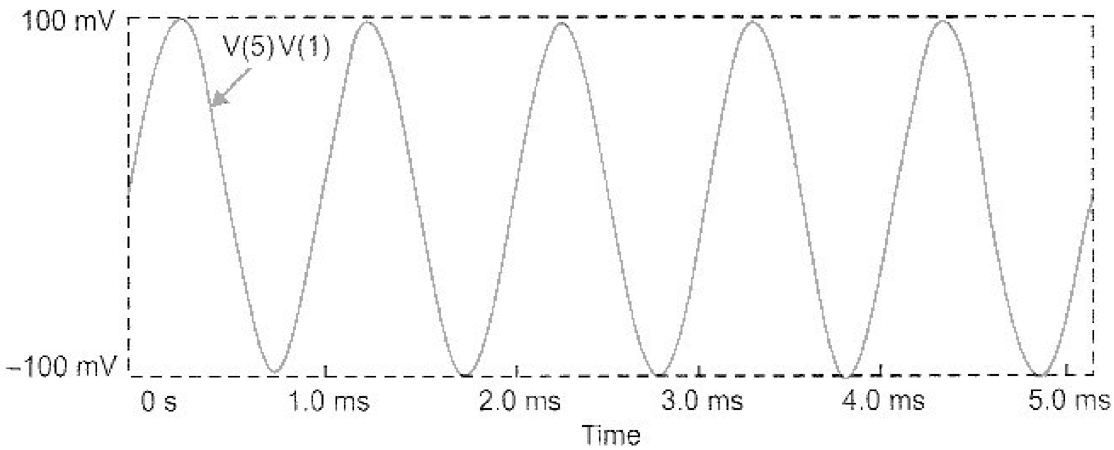

Fig. C. 2.3 (b) Transient response of voltage follower

Program 2.3 Listing

```
* Voltage Follower
  * * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

* * *
   RF  2  5  IM
*  Op Amp Analysis
   X1  1  2  3  4  5  µA741
   . LIB  EVAL.LIB
*  Power Supplies
   VCC  3  0  DC  12V
   VEE  0  4  DC  12V
*  Input Signal  Source
   V1  1  0  DC  2V  SIN(0 0.1V 1KHZ)
*  Output
   * DC  V1  2  2  2
   * TRAN 0.5µs 5ms 0ms 0.01 ms
   * PRINT  DC  V(5)  V(1)
   * PROBE
 * * * *    DC Transfer Curves              Temperature = 27.000 DEG C
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

* * *
       V1                       V(5)                      V(1)
   2.000E+00               2.000E+01                 2.000E + 00
```