$$v_{o1} = V_{CC} - \alpha_F I_Q R_C$$

and $$v_{o2} = V_{CC}$$

By proper choice of R_C, v_{o1} can be made very small.

2. For $v_d < -4\ V_T$, $i_{C1} = 0$ and $i_{C2} = \alpha_F I_Q$. Hence $v_{o1} = V_{CC}$ and V_{o2} is negligible. Thus, for $4V_T < v_d < -4V_T$, we can say that a differential amplifier can be made to function as a switch.
3. The differential amplifier functions as a very good limiter for $v_d > \pm 4\ V_T$.
4. DA can function as an automatic gain control (AGC) by varying I_Q.
5. Between the values $-2V_T \le v_d \le 2V_T$, DA functions as a linear amplifier.

2.4.3 Low Frequency Small Signal Analysis of Differential Amplifier

An ideal dual-input balanced-output differential amplifier as shown in Fig. 2.11 (a), should amplify only the differential signal at the two inputs and reject the signal common to these inputs. As transistors Q_1 and Q_2 are a matched pair of transistors, thus any unwanted signal, such as noise or hum pick up which is common to both the inputs would get rejected. However in a practical case transistors Q_1 and Q_2 are not equally matched and output does appear even when same voltage is applied to the two input terminals. In this section, we will discuss how to compute the small signal differential mode gain, A_{DM} and common-mode gain A_{CM}. These expressions help in finding the figure of merit CMRR of the differential amplifier and hence the ways to improve it.

The a.c. analysis of the differential amplifier can be performed either by using hybrid-π model or h-parameter model. Both the approaches have been dealt with.

Differential-mode Gain, A_{DM}

In Fig. 2.11 (a) for $v_1 = v_2$, the current I_Q divides equally into the two transistors Q_1 and Q_2 because of the symmetry of the circuit. However, if v_1 is now increased by an incremental voltage (small signal) $v_d/2$ and v_2 is decreased by $v_d/2$, it can be seen that the differential amplifier is being fed by differential small signal v_d. The common mode small signal is naturally zero. The collector current i_{C1} will now increase by an incremental current i_c and i_{C2} will decrease by an equal amount. The sum of total currents in transistors Q_1 and Q_2 however remains constant as constrained by the constant current I_Q. As there is no change of current through R_E, the voltage V_E at the common emitter point 'E' remains constant. Thus, for small signal analysis, the common emitter point 'E' can be considered to be at ground potential. Figure 2.13 (a) shows the small signal equivalent circuit of the differential amplifier under the differential input signal conditions described above. It may be noted that for differential amplifier to behave as a linear amplifier, the differential signal $v_d \le 2V_T$ (that is, v_d should be smaller than about 50 mV) as discussed in the transfer characteristics (section 2.4.2).

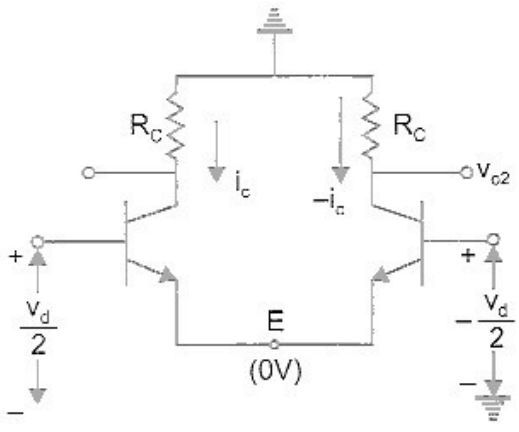


Fig. 2.13 (a) Differential amplifier with differential input signal v_d

Analysis

(i) Using Hybrid-π Model

Since the performance of two sides of the differential amplifier is identical, we need to analyze only one side of the differential amplifier called differential-half circuit. Figure 2.13 (b) shows a single stage CE transistor amplifier fed by a small signal voltage $v_d/2$ and it's a.c. equivalent circuit using hybrid-π model is shown in Fig. 2.13 (c).

From Fig. 2.13 (c),

$$\frac{v_{o1}}{v_d/2} = -g_m R_C$$

or
$$\frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C \tag{2.48}$$

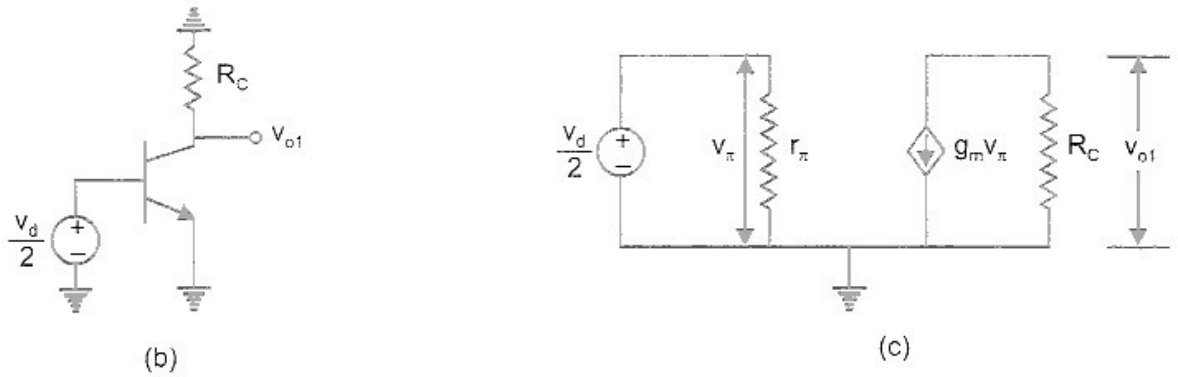


Fig. 2.13 (b) Differential mode half circuit (c) ac-equivalent circuit using hybrid-π model

Similarly, it can be seen that

$$\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C \tag{2.49}$$

The output voltage signal of a differential amplifier can be taken either differentially (i.e. between the two collectors) or single-ended (i.e. between one collector and ground). If the output is taken differentially, then the differential-mode gain, A_{DM} is given by

$$A_{DM} = \frac{v_{o1} - v_{o2}}{v_d} = -g_m R_C \text{ (differential-input, differential-output)} \tag{2.50}$$

On the other hand, if output is single-ended, (say between collector of transistor Q_1 and ground), then the differential-mode gain A_{DM} is given by

$$A_{DM} = \frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C \text{ (differential-input, single-ended output)} \tag{2.51(a)}$$

and
$$\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C \tag{2.51(b)}$$

In the above analysis, we have not included the output resistance r_o of the transistor. If r_o is included, Eq. (2.50) will modify to

$$A_{DM} = -g_m \ (R_C \parallel r_o)..$$

(ii) Using 'h' Parameters

The a.c. equivalent circuit for Fig. 2.13 (b) using approximate h-parameter model is shown in Fig. 2.13 (d).

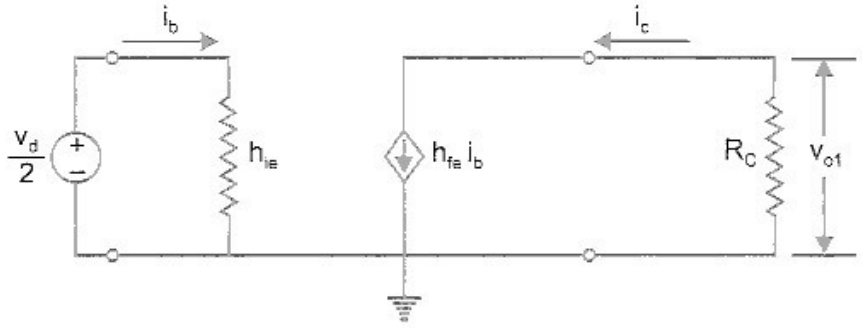


Fig. 2.13 (d) Small signal equivalent circuit of differential half circuit using h-parameter model

From Fig. 2.13 (d),

$$v_{o1} = -i_c R_C = -h_{fe}\, i_b\, R_C$$

and $$\frac{v_d}{2} = i_b h_{ie}$$

Therefore, differential mode gain, A_{DM} is given by

$$A_{DM} = \frac{v_{o1}}{v_d} = -\frac{1}{2}\frac{h_{fe}}{h_{ie}} R_C \text{ (Single-ended output)} \qquad (2.52\ (a))$$

Similarly, we may write

$$A_{DM} = \frac{v_{o2}}{v_d} = \frac{1}{2}\frac{h_{fe} R_C}{h_{ie}} \qquad \text{(Single-ended output)} \qquad (2.52\ (b))$$

If the output is taken differentially between the two collectors, then

$$A_{DM} = \frac{v_{o1} - v_{o2}}{v_d} = -\frac{h_{fe} R_C}{h_{ie}} \qquad \text{(differential-output)} \qquad (2.52\ (c))$$

In the above analysis, the source resistance R_s has not been taken into account.

Common-mode gain, A_{CM}

Now, consider the case when v_1 and v_2 both are increased by an incremental voltage v_c. The differential signal v_d now is zero and common-mode signal is v_c. Both the collector currents i_{C1} and i_{C2} will increase by an incremental current i_c. The current through R_E now increases by $2i_c$. The voltage, V_E at emitter node is now increased by $2i_c R_E$ and no longer constant. In order to draw the common mode half circuit, replace resistance R_E by $2R_E$ as shown in Fig. 2.14 (a). The common-mode gain, A_{CM} is calculated from the small-signal hybrid-π equivalent model shown in Fig. 2.14 (b). It can be seen,

$$A_{CM} = \frac{v_{o1}}{v_c} = \frac{v_{o2}}{v_c} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0)R_E} \qquad (2.53\ (a))$$

For $\beta_0 >> 1$,

β_0 is the small signal CE current gain and is same as h_{fe}.

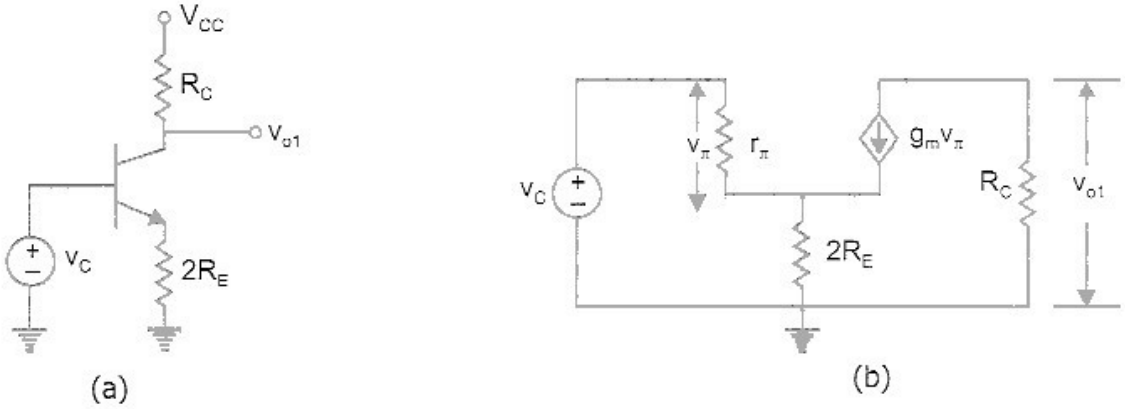


Fig. 2.14 (a) Common-mode half circuit (b) ac equivalent circuit using hybrid-π model

$$A_{CM} = \frac{-g_m R_C}{1+2g_m R_E} \cong -\frac{R_C}{2R_E} \qquad (2.53\ (b))$$

It can be seen that, if the output is taken differentially, then the output voltage $v_{01} - v_{02}$ will be zero and the common-mode gain will be zero. In this analysis, we have assumed that the circuit is perfectly symmetrical. However, in practical circuits, it will not be so, and the differential output voltage will not be exactly zero. If the output is taken single ended, the common-mode gain will be finite and given by Eqs. (2.53 (a)) and (2.53 (b)).

The common mode gain, A_{CM}, using h-parameter model can be easily computed as

$$A_{CM} = \frac{v_{o1}}{v_c} = \frac{-h_{fe} R_C}{h_{ie} + (1+h_{fe})2R_E} \qquad (2.54)$$

The common-mode rejection ratio (CMRR) is defined as

$$\text{CMRR} = \frac{|A_{DM}|}{|A_{CM}|}$$

For differential-input, differential-output, using Eqs. (2.50) and (2.53 b), we obtain

$$\begin{aligned} \text{CMRR} &\cong \frac{g_m R_C (1+2g_m R_E)}{g_m R_C} \\ &= 1 + 2g_m R_E \\ &\cong 2\, g_m R_E \end{aligned} \qquad (2.55)$$

Output for Arbitrary Signals

In the previous analysis, we have assumed that either common mode signals (v_c) or a differential mode signals $\left(\frac{v_d}{2}\right)$ are applied to the two input terminals. However, in a practical situation it will not be so. If, say, any arbitrary signals v_1 and v_2 are applied at the inputs of transistors Q_1 and Q_2 in Fig. 2.11(a), then we can represent these signals by the sum and difference of common mode component v_{CM} (= v_c) and differential mode component v_{DM} $\left(= \frac{v_d}{2}\right)$ as

$$v_1 = v_{CM} + v_{DM}$$

and $$v_2 = v_{CM} - v_{DM}$$

such that,

$$v_{DM} = \frac{v_1 - v_2}{2} \qquad (2.56(a))$$

$$v_{CM} = \frac{v_1 + v_2}{2} \qquad (2.56(b))$$

The output voltage v_{o1} and v_{o2} at the output of transistor Q_1 and Q_2 in Fig. 2.11(a) are given by

$$v_{o1} = A_{DM}\, v_{DM} + A_{CM}\, v_{CM} \qquad (2.57(a))$$

and $$v_{o2} = -A_{DM}\, v_{DM} + A_{CM}\, v_{CM} \qquad (2.57(b))$$

Example 2.6

Differential amplifier shown in Fig. 2.11 (a) uses a transistor with $\beta = 200$ and is biased at $I_{CQ} = 100\ \mu A$. Determine the value of R_C and R_E if $|A_{DM}| = 500$ and CMRR = 80 dB.

Solution

Given $I_{CQ} = 100\ \mu A$

We know that $g_m = \frac{I_{CQ}}{V_T} = \frac{100 \times 10^{-6}}{25 \times 10^{-3}}$ ℧ $= 4$ m℧ [for $V_T = 25$ mV]

Using Eq. (2.50),

$$A_{DM} = -g_m R_C \qquad \text{[For differential output]}$$

$$\therefore \quad R_C = -\frac{A_{DM}}{g_m} = \frac{500}{4\,\text{m}\,℧} = 125\ \text{k}\Omega \qquad \textbf{Ans.}$$

As CMRR = 80 dB,

$$\therefore \quad \text{CMRR} = \log^{-1}\left(\frac{80}{20}\right) = 10^4$$

Using Eq. (2.55),

$$\text{CMRR} = 1 + 2\, g_m\, R_E = 1 + 2 \times 4 \times R_E$$

Solving for R_E, we get

$$R_E = 1.25\ \text{M}\Omega \qquad \textbf{Ans.}$$

Example 2.7

In the basic differential amplifier of Fig. 2.11(a), Given: $R_C = 2\ \text{k}\Omega$; $R_E = 4.3\ \text{k}\Omega$, $V_{CC} = |V_{EE}| = 5$ V; $\beta_0 = 200$, $V_{BE} = 0.7$ V.

Determine:

(i) For $V_1 = V_2 = 0$, that is for both the inputs grounded, the values of quiescent currents and voltages, I_{BQ}, I_{CQ}, V_{o1}, V_{o2}, V_{CEQ}.

(ii) A_{DM}, A_{CM} and CMRR.

Solution

(i) For $V_1 = V_2 = 0$, applying KVL for the base emitter loop, we may write,

$$V_{BE} + 2(1 + \beta_0) I_{BQ} R_E - V_{EE} = 0$$

or
$$I_{BQ} = \frac{V_{EE} - V_{BE}}{2(1+\beta_0)R_E} = \frac{5\,\text{V} - 0.7\,\text{V}}{2(1+200)\,4.3\,\text{k}\Omega}$$

$$= .0024\ \text{mA} = 2.4\ \mu\text{A}$$

$\therefore$
$$I_{CQ} = 200 \times I_{BQ} = 0.48\ \text{mA}$$

$$V_{o1} = V_{o2} = 5\,\text{V} - 2\ \text{k}\Omega \times 0.48\ \text{mA} \qquad \text{(due to symmetry)}$$

$$= 5\,\text{V} - .96\,\text{V} = 4.04\,\text{V}$$

$$V_{CEQ} = V_C - V_E$$

$$= V_{o1} - (-V_{BE}) = V_{o1} + V_{BE}$$

$$= 4.04\ \text{V} + 0.7\ \text{V} = 4.74\ \text{V}$$

(ii)
$$g_m = \frac{I_{CQ}}{V_T} = \frac{0.48\,\text{mA}}{25\ \text{mV}} = .0192\ \text{℧} = 19.2\ \text{m℧}$$

$$r_\pi = \frac{\beta_0}{g_m} = \frac{200}{19.2\ \text{m℧}} = 10.4\ \text{k}\Omega$$

Using Eq. (2.50),

$$A_{DM} = -g_m R_C$$

$$= -19.2\ \text{m℧} \times 2\ \text{k}\Omega = -38.4$$

From Eq. (2.53a)

$$A_{CM} = \frac{-\beta_0 R_C}{r_\pi + 2(1+\beta_0)R_E}$$

$$= \frac{-200 \times 2\,\text{k}\Omega}{10.4\,\text{k}\Omega + 2(1+200)4.3\,\text{k}\Omega} = -0.23$$

$$\text{CMRR} = \frac{A_{DM}}{A_{CM}} = \frac{-38.4}{-0.23} = 166.9 = 44.4\ \text{dB}$$

Example 2.8

In the differential amplifier designed in Example 2.6, the following inputs are applied:

$$v_1 = 15 \sin 2\pi\,(60)t + 5 \sin 2\pi\,(1000)t\ \text{mV}$$

$$v_2 = 15 \sin 2\pi\,(60)t - 5 \sin 2\pi\,(1000)t\ \text{mV}$$

Here, the signal at 60 Hz is the interference signal and the signal to be processed is at 1 kHz. Determine the output voltages v_{o1} and v_{o2}.

Solution

We know from Example 2.6

$$g_m = 4\ m℧;\ R_C = 125\ k\Omega,\ R_E = 1.25\ k\Omega$$

and

$$r_\pi = \frac{\beta_0}{g_m} = \frac{200}{4\,m℧} = 50\ k\Omega$$

Given, $A_{DM} = -500$,

We compute A_{CM} from Eq. (2.53(a))

$$A_{CM} = \frac{-\beta_0 \times R_C}{2(1+\beta_0)R_E + r_\pi} = \frac{-200 \times 125\ k\Omega}{2(1+200)1250\ k\Omega + 50\ k\Omega} = -0.05$$

From Eqs. (2.56(a)) and (2.56(b))

$$v_{DM} = \frac{v_1 - v_2}{2} = 5 \sin 2\pi\,(1000)t$$

and

$$v_{CM} = \frac{v_1 - v_2}{2} = 15 \sin 2\pi\,(60)t$$

From Eqs. (2.57a) and (2.57b), we get

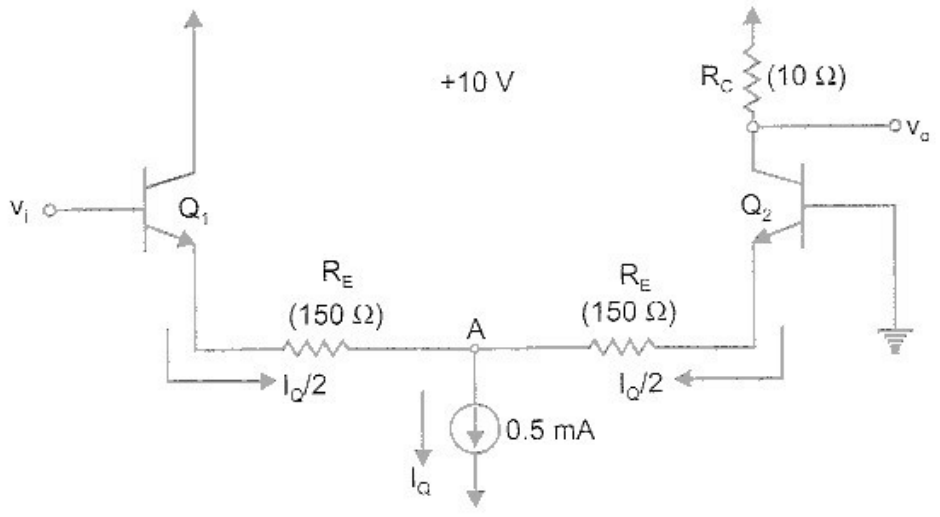
$$v_{o1} = -500[5 \sin 2\pi\,(1000)t] - 0.05[15 \sin 2\pi\,(60)t]$$
$$= -2500 \sin 2\pi\,(1000)t - 0.75 \sin 2\pi\,(60)t\ mV.$$

and

$$v_{o2} = -(-500)[5 \sin 2\pi\,(1000)t] - 0.05[15 \sin 2\pi\,(60)t]$$
$$= +2500 \sin 2\pi\,(1000)t - 0.75 \sin 2\pi\,(60)t\ mV$$

Example 2.9

For the differential amplifier shown in Fig. (i) find the differential voltage gain. Given $\beta_0 = 100$



(i) Circuit for Example 2.9

Solution

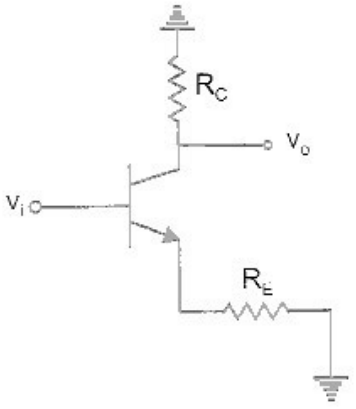
Note that the circuit is a differential amplifier with single ended output taken at the collector of Q_2. Also there is a 150 Ω resistor between emitter and terminal A.

$$I_{CQ} = \frac{I_Q}{2} = \frac{0.5\,\text{mA}}{2} = 0.25\,\text{mA}$$

$$\therefore \quad g_m = \frac{I_{CQ}}{V_T} = \frac{0.25\,\text{mA}}{25\,\text{mV}} = \frac{1}{100}\,\text{℧}$$

and

$$r_\pi = \frac{\beta_0}{g_m} = \frac{100}{1/100} = 10\ \text{k}\Omega$$



(ii) Equivalent circuit

The differential mode gain for a single stage is found from the equivalent circuit shown in Fig. (ii) and can be written as

$$A_{DM} = \frac{1}{2}\left[\frac{\beta_0 R_C}{r_\pi + (1+\beta_0)R_E}\right] \quad \text{[Eq. 2.51(b) modified on account of } R_E\text{]}$$

$$= \frac{1}{2}\left[\frac{100 \times 10\ \text{k}\Omega}{10\ \text{k}\Omega + 101 \times 150\Omega}\right] = 40\ \text{V/V}$$

Note that the sign of A_{DM} is positive because the output is taken at the collector of Q_2 whereas input is applied at the base of Q_1.

2.4.4 Circuits for Improving CMRR

For CMRR to be large, A_{CM} should be as small as possible. From Eq. (2.54), it can be seen that $A_{CM} \to 0$ as $R_E \to \infty$. There are, however, practical limitations on the magnitude of R_E because of the quiescent dc voltage across it. If R_E is made large, the emitter supply V_{EE} will also have to be increased in order to maintain the proper quiescent current. And if the operating currents of the transistors are allowed to decrease, then h_{ie} will decrease, thereby decreasing h_{fe} too. This too will decrease the common mode rejection ratio.

The use of a constant current bias in place of R_E is found to be a practical solution to the problem discussed above. In Fig. 2.15, R_E is replaced by a constant current transistor circuit in which R_1, R_2 and R_3 can be adjusted to give the same quiescent conditions for the transistors Q_1 and Q_2 as in the original circuit of Fig. 2.11 (a). The modified circuit presents a very high effective emitter resistance R_E even for very small values of R_3. Typically, R_E is hundreds of kΩ even if R_3 is as small as 1 kΩ.

Let us calculate the current I_Q and verify that the emitter circuit really behaves as a constant current source. Writing KVL for the base circuit of Q_3, we get

$$V_{BE3} + I_3 R_3 = V_D + (V_{EE} - V_D)\frac{R_2}{R_1 + R_2} \qquad (2.58)$$

Here V_D represents the drop across the diode D. If the base current is neglected, then

$$I_Q \simeq I_3 = \frac{1}{R_3}\left(\frac{V_{EE}R_2}{R_1+R_2} + \frac{V_D R_1}{R_1+R_2} - V_{BE3}\right) \tag{2.59}$$

By proper choice of resistors R_1 and R_2, it is possible to set,

$$\frac{V_D R_1}{R_1+R_2} = V_{BE3} \tag{2.60}$$

Then,
$$I_Q \simeq \frac{1}{R_3}\left(\frac{V_{EE}R_2}{R_1+R_2}\right) \tag{2.61}$$

So, it can be seen that the current I_Q will be essentially constant as it does not depend upon signal voltages v_1 and v_2.

What is the use of the diode D in this circuit? The diode D makes I_Q independent of temperature. We know that V_{BE3} decreases approximately by 2.5 mV/°C and the diode D also has the same temperature dependence. Hence, the two variations cancel each other and I_Q becomes independent of temperature. It is usually difficult to satisfy Eq. (2.60) with a single diode D in the circuit of Fig. 2.15 as V_D and V_{BE3} have almost the same value. Hence two diodes are normally used for V_D.

With I_Q constant, it can be shown that the common-mode gain is zero, so that the circuit provides very high CMRR. Under quiescent conditions (no ac signal) the current I_Q gets divided equally in identical transistors Q_1 and Q_2 and $I_{C1}=I_{C2}=I_{Q/2}$. Now if the same signal ($v_1 = v_2$) is applied to both the inputs, there will still be no change in the collector currents i_{C1} and i_{C2} as I_Q is constant. Thus the small signal current i_c flowing through the load resistor R_C is zero resulting in zero output voltage.

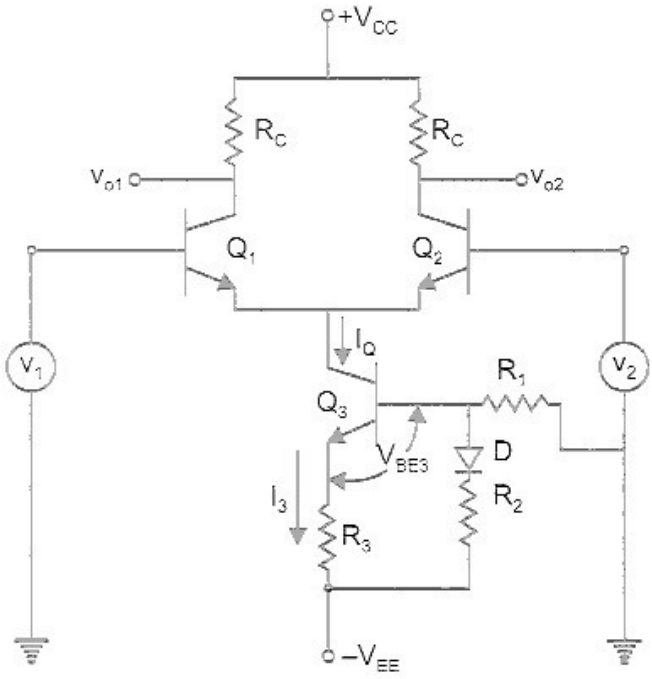


Fig. 2.15 Differential amplifier using constant current bias

Thus we can state that a diff-amp, if supplied by a constant current bias gives very high CMRR. The constant current circuit of the type shown in Fig. 2.15 is used in Motorola MC1530 (Fig. 2.21). A more commonly used IC op-amp μA 741 uses a different type of constant current source which is very simple and uses less number of components. This circuit is called current mirror and offers extremely large resistance under a.c. conditions, thereby providing a high value of CMRR.

Constant Current Source (Current Mirror)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in Fig. 2.16 transistors Q_1 and Q_2 are matched as the circuit is fabricated using IC technology. It may be noted that bases and emitter of Q_1 and Q_2 are tied together and thus have the same V_{BE}. In addition, transistor Q_1 is connected as a diode by shorting its collector to base.

The input current I_{ref} flows through the diode-connected transistor Q_1 and thus establishes a voltage across Q_1. This voltage in turn appears between the base and emitter of Q_2. Since Q_2 is identical to Q_1, the emitter current of Q_2 will be equal to emitter current of Q_1 which is approximately equal to I_{ref}. Thus, we can say that as long as Q_2 is maintained in the active region, its collector current $I_{C2} = I_o$ will be approximately equal to I_{ref}. Since the output current I_o is a reflection or mirror of the reference current I_{ref}, the circuit is often referred to as a current mirror.

This mirror effect is however, valid only for large values of β. To study the effect of β on the operation of the current mirror circuit, we analyze it further.

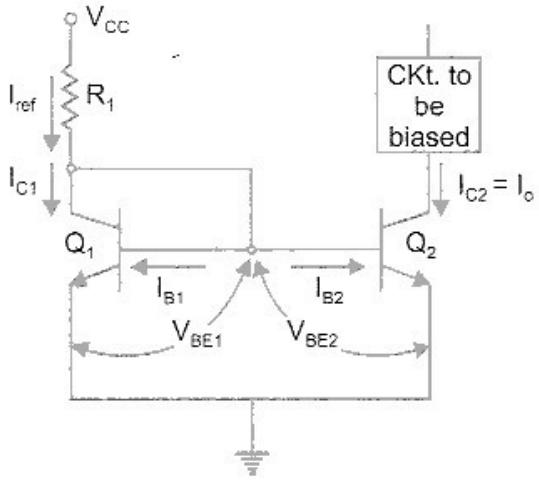


Fig. 2.16 The basic BJT current mirror

Analysis

The collector currents I_{C1} and I_{C2} for transistors Q_1 and Q_2 can be approximately expressed as

$$I_{C1} \cong \alpha_F I_{ES}\, e^{V_{BE1}/V_T} \tag{2.62}$$

$$I_{C2} \cong \alpha_F I_{ES}\, e^{V_{BE2}/V_T} \tag{2.63}$$

From Eqs. (2.62) and (2.63), we may write

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T} \tag{2.64}$$

Since $V_{BE1} = V_{BE2}$, we obtain

$$I_{C2} = I_{C1} = I_C = I_o$$

Also since both the transistors are identical, $\beta_1 = \beta_2 = \beta$.

KCL at the collector of Q_1 gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{2.65}$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2} = I_C\left(1 + \frac{2}{\beta}\right) \tag{2.66}$$

Solving Eq. (2.66), I_C may be expressed as

$$I_C = \frac{\beta}{\beta + 2} I_{ref} \tag{2.67}$$

where I_{ref} from Fig. 2.16 can be seen to be

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \cong \frac{V_{CC}}{R_1} \text{ (as } V_{BE} = 0.7 \text{ V is small)} \tag{2.68}$$

From Eq. (2.67), for $\beta >> 1$, $\beta/(\beta + 2)$ is almost unity and the output current I_o is equal to the reference current, I_{ref} which for a given R_1 is constant. Typically I_o varies by about 3% for $50 \le \beta \le 200$.

* $\beta = \beta_F$ and is the large signal CE current gain.

It is possible to obtain current transfer ratio other than unity simply by controlling the area of the emitter-base junction (EBJ) of the transistor Q_2. For example, if the area of EBJ of Q_2 is 4 times that of Q_1, then

$$I_o = 4\ I_{ref}$$

The output resistance of the current source is the output resistance, r_o of Q_2,

$$R_o = r_{02} = \frac{V_A}{I_o} \cong \frac{V_A}{I_{ref}} \quad [V_A \text{ is the Early voltage}]$$

The circuit however operates as a constant current source as long as Q_2 remains in the active region. From the volt-ampere characteristics of Q_2 shown in Fig. 2.17, it can be seen that for $V_{CE2} < 0.3$ V, Q_2 is saturated. For $V_{CE2} > 0.3$ V, transistor operates in the active region and I_{C2} is essentially constant. The slight increase in I_{C2} is due to Early effect. The 1/slope of the curve in this region gives the output resistance r_o of the current source. For all practical purposes, early voltage may be assumed to be infinite, so that $r_o \to \infty$ and I_{C2} is constant.

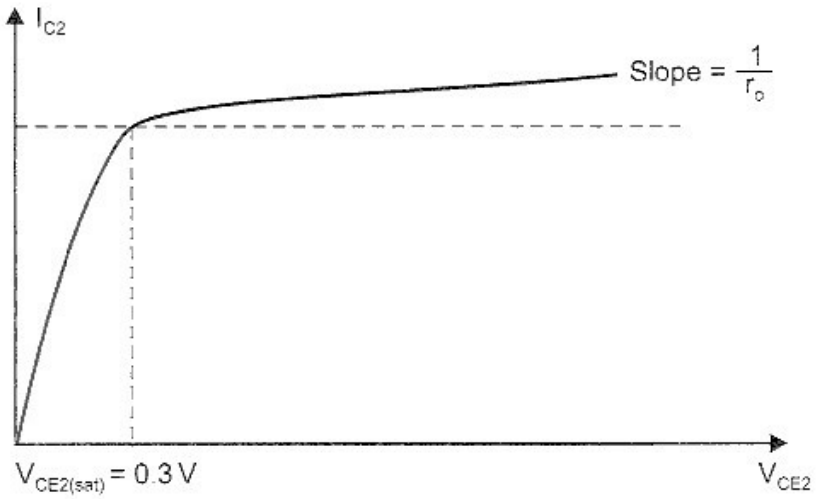


Fig. 2.17 Volt-ampere characteristics for transistor Q_2

Example 2.10

The current mirror of Fig. 2.16 is to provide a 1.0 mA current with $V_{CC} = 10$ V. Assume $\beta = 125$ and $V_{BE} = 0.7$ V. Determine (a) the value of R_1 (b) value of R_1 for $I_C = 10\ \mu A$.

Solution

(a) From Eq. (2.67), we have

$$1.0\ \text{mA} = \frac{125}{125+2} \times \frac{10\ \text{V} - 0.7\ \text{V}}{R_1}$$

$$R_1 = 9.15\ \text{k}\Omega$$

(b) Again using Eq. (2.67), the value of R_1 is found to be

$$R_1 = 915\ \text{k}\Omega$$

Widlar Current Source

The basic current mirror of Fig. 2.16 has a limitation. Whenever, we need low value current source as in Example 2.6 part (b), the value of the resistance R_1 required is sufficiently high and can not be fabricated economically in IC circuits. In Fig. 2.18 is shown a widlar current source which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance R_E that is included in the emitter lead of Q_2. It can be seen that due to R_E, the base-emitter voltage V_{BE2} is less than V_{BE1} and consequently current I_o is smaller than I_{C1}.

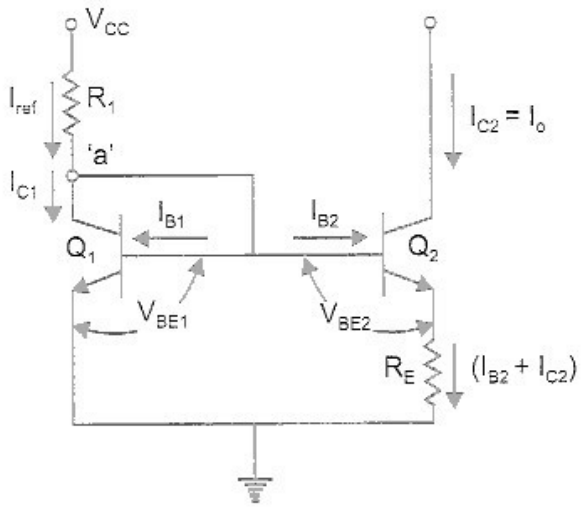


Fig. 2.18 Widlar current source

The ratio of collector currents I_{C1} and I_{C2} using Eqs. (2.62) and (2.63) is given by

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \tag{2.69}$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln\left(\frac{I_{C1}}{I_{C2}}\right) \tag{2.70}$$

Writing KVL for the emitter base loop

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2})R_E \tag{2.71}$$

or
$$V_{BE1} - V_{BE2} = (1/\beta + 1)\, I_{C2}R_E \tag{2.72}$$

From Eqs. (2.70) and (2.72), we obtain

$$\left(\frac{1}{\beta} + 1\right) I_{C2}R_E = V_T \ln \frac{I_{C1}}{I_{C2}} \tag{2.73}$$

or
$$R_E = \frac{V_T}{\left(1 + \frac{1}{\beta}\right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}} \tag{2.74}$$

A relation between I_{C1} and the reference current I_{ref} is obtained by writing KCL at the collector point of Q_1 (node 'a')

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \tag{2.75}$$

$$= I_{C1}\left(1 + \frac{1}{\beta}\right) + \frac{I_{C2}}{\beta} \tag{2.76}$$

(Assuming $\beta_2 = \beta_1 = \beta$ for identical transistors)

In the Widlar current source $I_{C2} << I_{C1}$, therefore the term I_{C2}/β may be neglected in Eq. (2.76).

Thus $$I_{ref} \cong I_{C1}\left(1+\frac{1}{\beta}\right) \tag{2.77}$$

or $$I_{C1} = \frac{\beta}{\beta+1} I_{ref} \tag{2.78}$$

where $$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \tag{2.79}$$

For $\beta >> 1$, $$I_{C1} \cong I_{ref} \tag{2.80}$$

The design and advantages of Widlar current source are illustrated in the following example:

Example 2.11

Design a Widlar current source for generating a constant current I_0 = 10 μA. Assume V_{CC} = 10 V, V_{BE} = 0.7 V, β = 125. Use V_T = 25 mV.

Solution

For the Widlar current source of Fig. 2.18, we must first decide a suitable value for I_{ref}. If we choose I_{ref} = 1 mA, then, R_1 is given by

$$R_1 = \frac{10\,\text{V} - 0.7\,\text{V}}{1\,\text{mA}} = 9.3\,\text{k}\Omega$$

The value of R_E is determined from Eq. (2.74)

$$R_E = \frac{0.025}{\left(1+\frac{1}{125}\right)10\,\text{Ÿ}\,10^{-6}} \ln\left(\frac{1\,\text{mA}}{10\,\mu\text{A}}\right) = 11.5\ \text{k}\Omega$$

It is clearly seen that Widlar circuit allows the generation of small currents using relatively small resistors.

Sometimes, it is convenient to use emitter resistances in both the transistors Q_1 and Q_2 as shown in Fig. 2.19. If $R_1 = R_2$ the currents $I_{C1} = I_{C2}$. The same circuit can also be used to provide different currents in Q1 and Q2, as we shall now see.

Analysis

Rewriting Eq. (2.64) as

$$V_{BE2} - V_{BE1} = V_T \ln \frac{I_{C2}}{I_{C1}} \tag{2.81}$$

Writing KVL in the base-emitter loop

$$V_{BE2} - V_{BE1} = I_{C1}R_1 - I_{C2}R_2$$

(Neglecting base current) (2.82)

From Eqs. (2.81) and (2.82),

$$I_{C1}R_1 - I_{C2}R_2 = V_T \ln \frac{I_{C2}}{I_{C1}} \tag{2.83}$$

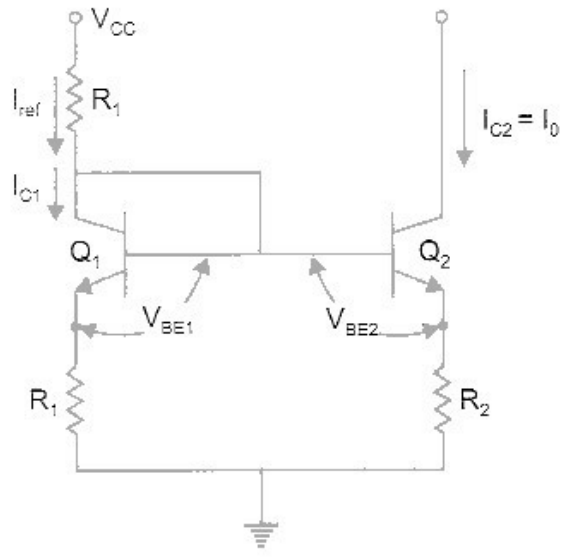


Fig. 2.19 A current mirror with magnification ($I_{C2}/I_{C1} \cong R_1/R_2$)

$$\frac{I_{C2}}{I_{C1}}\frac{R_2}{R_1} = 1 - \frac{V_T}{I_{C1}R_1}\ln\frac{I_{C2}}{I_{C1}} \tag{2.84}$$

$$\frac{I_{C2}}{I_{C1}} = \frac{R_1}{R_2}\left(1 - \frac{V_T}{I_{C1}R_1}\ln\frac{I_{C2}}{I_{C1}}\right) \tag{2.85}$$

For the range $0.1 < \frac{I_{C2}}{I_{C1}} < 10$, we can assume $\frac{I_{C2}}{I_{C1}} \cong \frac{R_1}{R_2}$. Thus even large ratios $\frac{I_{C2}}{I_{C1}}$ (say 10) is easily obtained by the modified circuit.

Current Repeaters

The basic current mirror of Fig. 2.16 can be used to source current to more than one load. Such a circuit is called current repeater and is shown in Fig. 2.20. If all the transistors are identical, then the current $I_C = I_{C1} = \ldots\ \ldots = I_{CN} \cong I_{ref}$.

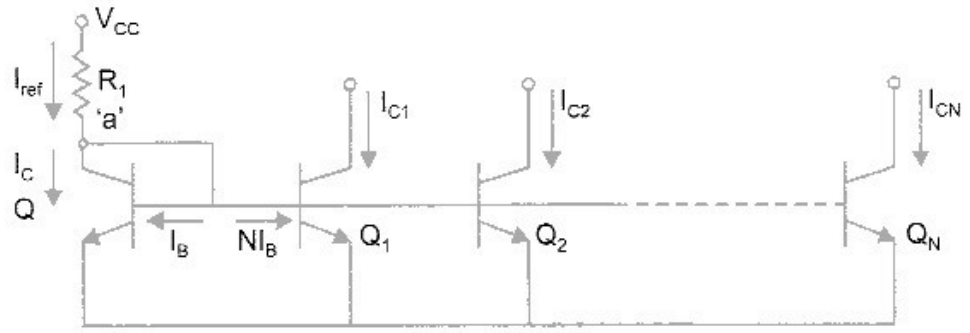


Fig. 2.20 A current repeater to source current to N transistors Q_1, Q_2, ... Q_N

It can be seen from Fig. 2.20 at node 'a'

$$I_{ref} = I_C + I_B + NI_B \text{ (Assuming identical transistors)} \tag{2.86}$$

$$= I_C + \frac{(1+N)}{\beta}I_C$$

$$= I_C\left(1 + \frac{(1+N)}{\beta}\right) \tag{2.87}$$

Thus

$$I_C = I_{ref}\frac{\beta}{\beta+1+N} \tag{2.88}$$

It is possible to achieve different value of I_{C1}, I_{C2}, ... I_{CN} by scaling the emitter area of transistors Q_1, Q_2, ... Q_N. The same can also be achieved by using emitter resistance as in the Widlar current source.

Example 2.12

For the circuit shown in Fig. 2.21 determine I_{C1}, I_{C2}, and I_{C3}. Assume $\beta = 125$

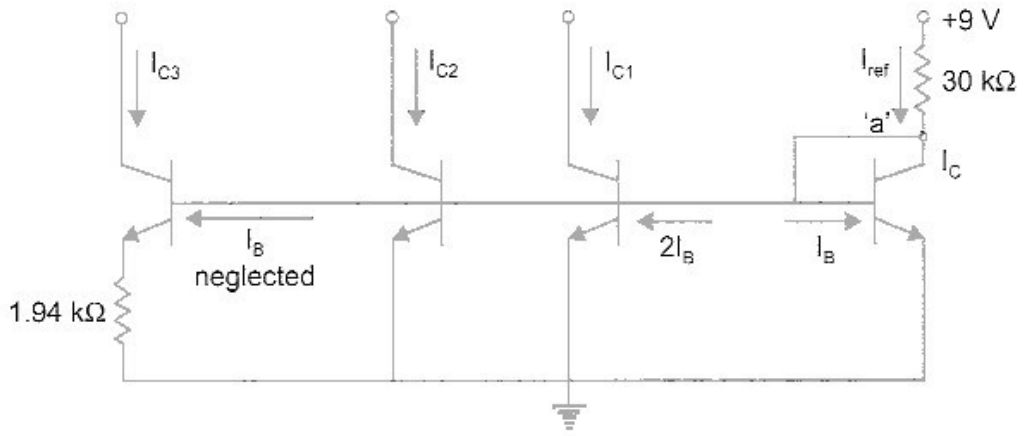


Fig. 2.21 Circuit for Example 2.12

Solution

$$I_{ref} = \frac{9\text{V} - 0.7\text{V}}{30\ \text{k}\Omega} = 0.277\ \text{mA}$$

Also at node 'a'

$$I_{ref} = I_C + 3I_B \text{ (Assume } I_{B3} \text{ of Widlar source negligible)}$$

$$= I_C\left(1 + \frac{3}{\beta}\right)$$

$$I_C = I_{ref}\left(\frac{\beta}{3+\beta}\right)$$

Putting the values and solving, we get

$$I_{C1} = I_{C2} = 0.271\ \text{mA}$$

Calculate I_{C3}, using Eq. (2.74) gives

$$1.94 = \frac{0.025}{I_{C3}\left(1 + \frac{1}{125}\right)} \ln \frac{0.271}{I_{C3}}$$

Solving the transcendental equation by trial and error, we obtain

$$I_{C3} = 0.0287\ \text{mA}$$

Improved Current Source Circuits

A good current source must meet two requirements. The first is that the output current, I_o should not be dependent upon β and secondly the output resistance of the current source should be very high. The need for high output resistance current source can be seen because the common-mode gain of the differential amplifier (used as basic building block in op-amps) can only be reduced by using high resistance current sources. Also, all differential amplifiers invariably use current source as a load. Thus to obtain high voltage gain a large output resistance load is required. Now, we discuss two circuits that exhibit reduced dependence on β or increased output resistance.

A Current Source with Gain

The circuit shown in Fig. 2.22 includes a transistor Q_3 whose emitter current supplies the base currents of Q_1 and Q_2. The expression for the source current $I_o = I_{C2}$ can be derived by writing KCL at node 'a'

$$I_{ref} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1+\beta} \qquad (2.89)$$

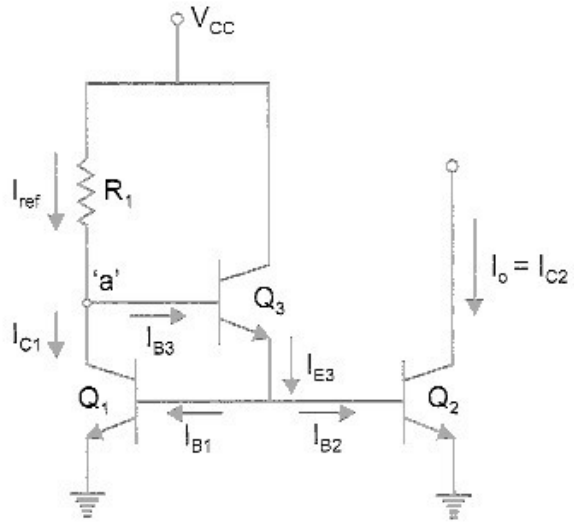


Fig. 2.22 A current source with gain

Also $I_{E3} = I_{B1} + I_{B2} = 2I_B$ (since Q_1 and Q_2 are identical)

Thus,

$$I_{ref} = I_{C1} + \frac{2I_B}{1+\beta} \qquad (2.90)$$

$$= I_C + \frac{2I_C}{\beta(1+\beta)} = I_C\left(1 + \frac{2}{\beta(1+\beta)}\right)$$

or $$I_o = I_C = I_{ref}\,\frac{\beta(1+\beta)}{\beta^2+\beta+2} \qquad [I_{C1} = I_{C2} = I_o] \qquad (2.91)$$

where

$$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1}$$

It is easily seen from Eq. (2.91) that the output current is essentially independent of β. The output resistance of the current source is only r_0. It can however be increased by using emitter resistances in Q_1 and Q_2 as is done in the modified Widlar source circuit in Fig. 2.19. The two emitter resistors can also be used to make I_o different from I_{ref}.

Wilson Current Source

The final current source shown in Fig. 2.23 provides an output current I_0, which is very nearly equal to I_{ref} and also exhibits a very high output resistance.

Analysis

Since $V_{BE1} = V_{BE2}$

$I_{C1} = I_{C2}$ and $I_{B1} = I_{B2} = I_B$

At node 'b'

$$I_{E3} = 2I_B + I_{C2} = \left(\frac{2}{\beta} + 1\right) I_{C2} \qquad (2.92)$$

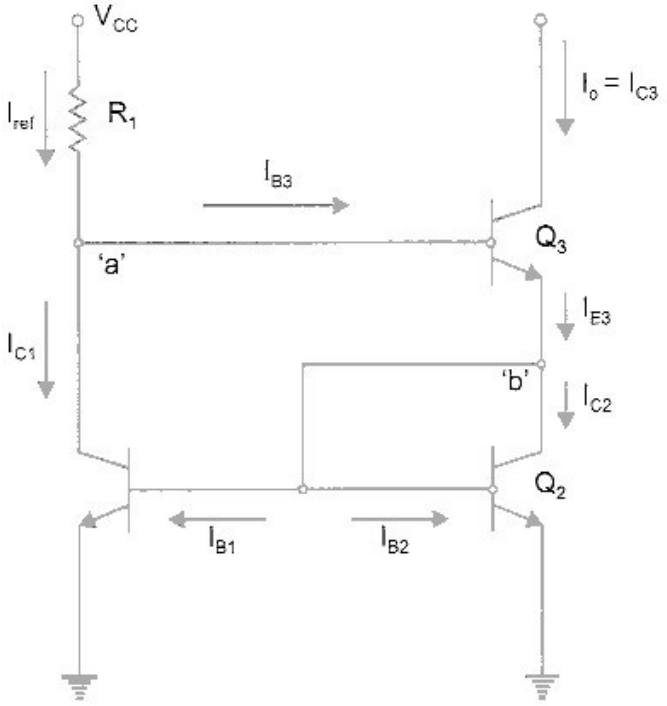


Fig. 2.23 A Wilson current source

I_{E3} is also equal to

$$I_{E3} = I_{C3} + I_{B3} = I_{C3}\left(1 + \frac{1}{\beta}\right) \tag{2.93}$$

From Eqs. (2.92) and (2.93), we obtain

$$I_{C3}\left(1 + \frac{1}{\beta}\right) = I_{C2}\left(1 + \frac{2}{\beta}\right)$$

$$I_{C3} = I_o = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C2} \tag{2.94}$$

Since $I_{C1} = I_{C2}$

$$I_o = \left(\frac{\beta + 2}{\beta + 1}\right) I_{C1} \tag{2.95}$$

At node 'a'

$$I_{ref} = I_{C1} + I_{B3} = \frac{\beta + 1}{\beta + 2} I_o + \frac{I_o}{\beta} = \frac{\beta^2 + 2\beta + 2}{\beta^2 + 2\beta} I_o$$

or

$$I_o = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} I_{ref} \tag{2.96}$$

where

$$I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1} \tag{2.97}$$

The difference

$$I_o - I_{ref} = \frac{2}{\beta^2 + 2\beta + 2} I_{ref} \tag{2.98}$$

is extremely small error for modest values of β. The output resistance of a Wilson current mirror is substantially greater $\left(\cong \beta\frac{r_o}{2}\right)$ than simple current mirror or Widlar current mirror.

More Solved Examples

Example 2.13

For the circuit shown in Fig. 2.24, determine the value of I_0 for β = 100. Assume V_{BE} = 0.7 V

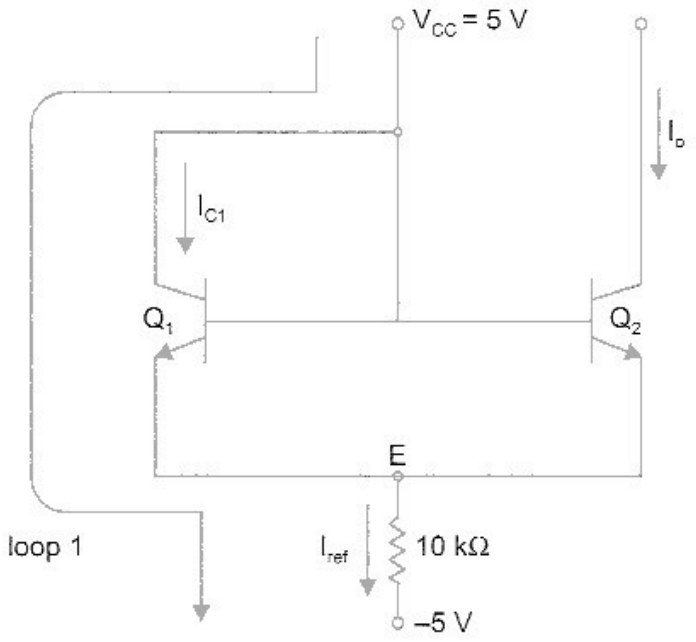


Fig. 2.24 Circuit for Example 2.13

Solution

Writing KVL for the indicated loop 1

$$5\,\text{V} - V_{BE} - 10\,\text{k}\Omega\, I_{ref} + 5\,\text{V} = 0$$

$$I_{ref} = \frac{10\,\text{V} - 0.7\,\text{V}}{10\,\text{k}\Omega} = 0.93\ \text{mA}$$

At emitter node '*E*'

$$I_{ref} = 2I_E \qquad \text{(Assuming identical transistors)}$$

$$= 2(I_C + I_B) = 2I_C\left(1 + \frac{1}{\beta}\right)$$

Then $$I_C = \frac{\beta}{2(1+\beta)} I_{ref} = 0.46\ \text{mA}$$

Due to mirror effect $$I_o = I_{C1} = I_C = 0.46\ \text{mA}$$

Example 2.14

For the circuit shown in Fig. 2.25.

(a) Determine I_{C1} and I_{C2}

(b) Find R_C so that $V_0 = 6$ V. Assume $\beta = 200$.

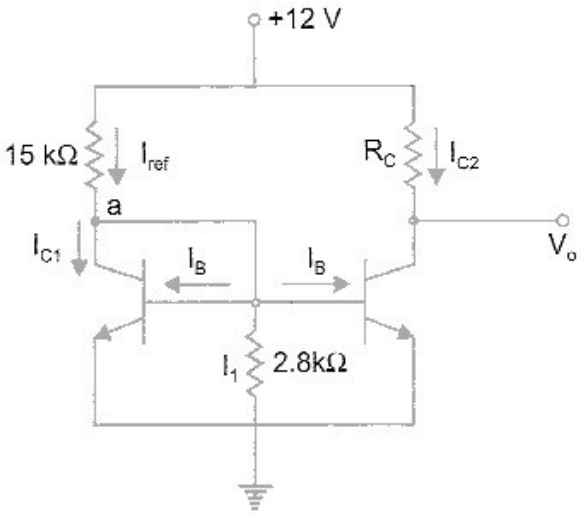


Fig. 2.25 Circuit for Example 2.14

Solution

(a) $$I_{ref} = \frac{12\,\text{V} - 0.7\,\text{V}}{15\,\text{k}\Omega} = 0.75\,\text{mA}$$

and $$I_1 = \frac{0.7\,\text{V}}{2.8\,\text{k}\Omega} = 0.25\,\text{mA}$$

At node 'a'

$$I_{ref} = I_{C1} + 2I_B + I_1$$

$$= I_{C1}\left(1 + \frac{2}{\beta}\right) + I_1$$

Solving for I_{C1} gives

$$I_{C1} = 0.495\ \text{mA} \cong 0.5\ \text{mA}$$

$$I_{C2} = I_{C1} \qquad \text{(due to mirror effect)}$$

(b) From the outer loop

$$12\ \text{V} = I_{C2}R_C + V_o$$

$$R_C = \frac{12\,\text{V} - 6\,\text{V}}{0.5\,\text{mA}} = 12\ \text{k}\Omega$$

Example 2.15

Figure 2.26 shows a modified current mirror circuit. Determine the emitter current in transistor Q_3 if $\beta = 100$ and $V_{BE} = 0.75$ V.

Solution

From Fig. 2.26 at node 'a'

$$I = I_{C1} + I_1 = I_{C1} + I_{B1} + I_1'$$

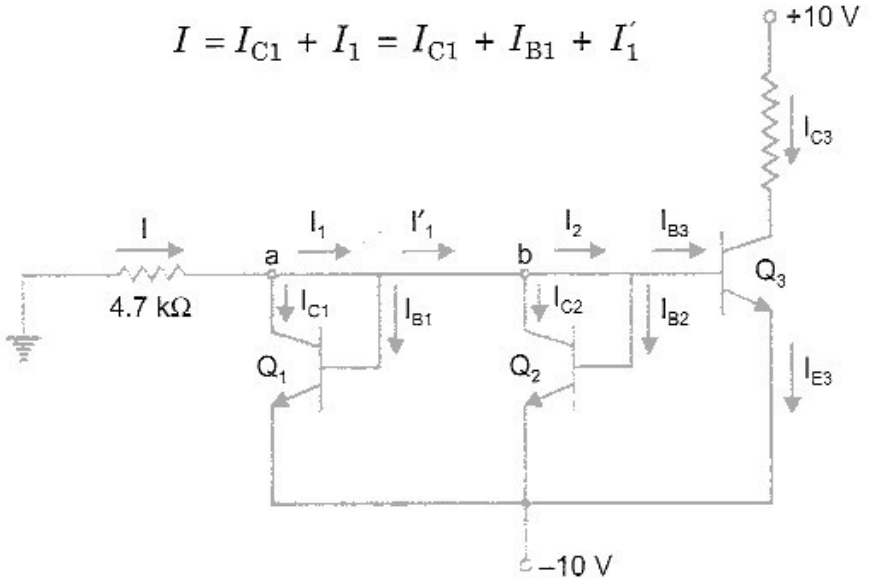


Fig. 2.26 Circuit of Example 2.15

or, $$I = I_{C1}\left(1+\frac{1}{\beta}\right) + I_1' \simeq I_{C1} + I_1' \quad (\text{as } \beta >> 1)$$

Also at node 'b'

$$I_1' = I_{C2} + I_2 = I_{C2} + I_{B2} + I_{B3} = I_{C2}\left(1+\frac{1}{\beta}\right) + I_{B3} \simeq I_{C2} + I_{B3}$$

Putting the value of I_1', we get

$$I = I_{C1} + I_{C2} + I_{B3} = 2I_C + I_{B3} \qquad [\text{as } I_{C1} = I_{C2} = I_C]$$

$$\simeq I_C\left(2+\frac{1}{\beta}\right) \simeq 2I_C$$

The current I is given by,

$$I = \frac{10 - 0.75}{4.7\ \text{k}\Omega} = \frac{9.25}{4.7\ \text{k}\Omega} = 1.97\ \text{mA}$$

The collector current of Q_3 is equal to the collector current of Q_1 and Q_2 due to mirror action. Therefore, the emitter current

$$I_{E3} \simeq I_{C3} = I_C = \frac{I}{2} = 0.98\ \text{mA}$$

2.4.5 Input Resistance

The resistance offered by the differential amplifier of Fig. 2.27 to the differential input signal $(v_1 - v_2)$ is called differential input resistance R_{id}. The emitters of Q_1 and Q_2 are floating as R_E is replaced by a constant current source, therefore $R_{id} \simeq h_{ic1} + h_{ic2} = 2\ h_{ic}$. If input 2 is grounded, then input 1 is loaded by 2 h_{ie}. The value of h_{ie} can be increased by reducing the biasing currents for Q_1 and Q_2 and input resistance of the order of 500 kΩ can be obtained.

Higher values of input resistance can be obtained by using a Darlington pair in place of transistor Q_1 and Q_2 of Fig. 2.27 as shown in Fig. 2.28. One drawback of the Darlington differential amplifier is the higher offset voltage V_{os}, (due to cascaded stages) which is about 2 times larger than the ordinary two transistor differential amplifier.

The most important feature of the Darlington pair differential amplifier is its extraordinary large current gain. For the circuit shown in Fig. 2.28, the overall current gain is

$$\beta = \frac{I_C}{I_{B1}} = \frac{I_{C1} + I_{C2}}{I_{B1}} = \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B1}}$$

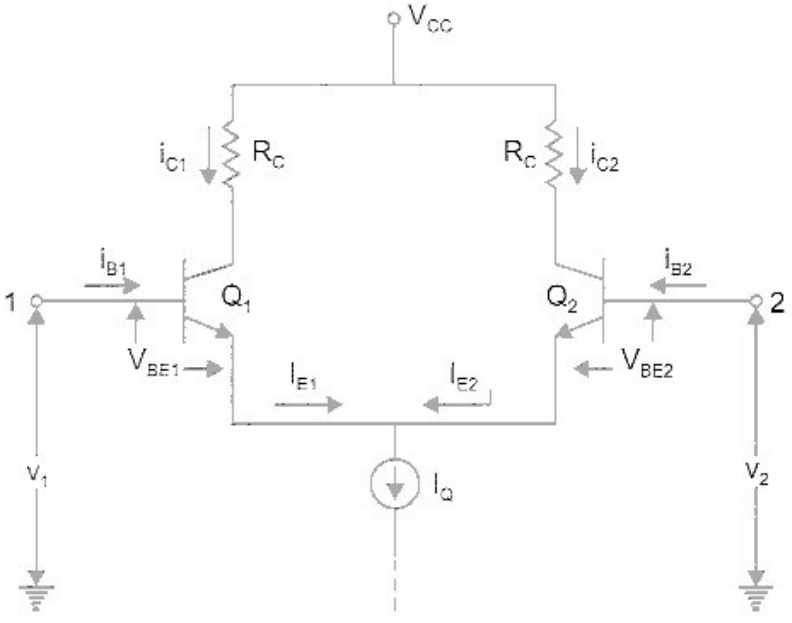


Fig. 2.27 Differential amplifier

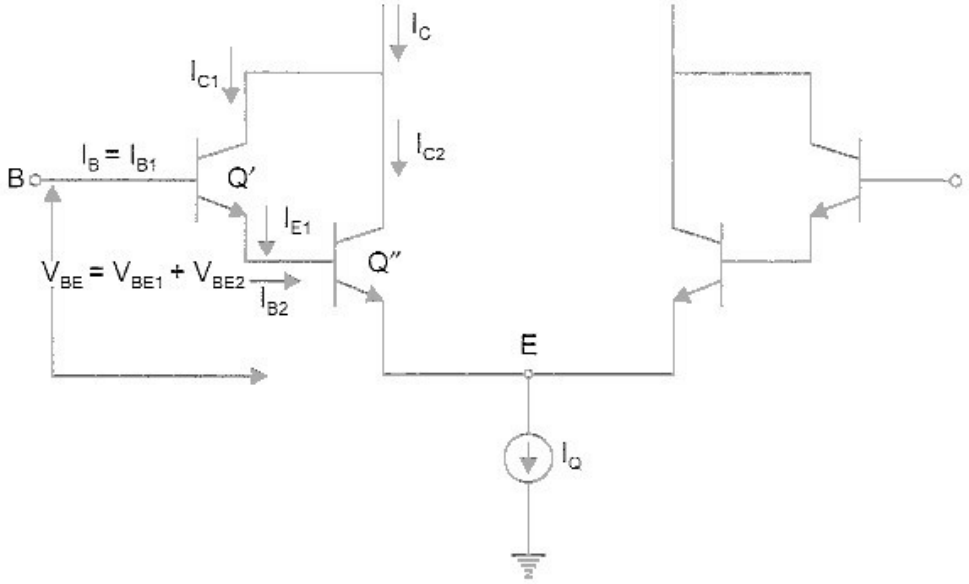


Fig. 2.28 Differential amplifier using Darlington pair

$$= \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B2}} \times \frac{I_{B2}}{I_{B1}}$$

$$= \beta_1 + \beta_2 (\beta_1 + 1) \quad \left[\begin{matrix} I_{B2} = I_{E1} \\ = I_{C1} + I_{B1} \end{matrix}\right] \cong \beta_2\beta_1$$

So, the overall current gain β of the Darlington circuit will be of the order of 10,000 if the current gain of the individual transistor is about 100. Another method to get higher input resistance is to fabricate a FET differential pair as the input stage with the rest of the stages made of BJTs. Input resistance of the order of 10^{12} Ω is possible with such JFET inputs. A number of such op-amps are described in Sec. 2.6.

2.4.6 Active Load

The open circuit voltage gain of an op-amp should be as large as possible and this is achieved by cascading gain stages. However, this increases the phase shift too and amplifier becomes more susceptible to breaking out into oscillations. One can think of increasing gain by using large collector resistance values as gain is proportional to load resistor R_C. However, there are limitations to the maximum value of R_C to be used due to the following two reasons:

(i) A large value of resistance requires a large chip area.

(ii) For large R_C quiescent drop across it increases and hence a large power supply will be required to maintain a given quiescent collector current. These difficulties are circumvented by using a current source of the type shown in Fig. 2.16 as load in the place of R_C.

The current mirror discussed earlier has a dc resistance of the order of few kilohms, as the quiescent voltage across it is a fraction of the supply voltage and the current is in milliamperes. However, since it acts as a constant current source, its dynamic resistance (ac) is very high. Hence, a current mirror can also be used as an active load for an amplifier to obtain a very large voltage gain. Figure 2.29 (a) shows a diff-amp with an active load. The current mirror uses *pnp* transistors Q_3 and Q_4. The constant current I_Q may also be obtained from a current mirror. The operation of the circuit in Fig. 2.29 (a) is as follows:

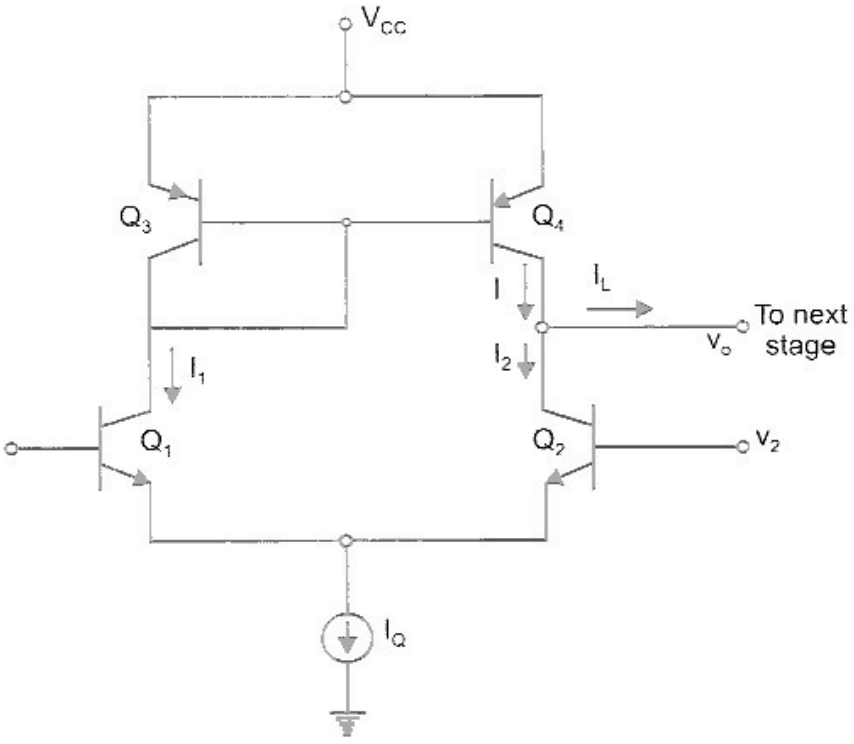


Fig. 2.29 (a) A differential amplifier with an active load Q_3–Q_4

Under the quiescent conditions, $v_1 = v_2 = 0$. From symmetry of Q_1 and Q_2, $I_1 = I_2 = I_Q/2$ where base currents are assumed to be neglected. Since Q_3 and Q_4 form a current mirror, $I = I_1 = I_2$. The load current I_L entering the next stage is

$$I_L = I - I_2 = 0 \tag{2.99}$$

However, when v_1 is increased over v_2, I_1 increases whereas I_2 decreases, since $I_1 + I_2 = I_Q$ (constant). Also the current I always remains equal to I_1 due to the current mirror. The load current is given by

$$\begin{aligned} I_L &= I - I_2 = I_1 - I_2 \\ &= g_m v_1 - g_m v_2 = g_m (v_1 - v_2) \\ &= g_m v_d \end{aligned} \tag{2.100}$$

The circuit thus behaves as a transconductance amplifier.

A popular op-amp (μA741) by Fairchild uses an alternate active load as shown in Fig. 2.29 (b). The transistors Q_1–Q_3 and Q_2–Q_4 are in cascode configuration (CE-CB) with input signal as v_1 (v_2). The transistors Q_5, Q_6 and Q_7 form the active load of the type shown in Fig. 2.22. The transistors Q_8 and Q_9 form the current mirror to provide the constant current I_Q required for high CMRR of the diff-amp. If base currents are neglected, then $I_Q \simeq I_3$. The arrangement Q_{10} and Q_{11} is another current mirror where $I_3 << I_4$ due to 5 kΩ emitter resistor. Consequently $I_Q = I_3$ is small (of the order of μA) giving a very high input resistance.

Under the quiescent conditions, $I_1 = I_2 = I_Q/2$. Since I is always equal to I_1, the load current $I_L = I_2 - I = I_2 - I_1 = 0$. Now if v_1 is increased and v_2 is decreased, I_1 rises and I_2 falls from the quiescent value of $I_Q/2$. With this excitation, $I_L = I_2 - I_1$ changes from zero to a negative value. Thus the circuit behaves as a transconductance amplifier because I_L is proportional to $v_1 - v_2$.

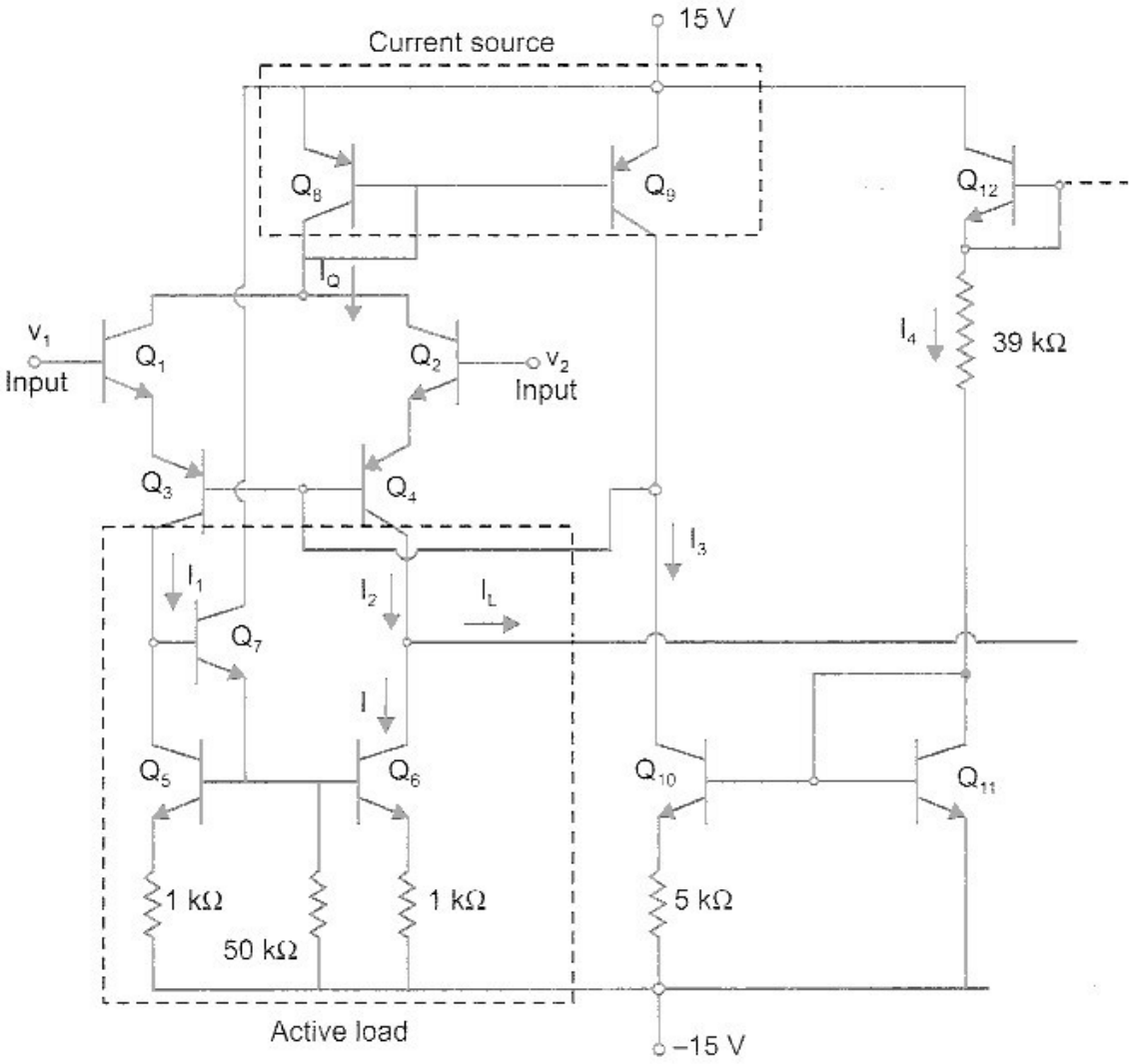


Fig. 2.29 (b) Active load (Q_5–Q_6–Q_7) of a low current differential amplifier μA741

2.4.7 Level Translator

There are two good reasons for using a level shifter in an IC op-amp. As we want an op-amp to operate down to dc, no coupling capacitor is used. Because of direct coupling, the dc level rises from stage to stage. The increase in dc level tends to shift the operating point of the next stage. This, in turn, limits the output voltage swing and may even distort the output signal. It, therefore, becomes essential that the quiescent voltage of one stage is shifted before it is applied to the next stage. Another requirement to be satisfied is that the output should have quiescent voltage level of 0 V for zero input signal.

The simplest type of a level shifter is shown in Fig. 2.30 (a). It may be noted that this is basically an emitter follower. Hence the level shifter also acts as a buffer to isolate the high gain stages from the output stage. The amount of shift obtained

$$V_o - V_i = -V_{BE} \simeq -0.7 \text{ V} \tag{2.101}$$

If this shift is insufficient, the output can be taken at the junction of two resistors R_1 and R_2, as shown in Fig. 2.30 (b). The voltage shift is now increased by the drop across R_1. However, this arrangement has the disadvantage that signal voltage also gets attenuated by $R_2/(R_1 + R_2)$. This can be easily circumvented if R_2 is replaced by a current mirror I as shown in Fig. 2.30 (c).

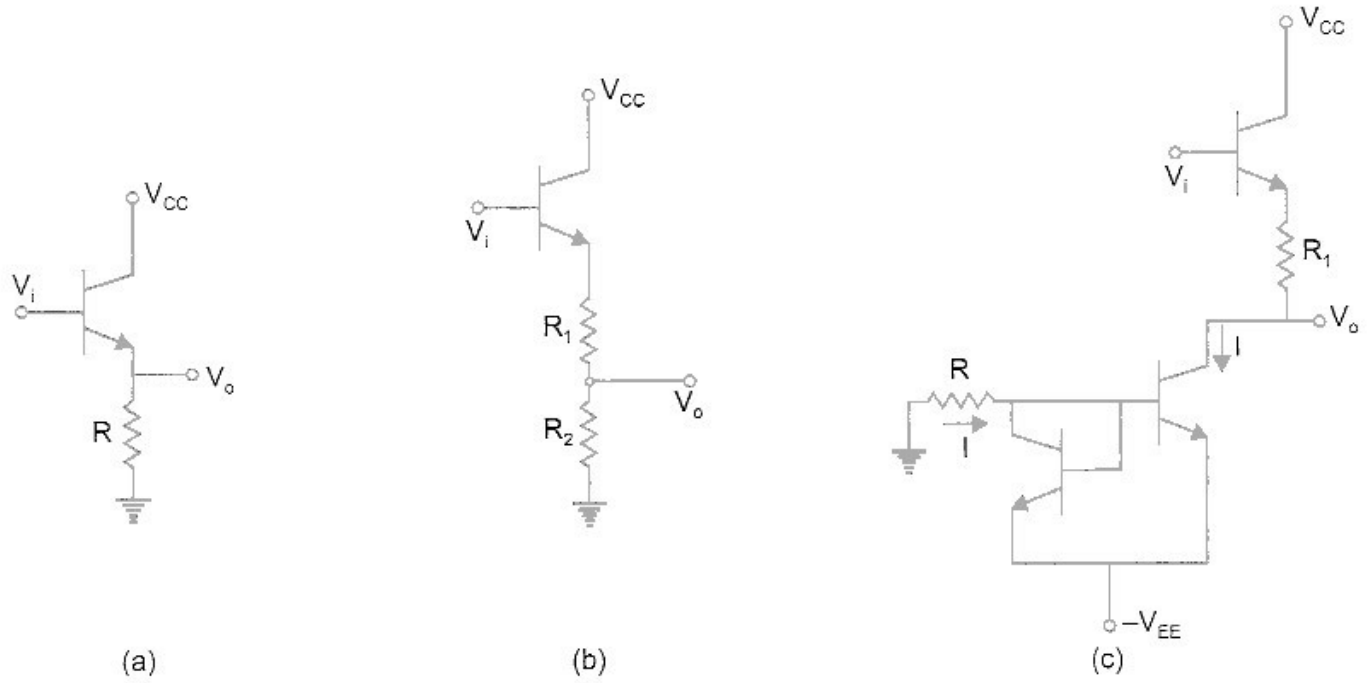


Fig. 2.30 (a)–(c) Level shifters using emitter follower buffer

The shift in level now is

$$V_o - V_i = -(V_{BE} + I R_1) \tag{2.102}$$

and there is no ac attenuation due to high resistance of the current source.

Another voltage source commonly used in μA741 op-amp is shown in Fig. 2.30 (d). It can be seen that if base current is negligible compared to the current in R_3 and R_4, then the circuit behaves as a V_{BE} multiplier as,

$$V = \frac{V_{BE}}{R_4}(R_3 + R_4) = V_{BE}\left(1 + \frac{R_3}{R_4}\right) \tag{2.103}$$

This voltage source can also be used to replace R_1 in Fig. 2.30 (b).

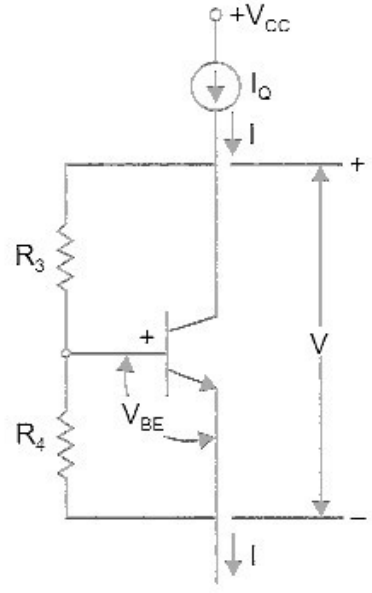


Fig. 2.30 (d) A voltage source V which is a multiple of V_{BE}

Example 2.16

Calculate $V_1 - V_2$ for the level shifter shown in Fig. 2.31. Assume identical silicon transistors with $V_{BE} = 0.7$ V and very large values of β.

Solution

Transistors Q_1 and Q_2 form a current mirror.

So, $$I_{C1} = I_{C2} = I$$

and $$I = \frac{15 - 0.7}{10\,\text{k}\Omega} = 1.43\,\text{mA}$$