2

OPERATIONAL AMPLIFIER

2.1 INTRODUCTION

Linear integrated circuits are being used in a number of electronic applications such as in fields like audio and radio communication, medical electronics, instrumentation control, etc. An important linear IC is operational amplifier which will be discussed in this chapter.

The operational amplifier (commonly referred to as op-amp) is a multi-terminal device which internally is quite complex. Fortunately, for the ordinary user, it is not necessary to know about the op-amp's internal make-up. The manufacturers have done their job so well that op-amp's performance can be completely described by its terminal characteristics and those of external components that are connected to it. However, for the designer's interest, the electronics of op-amp is described where the various stages of op-amp are discussed. Then some of the FET op-amps are described. The dc and ac characteristics with compensating techniques and the various applications of op-amp are taken up later.

2.2 BASIC INFORMATION OF OP-AMP

Circuit Symbol

The circuit schematic of an op-amp is a triangle as shown in Fig. 2.1. It has two input terminals and one output terminal. The terminal with a (–) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

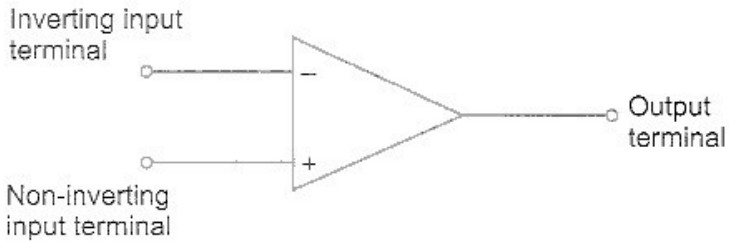


Fig. 2.1 Op-amp circuit symbol

Packages

There are three popular packages available:

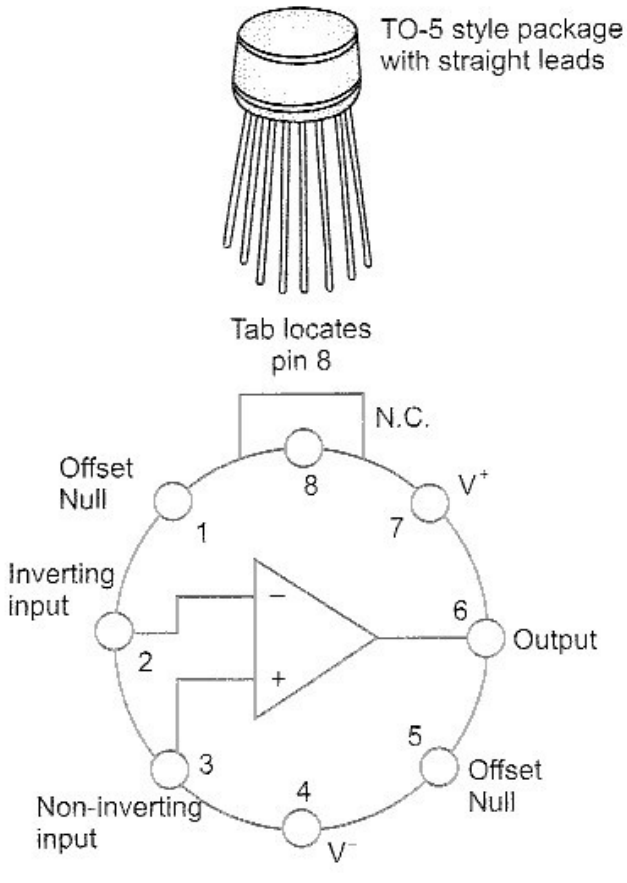
1. The metal can (TO) package
2. The dual-in-line package (DIP)
3. The flat package or flat pack

Op-amp packages may contain single, two (dual) or four (quad) op-amps. Typical packages have 8 terminals (the can and the DIP or MINI DIP), 10 terminals (flatpacks and some cans) and 14 terminals (the DIP and the flat pack). The widely used very popular type, for example μA741 is a single op-amp and is available as an 8-pin can, an 8-pin DIP, a 10-pin flatpack or a 14-pin DIP. The μA747 is a dual 741 and comes in either a 10-pin can or a 14-pin DIP. Figure 2.2 shows the various IC packages along with the top view of connection diagram.

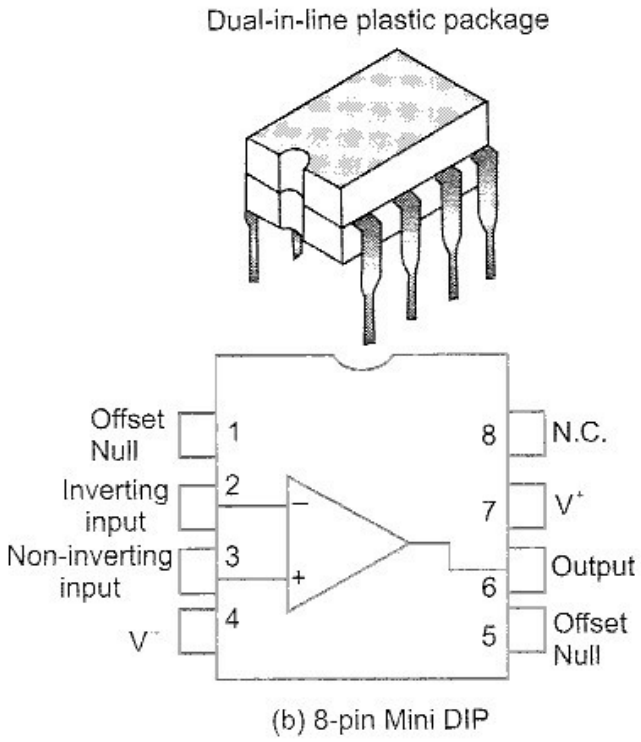
OP-AMP Terminals

Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals. The significance of other terminals varies with the type of the op-amp.

Refer to the top view of a metal can package (μA741) in Fig. 2.2 (a). The metal can has eight pins with pin number 8 identified by a tab. The other pins are numbered counter-clockwise from pin 8, beginning with pin 1. Pin 2 is called the inverting input terminal and pin 3 is the non-inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the power supply terminals labelled as V^+ and V^- respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates 'No Connection'. In case of DIP package of 741 as in Fig. 2.2 (b, c), the top pin on the left of the notch locates pin 1, and the flat pack of Fig. 2.2 (d) has a dot on it for identification. The other pins are numbered counter-clockwise from pin 1. The pin numbers have been illustrated only for some popular op-amps and the user should consult the manufacturer's data sheet before connecting a given op-amp into a circuit.

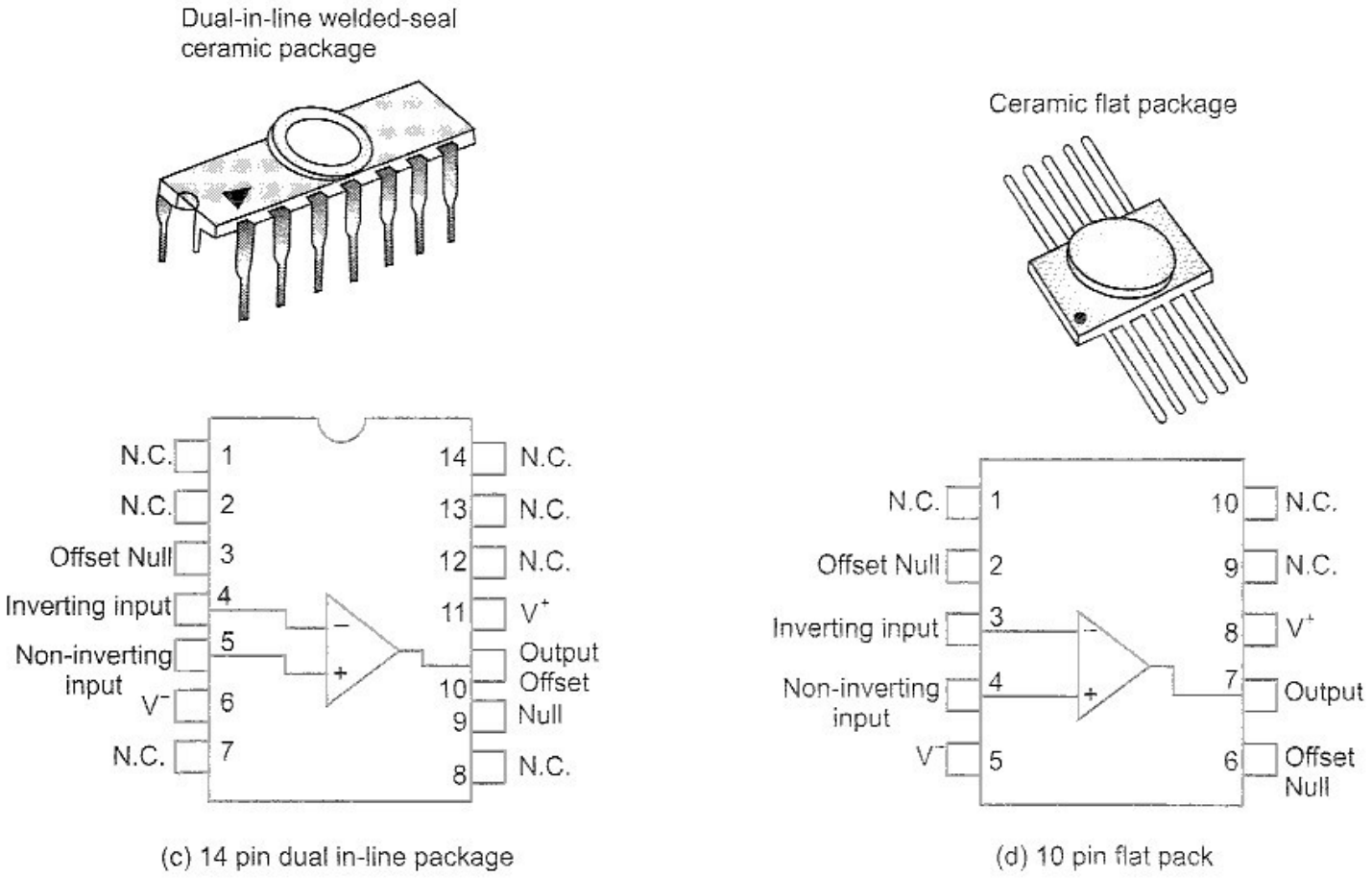


(a) 8-pin Metal can



(b) 8-pin Mini DIP

(Fig. 2.2 Contd.)

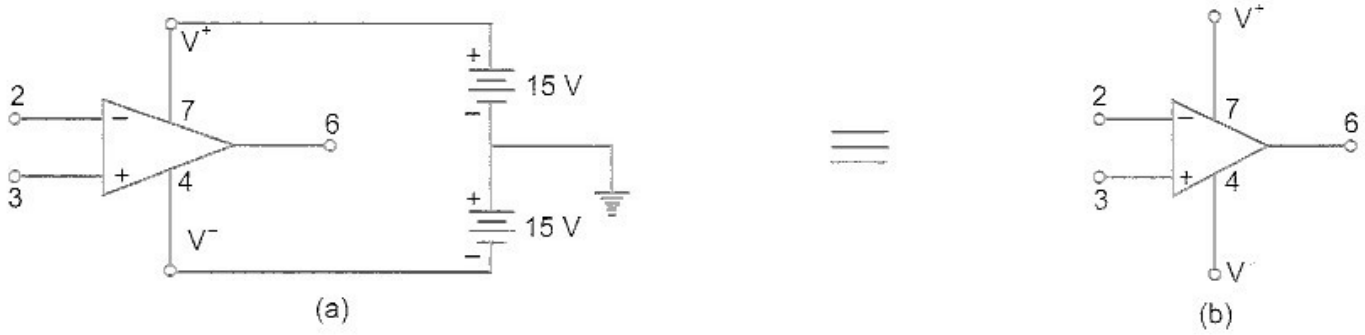


(c) 14 pin dual in-line package (d) 10 pin flat pack

Fig. 2.2 (a, b, c, d) Various IC packages of $\mu A741$ op-amp along with connection diagrams (top view)

Power Supply Connections

The V^+ and V^- power supply terminals are connected to two dc voltage sources. The V^+ pin is connected to the positive terminal of one source and the V^- pin is connected to the negative terminal of the other source as illustrated in Fig. 2.3 (a) where the two sources are 15 V batteries each. These are typical values, but in general, the power supply voltage may range from about ± 5 V to ± 22 V. The common terminal of the V^+ and V^- sources is connected to a reference point or ground. Some op-amps have a ground terminal, but most do not. The ground is simply a convenient point on the circuit bread-board to which the op-amp is connected through the power supplies. The equivalent representation of Fig. 2.3 (a) is given in Fig. 2.3 (b). The common point of the two supplies must be grounded, otherwise twice the supply voltage will get applied and it may damage the op-amp. Instead of using two power



(Fig. 2.3 Contd.)

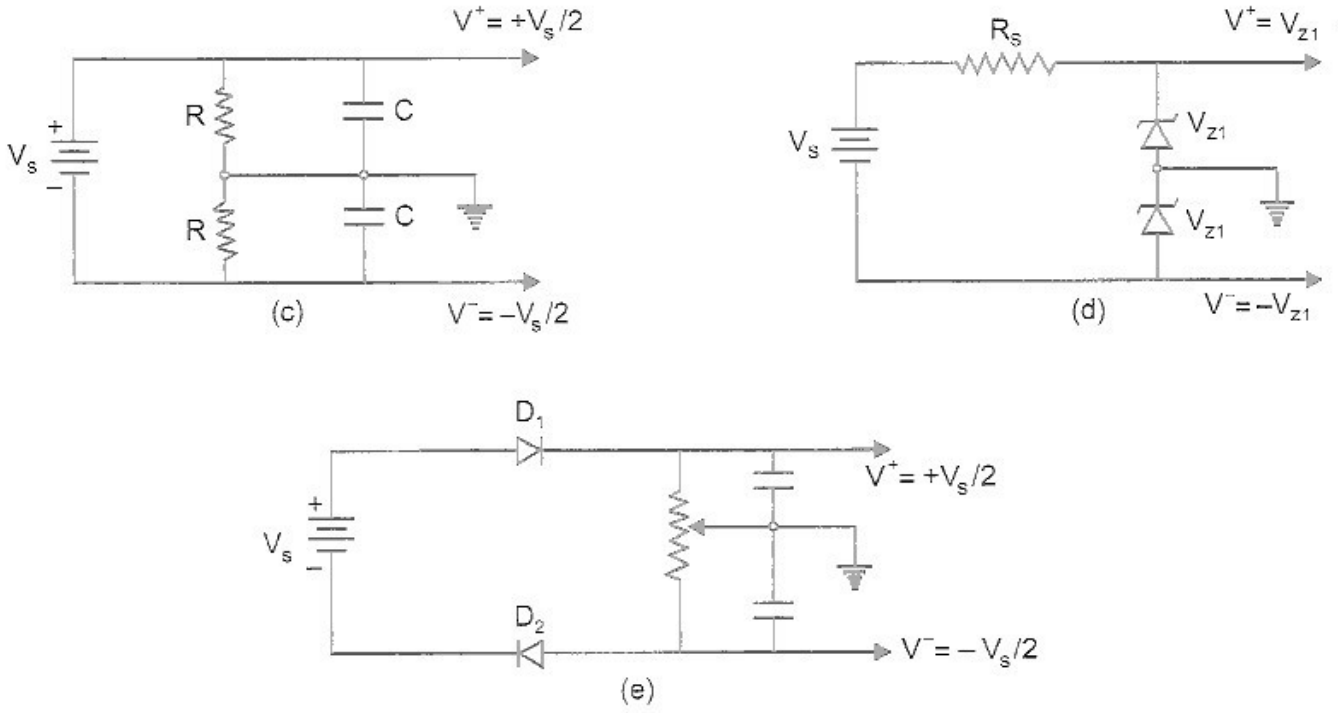


Fig. 2.3 (a) Power supply connections, (b) Circuit symbol showing power supply terminals (c, d, e) Different circuits for obtaining positive and negative supply voltages for op-amp

supplies, one can use a single power supply to obtain V^+ and V^- as shown in circuits of Fig. 2.3 (c, d, e). In Fig. 2.3 (c), resistor R should be greater than 10 kΩ so that it does not draw more current from the supply V_s. The two capacitors provide decoupling of the power supply and range in value from 0.01 to 10 μF. In the circuit of Fig. 2.3 (d), zener diodes are used to give symmetrical supply voltages. The value of the resistor R_s is chosen such that it supplies sufficient current for the zener diodes to operate in the avalanche mode. In Fig. 2.3 (e), potentiometer is used to get equal values of V^+ and V^-. Diodes D_1 and D_2 protect the IC if the positive and negative leads of the supply voltage V_s are accidentally reversed. These diodes can also be connected in the circuits of Fig. 2.3 (c) and 2.3 (d).

Manufacturer's Designation for Linear ICs

Each manufacturer uses a specific code and assigns a specific type number to the ICs produced. For example, 741 an internally compensated op-amp originally manufactured by Fairchild is sold as μA741. Here μA represents the identifying initials used by Fairchild. The codes used by some of the well-known manufacturers of linear ICs are:

(1)	Fairchild	μA, μAF
(2)	National Semiconductor	LM, LH, LF, TBA
(3)	Motorola	MC, MFC
(4)	RCA	CA, CD
(5)	Texas Instruments	SN
(6)	Signetics	N/S, NE/SE
(7)	Burr-Brown	BB

A number of manufacturers also produce popular ICs of the other manufacturers. For easy use, they usually retain the original type number of the IC alongwith their identifying

initials. For example, Fairchild's original μA741 is also manufactured by other manufacturers as follows:

(1)	National Semiconductor	LM741
(3)	Motorola	MC1741
(4)	RCA	CA3741
(5)	Texas Instruments	SN52741
(6)	Signetics	N5741

It may be noted that the last three digits in each manufacturer's designation are 741. All these op-amps have the same specifications. Since a number of manufacturers produce the same IC, one can refer to such ICs by their type number only and delete manufacturer's identifying initials. For example, μA741 or MC1741 may simple be referred as 741.

Some linear ICs are available in different classes such as A, C, E, S and SC. For example 741, 741A, 741C, 741E, 741S and 741SC are different versions of the same op-amp. The main difference of these op-amps are:

741	Military grade op-amp (Operating temperature range –55° to 125°C)	
741C	Commercial grade op-amp (Operating temperate range 0° to 70°/75°C)	
741A	Improved version of 741	Better electrical
741E	Improved version of 741C	specifications
741S	Military grade op-amp with higher slew-rate	
741SC	Commercial grade op-amp with higher slew-rate	

2.3 THE IDEAL OPERATIONAL AMPLIFIER

The schematic symbol of an op-amp is shown in Fig. 2.4 (a). It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The – and + symbols at the input refer to inverting and non-inverting input terminals respectively, i.e. if $v_1 = 0$, output v_o is 180° out of phase with input signal v_2. And, when $v_2 = 0$, output v_o will

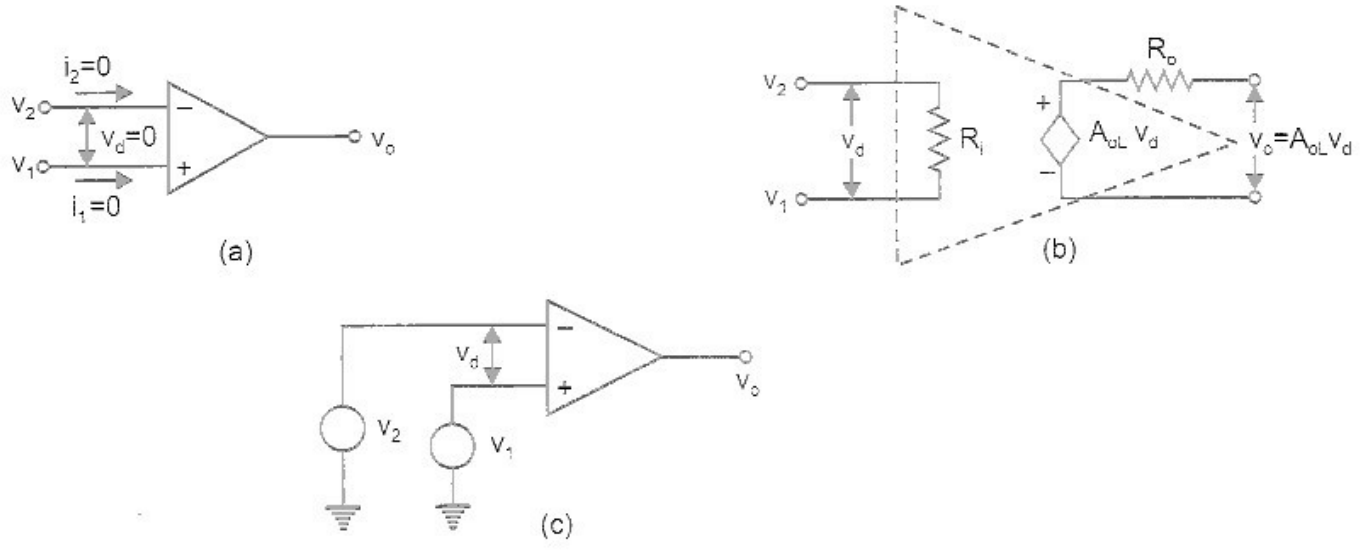


Fig. 2.4 (a) Ideal op-amp, (b) Equivalent circuit of an op-amp (c) Open loop circuit

be in phase with the input signal applied at v_1. This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain,	A_{OL}	=	∞
Input impedance,	R_i	=	∞
Output impedance	R_o	=	0
Bandwidth	BW	=	∞

Zero offset, i.e. $v_o = 0$ when $v_1 = v_2 = 0$.

It can be seen that

(i) an ideal op-amp draws no current at both the input terminals i.e., $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

(ii) Since gain is ∞, the voltage between the inverting and non-inverting terminals, i.e., differential input voltage $v_d = (v_1 - v_2)$ is essentially zero for finite output voltage v_o.

(iii) The output voltage v_o is independent of the current drawn from the output as $R_o = 0$. The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an 'Ideal op-amp' model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

A physical amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 2.4 (b) where $A_{OL} \neq \infty$, $R_i \neq \infty$ and $R_o \neq 0$. It can be seen that op-amp is a voltage controlled voltage source and $A_{OL}\, v_d$ is an equivalent *Thevenin* voltage source and R_o is the *Thevenin* equivalent resistance looking back into the output terminal of an op-amp. The equivalent circuit is useful in analyzing the basic operating principles of op-amp. For the circuit shown in Fig. 2.4 (b), the output voltage is

$$v_o = A_{OL}\, v_d$$

$$= A_{OL}\, (v_1 - v_2) \qquad (2.1)$$

The equation shows that the op-amp amplifies the difference between the two input voltages.

2.3.1 Open Loop Operation of Op-Amp

The simplest way to use an op-amp is in the open loop mode. Refer to Fig. 2.4 (c) where signals v_1 and v_2 are applied at non-inverting and inverting input terminals respectively. Since the gain is infinite, the output voltage v_o is either at its positive saturation voltage $(+V_{sat})$ or negative saturation voltage $(-V_{sat})$ as $v_1 > v_2$ or $v_2 > v_1$ respectively. The output assumes one of the two possible output states, that is, $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only. This has a limited number of applications such as voltage comparator, zero crossing detector etc. which are discussed later.

2.3.2 Feedback in Ideal Op-Amp

The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

Two Important Negative Feedback Circuits

There are two basic feedback connections used. In order to understand the operation of these circuits, we make two realistic simplifying assumptions discussed earlier also.

1. The current drawn by either of the input terminals (non-inverting and inverting) is negligible.
2. The differential input voltage v_d between non-inverting and inverting input terminals is essentially zero.

2.3.3 The Inverting Amplifier

This is perhaps the most widely used of all the op-amp circuits. The circuit is shown in Fig. 2.5 (a). The output voltage v_o is fed back to the inverting input terminal through the $R_f - R_1$ network where R_f is the feedback resistor. Input signal v_i (ac or dc) is applied to the inverting input terminal through R_1 and non-inverting input terminal of op-amp is grounded.

Analysis: For simplicity, assume an ideal op-amp. As $v_d = 0$, node 'a' is at ground potential and the current i_1 through R_1 is

$$i_1 = \frac{v_i}{R_1} \tag{2.2}$$

Also since op-amp draws no current, all the current flowing through R_1 must flow through R_f. The output voltage,

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1} \tag{2.3}$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1} \tag{2.4}$$

Alternatively, the nodal equation at the node 'a' in Fig. 2.5 (a) is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where v_a is the voltage at node 'a'. Since node 'a' is at virtual ground $v_a = 0$. Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

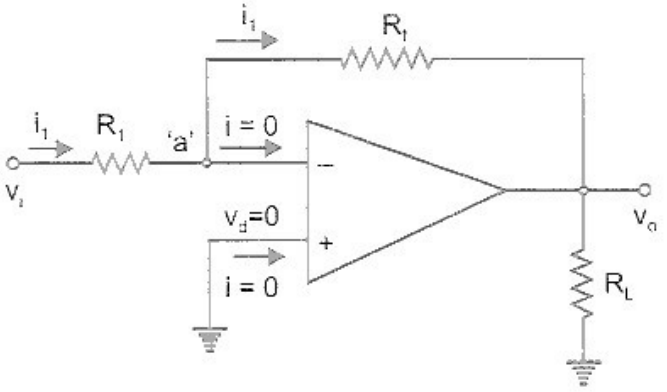


Fig. 2.5 (a) Inverting amplifier

The negative sign indicates a phase shift of 180° between v_i and v_o. Also since inverting input terminal is at virtual ground, the effective input impedance is R_1. The value of R_1 should be kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit. A load resistor R_L is usually put at the output in actual practice

otherwise, the input impedance of the measuring device such as oscilloscope or DVM acts as the load. The calculation of load and output currents is shown in the Example 2.2.

If, however, resistances R_1 and R_f in Fig. 2.5 (a) are replaced by impedances Z_1 and Z_f respectively, then the voltage gain, A_{CL} will be

$$A_{CL} = -\frac{Z_f}{Z_1} \tag{2.5}$$

This expression for the voltage gain will be used in op-amp applications, such as integrator, differentiator etc.

Example 2.1

Design an amplifier with a gain of –10 and input resistance equal to 10 kΩ.

Solution

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

In Fig. 2.5 (a) choose $R_1 = 10$ kΩ

Then $R_f = -A_{CL} R_1$ (from Eq. 2.4)

$= -(-10) \times 10\ \text{k}\Omega = 100\ \text{k}\Omega$

Example 2.2

In Fig. 2.5 (b), $R_1 = 10$ kΩ, $R_f = 100$ kΩ, $v_i = 1$ V. A load of 25 kΩ is connected to the output terminal. Calculate (i) i_1 (ii) v_o (iii) i_L and (iv) total current i_o into the output pin.

Solution

(i) $i_1 = \dfrac{v_i}{R_1} = \dfrac{1\ \text{V}}{10\ \text{k}\Omega} = 0.1\ \text{mA}$

(ii) $v_o = -\dfrac{R_f}{R_1} v_i = -\dfrac{100\ \text{k}\Omega}{10\ \text{k}\Omega} 1\ \text{V} = -10\ \text{V}$

(iii) $i_L = \dfrac{v_o}{R_L} = \dfrac{10\ \text{V}}{25\ \text{k}\Omega} = 0.4\ \text{mA}$

The direction of i_L is shown in Fig. 2.5 (b).

(iv) i_1 as calculated above is 0.1 mA. Therefore, total current $i_o = i_1 + i_L$ = 0.1 mA + 0.4 mA = 0.5 mA. In an inverting amplifier, for a + ive input, output will be –ive, therefore the direction of i_o is as shown in Fig. 2.5 (b).

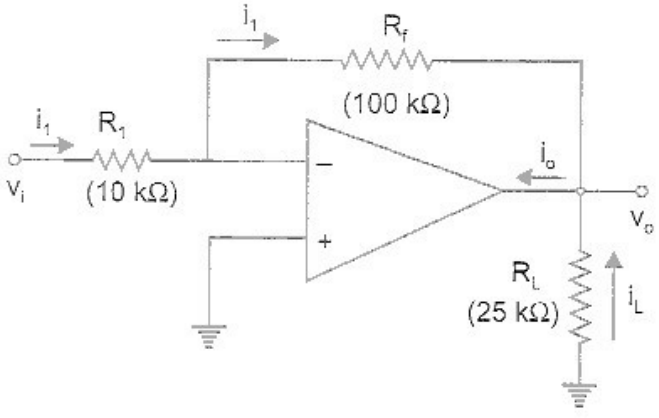


Fig. 2.5 (b) Circuit for Example 2.2

Practical Inverting Amplifier

Equation (2.4) is valid only if the op-amp is an ideal one. For a practical op-amp, the expression for the closed loop voltage gain should be calculated using the low frequency model of Fig. 2.4 (b). The equivalent circuit of a practical inverting amplifier is shown in Fig. 2.6 (a). This circuit can be simplified by replacing the signal source v_i and resistors R_1 and R_i by Thevenin's equivalent as shown in Fig. 2.6 (b) which is analysed to calculate the exact expression for closed loop gain, A_{CL} and input impedance R_{if}.

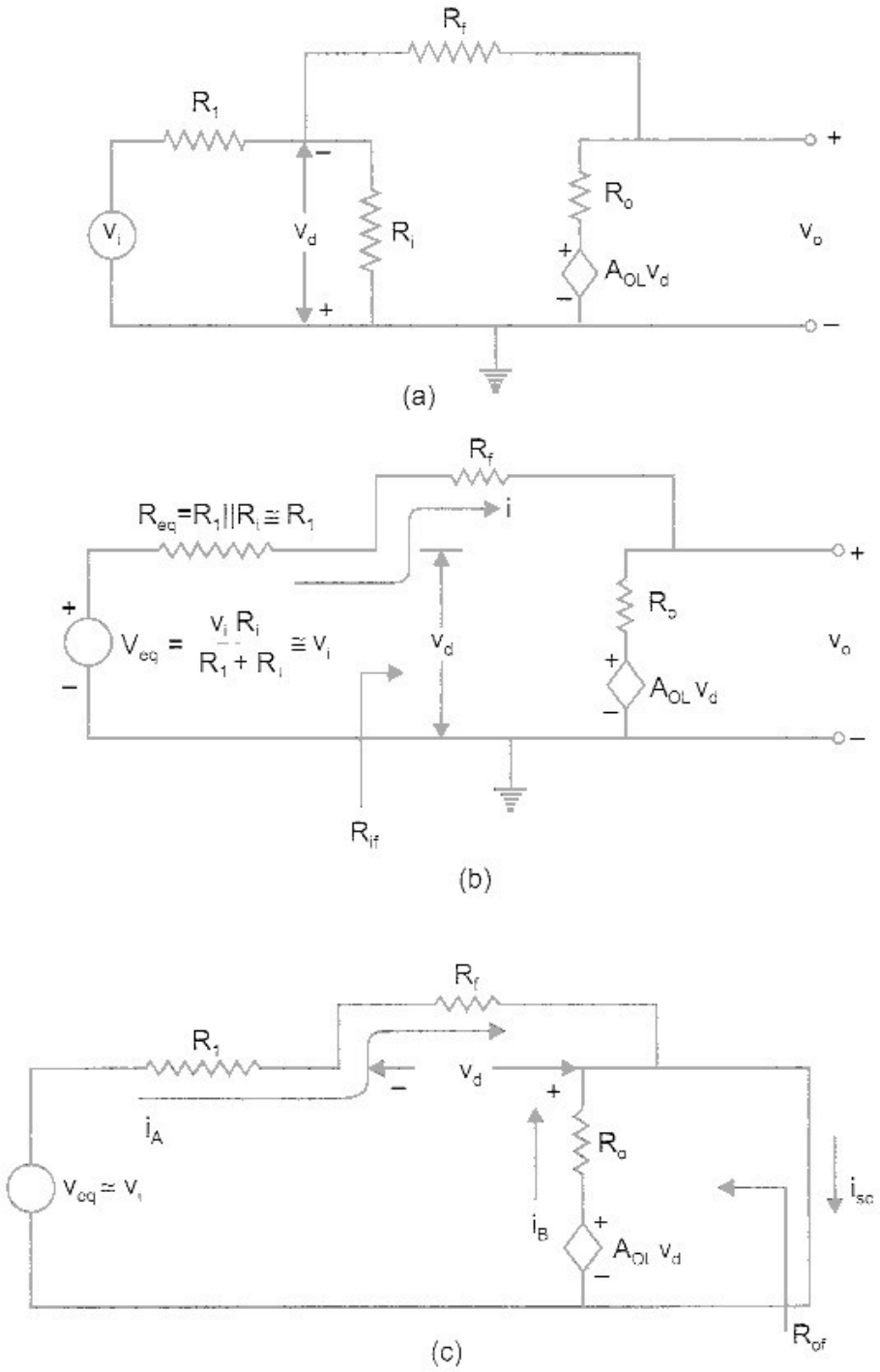


Fig. 2.6 (a) Equivalent circuit of a practical op-amp inverting amplifier, (b) Simplified circuit by using Thevenin's equivalent (c) Equivalent circuit for computing R_{of}

The input impedance R_i of an op-amp is usually much greater than R_1, so one may assume, $v_{eq} \cong v_i$ and $R_{eq} \cong R_1$.

From the output loop in Fig. 2.6 (b)

$$v_o = iR_o + A_{OL}\, v_d \tag{2.6}$$

Also

$$v_d + iR_f + v_o = 0 \tag{2.7}$$

Putting the value of v_d from Eq. (2.6) to Eq. (2.7) and simplifying,

$$v_o(1 + A_{OL}) = i(R_o - A_{OL}\, R_f) \tag{2.8}$$

Also the KVL loop equation gives

$$v_i = i(R_1 + R_f) + v_o \tag{2.9}$$

Putting the value of i from Eq. (2.8) in Eq. (2.9) and solving for closed loop gain $A_{CL} = \frac{v_o}{v_i}$, gives

$$A_{CL} = \frac{v_o}{v_i} = \frac{R_o - A_{OL} R_f}{R_o + R_f + R_1 (1 + A_{OL})} \tag{2.10}$$

It can be seen from Eq. (2.10) that if $A_{OL} >> 1$ and $A_{OL} R_1 >> R_o + R_f$, and neglecting R_o,

$$A_{CL} \cong -\frac{R_f}{R_1}.$$

Input Resistance R_{if}

In Fig. 2.6 (b), it can be seen that

$$R_{if} = \frac{v_d}{i}$$

Writing the loop equation and solving for R_{if},

$$v_d + i (R_f + R_o) + A_{OL} v_d = 0$$

We obtain

$$R_{if} = \frac{R_f + R_o}{1 + A_{OL}} \tag{2.11}$$

Output Resistance R_{of}

Output impedance R_{of} (without load resistance R_L) is calculated from the open circuit output voltage v_{oc} and short circuit output circuit i_{sc}. Now consider the circuit shown in Fig. 2.6 (c). Under short circuit conditions at output,

$$i_A = \frac{v_i - 0}{R_1 + R_f} \tag{2.12}$$

and,

$$i_B = \frac{A_{OL} v_d}{R_o} \tag{2.13}$$

Since $v_d = -i_A R_f$

So, $$i_B = -\frac{A_{OL} i_A R_f}{R_o}$$

Solving for $i_{sc} = i_A + i_B$, we obtain

$$i_{sc} = i_A + i_B = v_i \frac{(R_o - A_{OL} R_f)}{R_o (R_1 + R_f)} \tag{2.14}$$

Since

$$R_{of} = \frac{v_{oc}}{i_{sc}}$$

and $$A_{CL} = \frac{v_{oc}}{v_i}$$

Therefore, $$R_{of} = \frac{A_{CL}\, v_i}{v_i \left[(R_o - A_{OL}\, R_f) \Big/ R_o (R_1 + R_f) \right]} \tag{2.15}$$

Putting the value of A_{CL} from Eq. (2.10), we obtain

$$R_{of} = \frac{R_o (R_1 + R_f)}{R_o + R_f + R_1 (1 + A_{OL})} \tag{2.16}$$

Equation (2.16) may alternatively be written as

$$R_{of} = \frac{\dfrac{R_o (R_1 + R_f)}{R_o + R_1 + R_f}}{1 + \dfrac{R_1 A_{OL}}{R_o + R_1 + R_f}} \tag{2.17}$$

It may be seen that numerator consists of a term $R_o \,||\, (R_1 + R_f)$ and is therefore smaller than R_o. The output resistance R_{of} (with feedback) is, therefore always less than R_o and for $A_{CL} \to \infty$, $R_{of} \to 0$.

2.3.4 The Non-Inverting Amplifier

If a signal (ac or dc) is applied to the non-inverting input terminal and feedback is given as shown in Fig. 2.7 (a), the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.

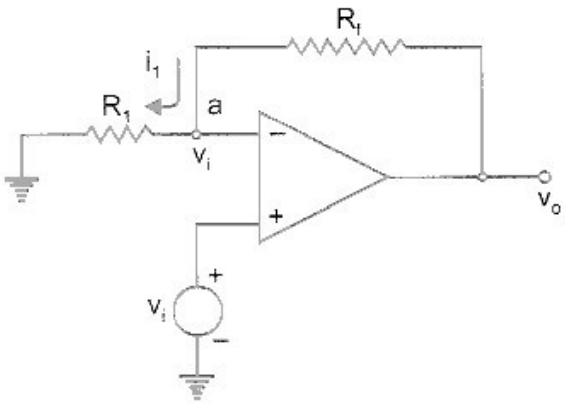


Fig. 2.7 (a) Non-inverting amplifier

As the differential voltage v_d at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 2.7 (a) 5is v_i, same as the input voltage applied to non-inverting input terminal. Now R_f and R_1 forms a potential divider. Hence

$$v_i = \frac{v_o}{R_1 + R_f} R_1 \tag{2.18}$$

as no current flows into the op-amp.

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \tag{2.19}$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1} \tag{2.20}$$

The gain can be adjusted to unity or more, by proper selection of resistors R_f and R_1. Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large (= ∞) as the op-amp draws negligible current from the signal source.

Practical Non-Inverting Amplifier

The analysis of a practical non-inverting amplifier can be performed by using the equivalent circuit shown in Fig. 2.7 (b). Writing KCL at the input node,

$$(v_i - v_d)\,Y_1 + v_d Y_i + (v_i - v_d - v_o)Y_f = 0$$

or,
$$-(Y_1 + Y_i + Y_f)\,v_d + (Y_1 + Y_f)\,v_i = Y_f v_o \tag{2.21}$$

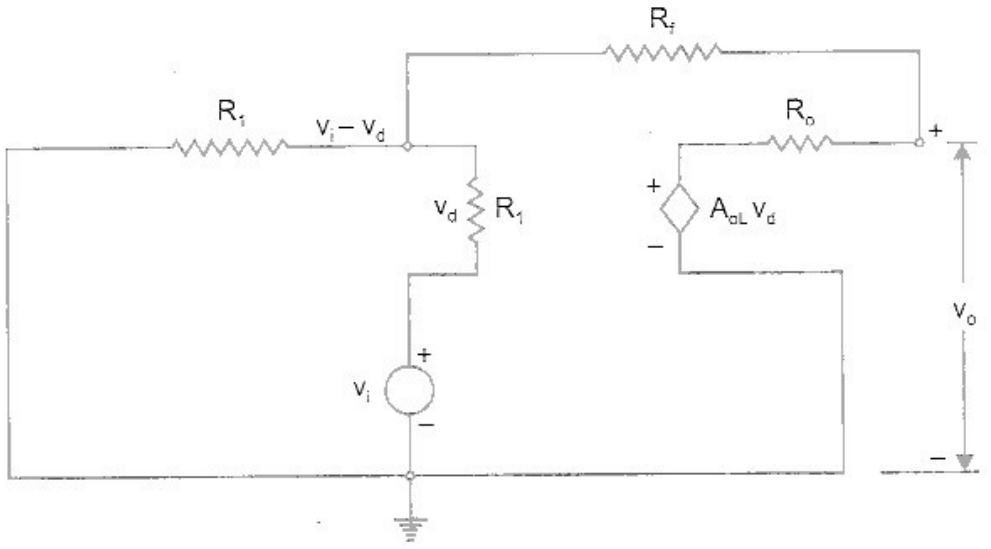


Fig. 2.7 (b) Equivalent circuit of non-inverting amplifier using low frequency model

Similarly at output node, KCL gives

$$(v_i - v_d - v_o)Y_f + (A_{OL}\,v_d - v_o)Y_o = 0$$

that is,
$$-(Y_f - A_{OL}\,Y_o)\,v_d + Y_f v_i = (Y_f + Y_o)\,v_o \tag{2.22}$$

Now solving Eqs. (2.21) and (2.22) for v_o/v_i, we get

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL}Y_o(Y_1+Y_f)+Y_fY_i}{(A_{OL}+1)Y_oY_f+(Y_1+Y_i)(Y_f+Y_o)} \tag{2.23}$$

where all admittances have been taken for simplicity.

If $A_{OL} \to \infty$, Eq. (2.23) reduces to

$$A_{CL} \approx \frac{A_{OL}Y_o(Y_1+Y_f)}{A_{OL}Y_oY_f} = \frac{Y_1+Y_f}{Y_f} = 1+\frac{Y_1}{Y_f}$$

$$= 1+\frac{R_f}{R_1}$$

which is the same expression as in Eq. (2.20).

2.3.5 Voltage Follower

In the non-inverting amplifier of Fig. 2.7 (a) if $R_f = 0$ and $R_1 = \infty$, we get the modified circuit of Fig. 2.7 (c). From Eq. (2.20) we get,

$$v_o = v_i \tag{2.24}$$

That is, the output voltage is equal to input voltage, both in magnitude and phase. In other words, we can also say that the output voltage follows the input voltage exactly. Hence, the circuit is called a voltage follower. The use of the unity gain circuit lies in the fact that its input impedance is very high (i.e. MΩ order) and output impedance is zero. Therefore, it draws negligible current from the source. Thus a voltage follower may be used as buffer for impedance matching, that is, to connect a high impedance source to a low impedance load.

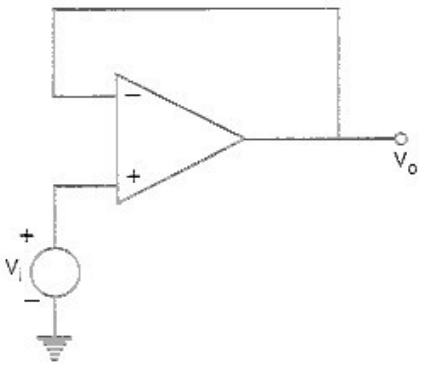


Fig. 2.7 (c) Voltage follower

Example 2.3

Design an amplifier with a gain of +5 using one op-amp.

Solution

Since the gain is positive, we have to make a non-inverting amplifier. In Fig. 2.7 (a) select R_1 = 10 kΩ. Then from Eq. (2.20)

$$A_{CL} = 1 + R_f/R_1$$

or, $$5 = 1 + R_f/10\ \text{k}\Omega$$

or, $$R_f = 4 \times 10\ \text{k}\Omega = 40\ \text{k}\Omega$$

Example 2.4

In the circuit of Fig. 2.7 (a), let R_1 = 5 kΩ, R_f = 20 kΩ and v_i = 1 V. A load resistor of 5 kΩ is connected at the output as in Fig. 2.5 (b). Calculate, (i) v_o (ii) A_{CL} (iii) the load current i_L (iv) the output current i_o indicating proper direction of flow.

Solution

(i) $$v_o = \left(1 + \frac{R_f}{R_1}\right) v_i = \left(1 + \frac{20\ \text{k}\Omega}{5\ \text{k}\Omega}\right)(1\ \text{V}) = 5\ \text{V}$$

(ii) $$A_{CL} = \frac{v_o}{v_i} = \frac{5\ \text{V}}{1\ \text{V}} = 5$$

(iii) $$i_L = \frac{v_o}{R_L} = \frac{5\ \text{V}}{5\ \text{k}\Omega} = 1\ \text{mA}$$

(iv) $$i_1 = \frac{v_i}{R_1} = \frac{v_o - v_i}{R_f} = 0.2\ \text{mA}$$

Therefore, $i_o = i_L + i_1 = 1\text{ mA} + 0.2\text{ mA} = 1.2\text{ mA}$

The op-amp output current i_o flows outwards from the output junction.

2.3.6 Differential Amplifier

A circuit that amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits (see section 4.3). A typical circuit is shown in Fig. 2.8. Since, the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at the same potential, designated as v_3. The nodal equation at 'a' is,

$$\frac{v_3 - v_2}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \qquad (2.25)$$

and at 'b' is

$$\frac{v_3 - v_1}{R_1} + \frac{v_3}{R_2} = 0 \qquad (2.26)$$

Rearranging, we get

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_2}{R_1} = \frac{v_o}{R_2} \qquad (2.27)$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_1}{R_1} = 0 \qquad (2.28)$$

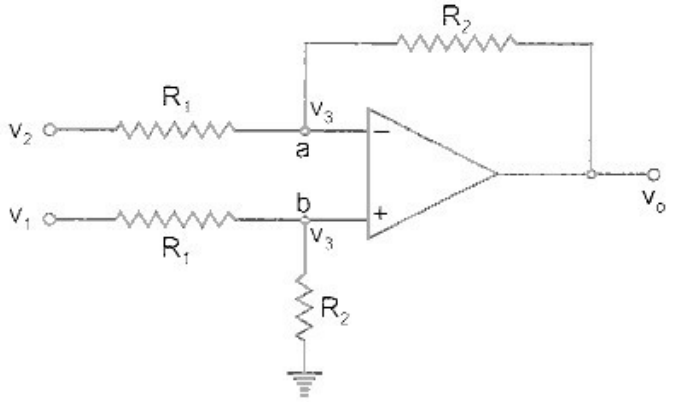


Fig. 2.8 A differential amplifier

Subtracting Eq. (2.28) from (2.27) we get,

$$\frac{1}{R_1}(v_1 - v_2) = \frac{v_o}{R_2} \qquad (2.29)$$

Therefore,

$$v_o = \frac{R_2}{R_1}(v_1 - v_2) \qquad (2.30)$$

Such a circuit is very useful in detecting very small differences in signals, since the gain R_2/R_1 can be chosen to be very large. For example, if $R_2 = 100\ R_1$, then a small difference $v_1 - v_2$ is amplified 100 times.

Difference-mode and Common-mode Gains

In Eq. (2.30) if $v_1 = v_2$ then $v_o = 0$. That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-amp, however, a practical op-amp exhibits some small response to the common mode component of the input voltages too. For example, the output v_o will have different value for case (i) with $v_1 = 100\ \mu V$ and $v_2 = 50\ \mu V$ and case (ii) with $v_1 = 1000\ \mu V$ and $v_2 = 950\ \mu V$, even though the difference signal $v_1 - v_2 = 50\ \mu V$ in both the cases. The output voltage depends not only upon the difference signal v_d at the input, but is also affected by the average voltage of the input signals, called the common-mode signal v_{CM} defined as,

$$v_{CM} = \frac{v_1 + v_2}{2}$$

For differential amplifier, though the circuit is symmetric, but because of the mismatch, the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. So, even with the same voltage applied to both inputs, the output is not zero. The output, therefore, must be expressed as,

$$v_o = A_1 v_1 + A_2 v_2 \tag{2.31}$$

where, A_1 (A_2) is the voltage amplification from input 1 (2) to the output with input 2(1) grounded. Since $v_{CM} = (v_1 + v_2)/2$ and $v_d = (v_1 - v_2)$,

$$v_1 = v_{CM} + \frac{1}{2} v_d \tag{2.32}$$

and

$$v_2 = v_{CM} - \frac{1}{2} v_d \tag{2.33}$$

Substituting the value of v_1 and v_2 in Eq. (2.31), we get

$$v_o = A_{DM} v_d + A_{CM} v_{CM} \tag{2.34}$$

where,

$$A_{DM} = \frac{1}{2}(A_1 - A_2) \tag{2.35}$$

and

$$A_{CM} = A_1 + A_2 \tag{2.36}$$

The voltage gain for the difference signal is A_{DM} and that for the common-mode signal is A_{CM}.

2.3.7 Common-mode Rejection Ratio

The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit ρ for the differential amplifier. So, CMRR is given by:

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right| \tag{2.37}$$

and is usually expressed in decibels (dB). For example, the μA741 op-amp has a minimum CMRR of 70 dB whereas a precision op-amp such as μA725A has a minimum CMRR of 120 dB. Clearly, we should have A_{DM} large A_{CM} should be zero ideally. So, higher the value of CMRR, better is the op-amp.

Example 2.5

In Fig. 2.9 is shown a differential amplifier using ideal op-amp.

(a) Find the output voltage v_o.

(b) Show that the output corresponding to common-mode voltage

$v_{CM} = \dfrac{(v_1 + v_2)}{2}$ is zero if $\dfrac{R'}{R} = \dfrac{R_2}{R_1}$.

Find v_o in this case.

(c) Find CMRR of the amplifier if $\dfrac{R'}{R} \neq \dfrac{R_2}{R_1}$.

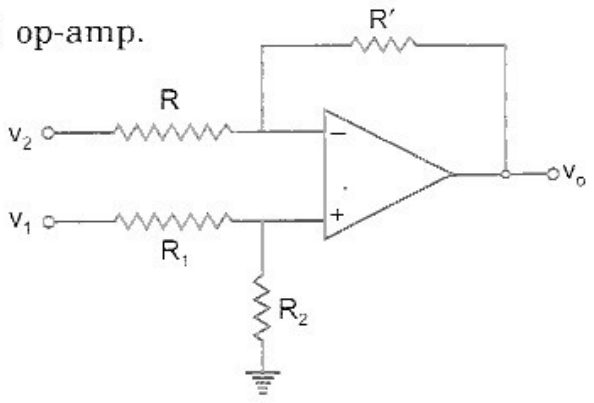


Fig. 2.9 Circuit of Example 2.5

Solution

The voltage at the non-inverting input terminal is $\frac{R_2}{R_1 + R_2} v_1$. Using principle of superposition and Eqs. (2.4) and (2.20), we have

(a) $$v_o = -\frac{R'}{R} v_2 + \left(\frac{R + R'}{R}\right)\left(\frac{R_2}{R_1 + R_2} v_1\right) \tag{2.38}$$

(b) $$v_{CM} = \frac{1}{2}(v_1 + v_2) \text{ and } v_d = (v_1 - v_2)$$

So, $$v_1 = v_{CM} + \frac{v_d}{2} \text{ and } v_2 = v_{CM} - \frac{v_d}{2}$$

v_o from Eq. (2.38) is,

$$v_o = -\frac{R'}{R}\left(v_{CM} - \frac{v_d}{2}\right) + \frac{R_2}{R}\frac{R + R'}{R_1 + R_2}\left(v_{CM} + \frac{v_d}{2}\right)$$

$$= \left(\frac{R_2}{R}\frac{R + R'}{R_1 + R_2} - \frac{R'}{R}\right) v_{CM} + \left(\frac{R'}{R} + \frac{R_2}{R}\frac{R + R'}{R_1 + R_2}\right)\frac{v_d}{2} \tag{2.39}$$

Now, if $\frac{R'}{R} = \frac{R_2}{R_1}$, we get,

$$\frac{R'}{R} + 1 = \frac{R_2}{R_1} + 1$$

or, $$\frac{R' + R}{R} = \frac{R_1 + R_2}{R_1}$$

So, from Eq. (2.39) the term corresponding to v_{CM} is zero, and

$$v_o = \left(\frac{R'}{R} + \frac{R_2}{R_1}\right)\frac{v_d}{2} = \left(\frac{R_2}{R_1}\right) v_d \tag{2.40}$$

(c) $$\text{CMRR} = \frac{A_{DM}}{A_{CM}}$$

From Eq. (2.39), find (i) $A_{DM} = v_o/v_d$ by putting $v_{CM} = 0$

and (ii) $A_{CM} = v_o/v_{CM}$ by putting $v_d = 0$

then we get

$$\text{CMRR} = \frac{R'(R_1 + R_2) + R_2(R + R')}{R'(R_1 + R_2) - R_1(R + R')} \tag{2.41}$$

2.4 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

Commercial IC op-amps usually consists of four cascaded blocks as shown in Fig. 2.10. The first two stages are cascaded differential amplifiers and are designed to provide high gain and high input resistance. The third stage acts as a buffer as well as a level shifter. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage. The level shifter adjusts the d.c. voltages so that output voltage is zero for zero inputs. The adjustment of d.c. level is required as the gain stages are direct coupled. As it is not possible to fabricate large value of capacitors, all IC's are direct coupled usually. The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics. The output voltage should swing symmetrically with respect to ground. To allow such symmetrical swing, the amplifier is provided with both positive and negative supply voltages. Power supply voltages of ± 15V are common. Additionally, an op-amp generally incorporates circuitry to provide drift compensation and frequency compensation which are discussed in sec. 3.3.3.

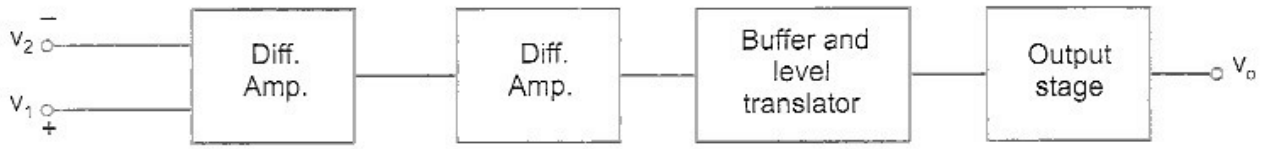


Fig. 2.10 Block schematic of an op-amp

Before describing the detailed IC circuit, we shall discuss each of the blocks in detail.

2.4.1 Differential Amplifier

The main purpose of the differential amplifier stage is to provide high gain to the difference-mode signal and cancel the common-mode signal. Thus, it is able to suppress any undesired noise which is common to both of the input terminals. The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit of the differential amplifier. The higher the value of CMRR, better is the op-amp. Another requisite of a good op-amp is that it should have high input impedance. In this section, we discuss in detail, the various circuits and then modifications to achieve these characteristics of a good op-amp.

A cascaded direct coupled amplifier can provide high gain down to zero frequency as it has no coupling capacitor. However, such an amplifier suffers from the major problem of drift of the operating point due to temperature dependency of I_{CO}, V_{BE} and h_{FE} of the transistor. This problem can be eliminated by using a balanced or differential amplifier as shown in Fig. 2.11 (a). It may be seen that it is essentially an emitter-coupled differential amplifier. This circuit has low drift on account of symmetrical construction. It can be designed to give high input resistance. It has two input terminals and it may be seen easily that terminal B_2 is the inverting input terminal since transistor Q_2 provides a phase shift of 180° for the output taken at the collector of Q_2. Obviously, B_1 is the non-inverting input terminal. So, a differential amplifier is well suited to obtain the ideal characteristics of an op-amp as discussed in Sec. 2.3.

A differential amplifier of the type shown in Fig. 2.11 (a) can be used in four different configurations depending upon the number of input signals used and the way output is taken. These four configurations are:

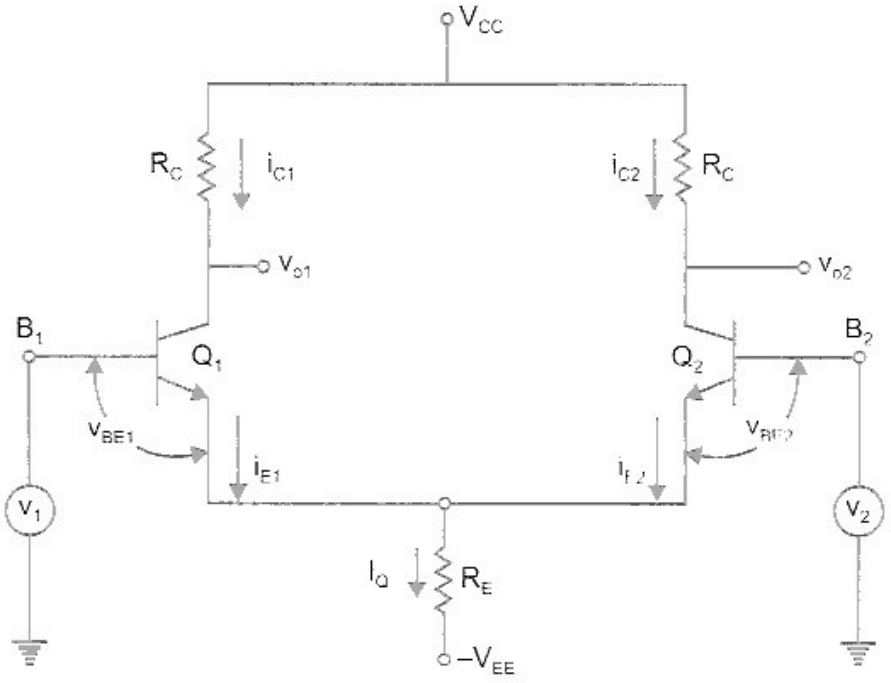


Fig. 2.11 (a) The basic differential amplifier

(i) Differential-input, differential-output or Dual-input balanced-output (ii) Differential-input, single ended-output (iii) Single-input, differential-output (iv) Single-input, single ended-output.

If signal is applied to both the inputs, then it is differential input or Dual input and the difference of signals applied to the two inputs gets amplified. In many applications a single input is only used as we shall see later. Similarly, if output voltage is measured between two collectors then it is a differential output. This is also referred to as a balanced output, as both collectors are at the same d.c. potential w.r.t. ground. We will come across these various configuration as we proceed further.

To understand the working of a differential amplifier first consider the case when both the bases B_1 and B_2 are joined together and connected to a voltage v_{CM} called the common-mode voltage. Thus in Fig. 2.11 (b), $v_1 = v_2 = v_{CM}$. As both the transistors Q_1 and Q_2 are forward-

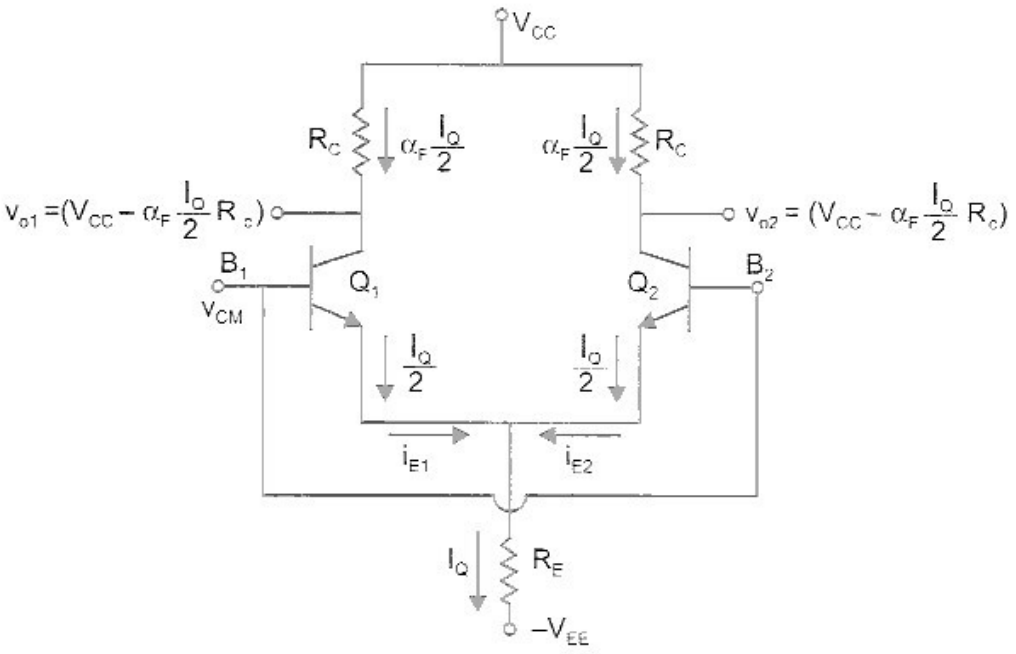


Fig. 2.11 (b) The differential pair with a common-mode input signal v_{CM}

biased and matched, due to symmetry of the circuit, the current I_Q divides equally through transistors Q_1 and Q_2, that is, $i_{E1} = i_{E2} = I_Q/2$. The collector currents i_{C1} and i_{C2} through the resistors R_C is $\alpha_F I_Q/2$. The voltage at each of the collectors will be $V_{CC} - \alpha_F \frac{I_Q}{2} R_C$ and, therefore the difference of the voltage between the two collectors $(v_{o1} - v_{o2})$ will be zero. Now, even if the value of v_{CM} is changed, the voltage across the collectors will not change. Thus, the differential pair does not respond to (or rejects) the common-mode input signals. Now, consider the case when the voltage v_2 is made zero and voltage $v_1 = 1$ V (say) as shown in Fig. 2.11 (c). It can be seen that the transistor Q_1 will conduct and transistor Q_2 will be **off**. The entire current I_Q will now flow through Q_1. Since Q_1 is **on**, the voltage at its emitter will be 0.3 V. This will make emitter-base junction of Q_2 reverse-biased and thus Q_2 will be **off**. The collector voltages will be $v_{o1} = V_{CC} - \alpha_F I_Q R_C$ and $v_{o2} = V_{CC}$.

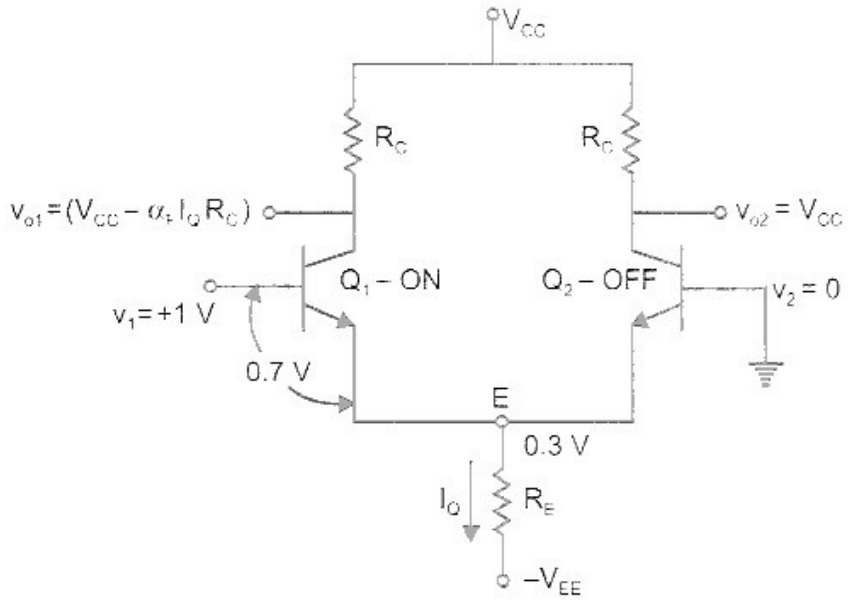


Fig. 2.11 (c) The differential pair with 'large' differential input signal

If, however, $v_1 = -1$ V and $v_2 = 0$ V, it can be seen that Q_1 will be **off** and the entire current I_Q will flow through Q_2. The voltage at the common emitter point 'E' will now be – 0.7 V which makes Q_1 **off** and Q_2 **on**. The collector voltages will be $v_{o1} = V_{CC}$ and $v_{o2} = V_{CC} - \alpha_F I_Q R_C$.

Thus, we see that the differential pair responds only to the difference mode signals and rejects common-mode signals. In the next section, we discuss the transfer characteristics of the circuit to show that a differential pair can be used either as a switch or a linear amplifier.

2.4.2 Transfer Characteristics

In Fig. 2.11 (a) collector currents i_{C1} and i_{C2} for transistors Q_1 and Q_2 biased in the forward-active mode may be given by (neglecting reverse saturation currents of the collector base junction)

$$i_{C1} = \alpha_F I_{ES}\, e^{v_{BE1}/V_T} \tag{2.42}$$

$$i_{C2} = \alpha_F I_{ES}\, e^{v_{BE2}/V_T} \tag{2.43}$$

Here, I_{ES} is the reverse saturation current of emitter-base junction and V_T is volts equivalent of temperature.

From Eqs. (2.42) and (2.43), we may write

$$\frac{i_{C1}}{i_{C2}} = e^{(v_{BE1} - v_{BE2})/V_T} \tag{2.44}$$

We may also write KVL for the loop containing two emitter-base junctions as

$$v_1 - v_{BE1} + v_{BE2} - v_2 = 0$$

or

$$v_{BE1} - v_{BE2} = v_1 - v_2 = v_d$$

where, v_d is the difference of two input voltages.

Also in Fig. 2.11 (a)

$$I_Q = i_{E1} + i_{E2} = \frac{i_{C1}}{\alpha_F} + \frac{i_{C2}}{\alpha_F}$$

$$= \frac{i_{C1}}{\alpha_F}\left(1 + \frac{i_{C2}}{i_{C1}}\right) \tag{2.45}$$

Using Eqs. (2.44) and (2.45) and solving for i_{C1} and i_{C2}, gives

$$i_{C1} = \frac{\alpha_F I_Q}{1 + e^{-v_d/V_T}} \tag{2.46}$$

$$i_{C2} = \frac{\alpha_F I_Q}{1 + e^{v_d/V_T}} \tag{2.47}$$

From Eqs. (2.46) and (2.47), the normalised transfer characteristics (i_C/I_Q vs v_d/V_T assuming $\alpha_F = 1$) for a differential amplifier are obtained as shown in Fig. 2.12.

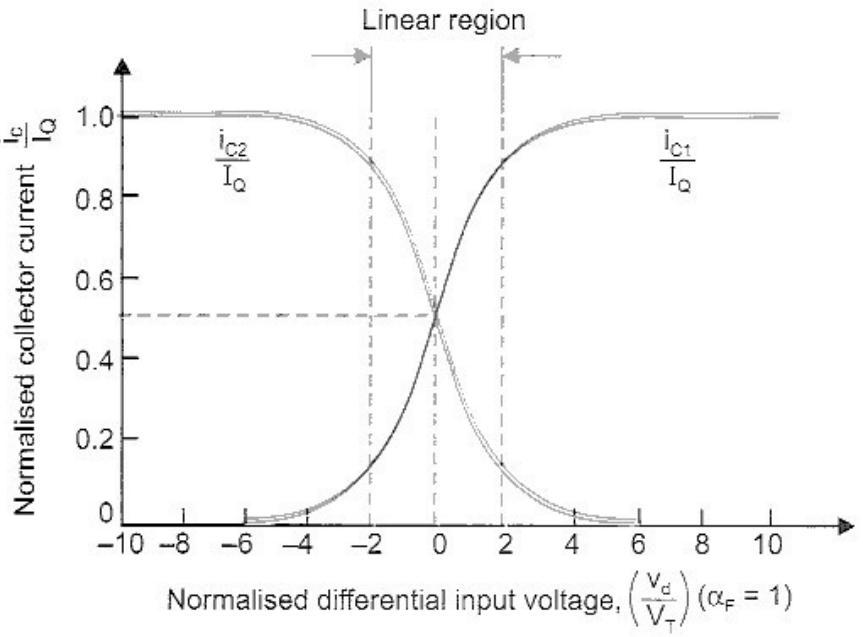


Fig. 2.12 Normalised transfer characteristics for the differential pair

The following important points are observed from the transfer characteristics:

1. For $v_d > 4\,V_T$ (~ 100 mV), $i_{C1} = \alpha_F I_Q$ and $i_{C2} = 0$, Hence