University Questions Solution

Part - B Unit - II

AARUPADAI VEEDU INSTITUTE OF TECHNOLOGY L.I.C Sheet No.

Q1. Explain the Working principle of RC phase Shift Oscillator with Neat Sketch.

Sol: The Circuit of an RC-phase Shift Oscillator is shown in fig. The op-amp is used in the inverting mode and therefore provides 180° phase Shift. The additional phase of 180° is provided by the RC feedback network to obtain a total phase Shift of 360°. The feedback network consists of three identical RC Stages Each of the RC Stage provides a 60° phase Shift so that the total phase Shift due to feedback network is 180° It is not necessary that all the three RC Sections are identical so long the total phase Shift is 180°. However if we use non-identical Stages. it is possible that the total phase Shift is 180° from more than one frequency. This phenomenon can led to undesirable inter-modal Oscillations.

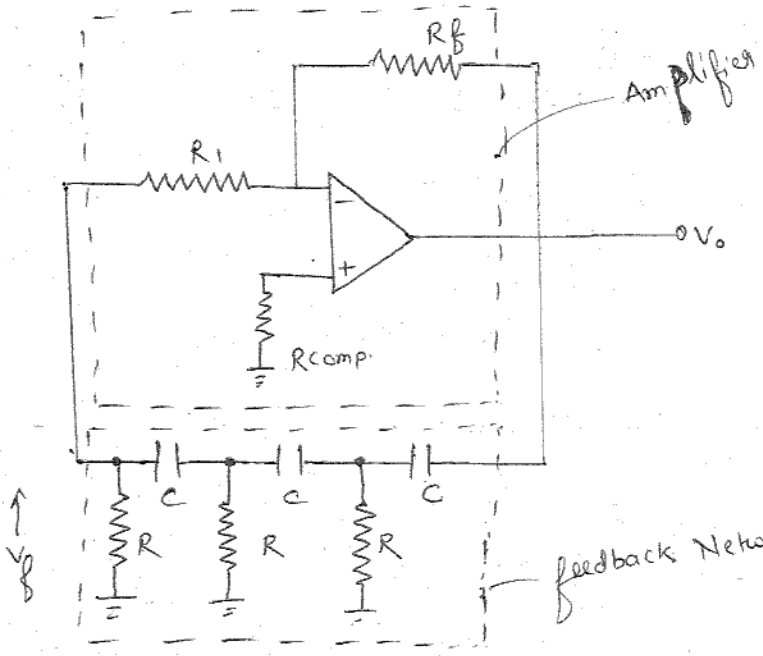
The feedback factor β of the RC network can be calculated by writing the KVL equations from fig.(b).

$$I_1\left(R + \frac{1}{sC}\right) - I_2 R = V_o \quad \text{——— (1)}$$

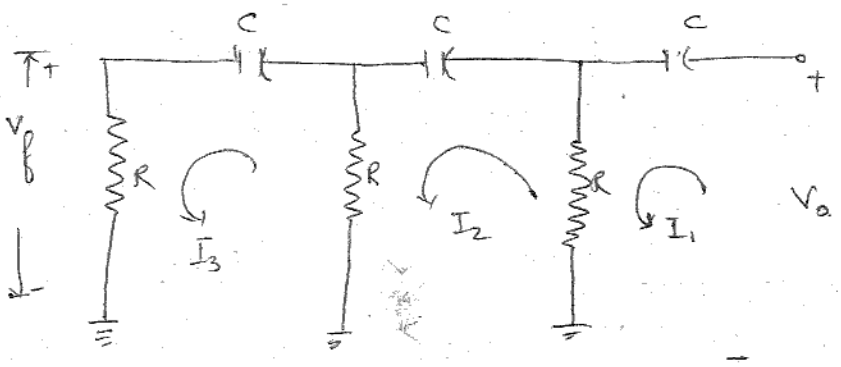
$$-I_1 R + I_2\left(2R + \frac{1}{sC}\right) - I_3 R = 0 \quad \text{——— (2)}$$

$$0 - I_2 R + I_3\left(2R + \frac{1}{sC}\right) = 6 \quad \text{——— (3)}$$

and $V_f = I_3 R$ ——— (4)



(a) Phase shift Oscillator



(b) Calculating β from the phase shift network

Solving Eq^n ① ② & ③ for I_3 we get.

$$I_3 = \frac{V_o R^2 s^3 C^3}{1 + 5sRC + 6s^2C^2R^2 + s^3C^3R^3} \quad \text{——— (5)}$$

and $$V_f = I_3 R = \frac{V_o R^3 s^3 C^3}{1 + 5sRC + 6s^2C^2R^2 + s^3C^3R^3} \quad \text{——— (6)}$$

$$= \frac{1}{1 + \frac{6}{sRC} + \frac{5}{s^2C^2R^2} + \frac{1}{s^3C^3R^3}} \quad \text{——— (7)}$$

Replacing $s = j\omega$, $s^2 = -\omega^2$ and $s^3 = -j\omega^3$ we get.

$$\beta = \frac{1}{1 - \frac{6}{j\omega RC} - \frac{5}{\omega^2 R^2 C^2} + \frac{1}{j\omega^3 R^3 C^3}} \quad \text{——— (8)}$$

$$= \frac{1}{(1 - 5\alpha^2) + j\alpha(6 - \alpha^2)} \quad \text{——— (9)}$$

Where $\alpha = \frac{1}{\omega RC}$

For $A\beta = 1$, β should be real that is the imaginary term in equation (9) must be zero. Thus:

$$\alpha(6 - \alpha^2) = 0$$

or $$\alpha^2 = 6$$

$$\alpha = \sqrt{6}$$

That is $$\frac{1}{\omega RC} = \sqrt{6}$$

The frequency of Oscillation f_o is therefor given by

$$f_o = \frac{1}{2\pi RC\sqrt{6}} \quad \text{——— (10)}$$

Putting $\alpha^2 = 6$ in eqn (9)

$$\beta = -1/29 \quad \text{——— (11)}$$

The negative sign indicates that the feedback n/w produces a phase shift of 180°.

So, $|\beta| = \frac{1}{29}$ Since $|A\beta| \geq 1$

Therfore for sustained Oscillator

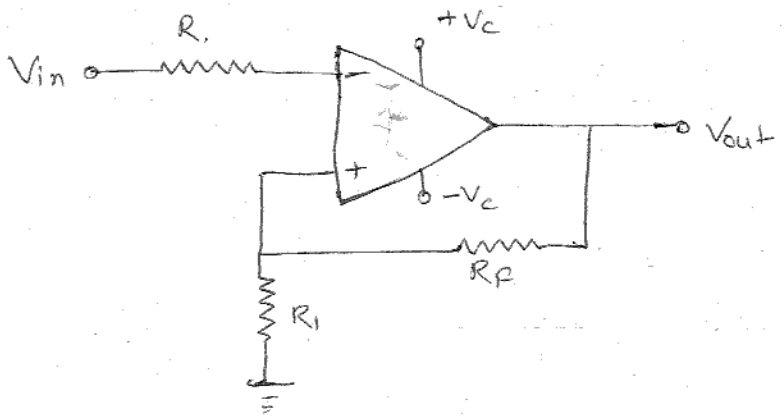
$$|A| \geq 29$$

That is the gain of the inverting op-amp should be atleast 29, or $R_f = 29 R_1$. The gain A_v is kept greater than 29 to ensure that variation in circuit parameters will not make $|A_v \beta| < 1$, otherwise oscillations will die out.

Q2 Explain the working of (i) Schmitt Trigger. (ii) Comparator

Sol^n i) **Schmitt Trigger:**

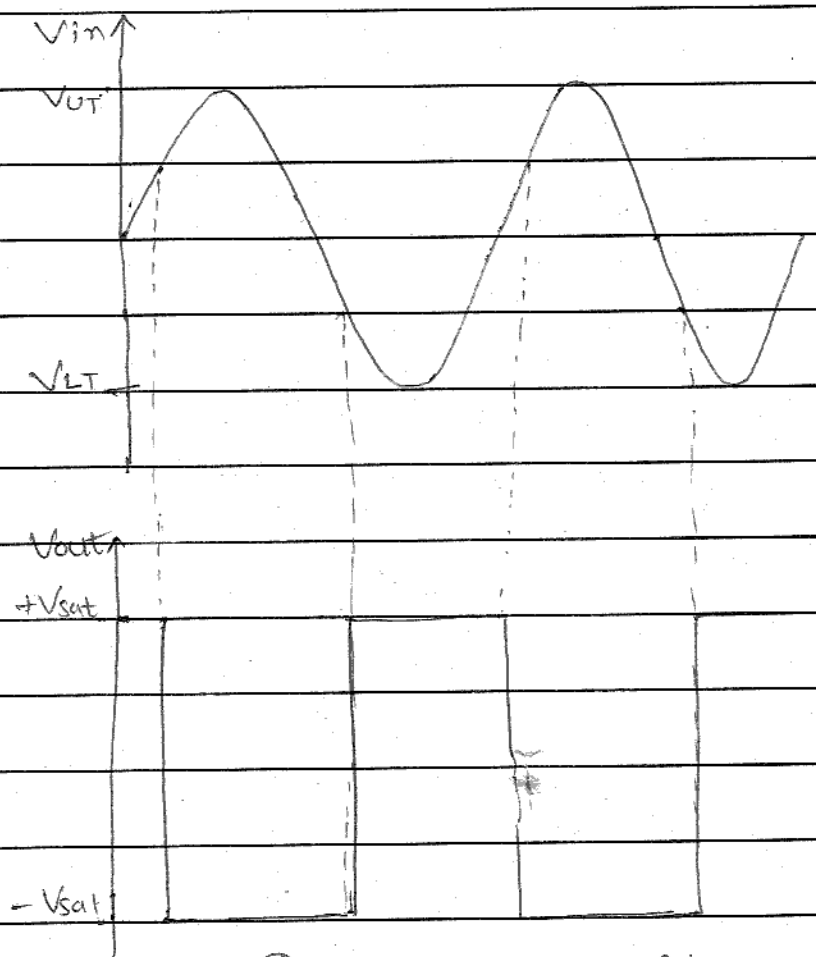
Schmitt trigger is a zero crossing detector with hysterics. Hysterics describes a system that acts differently when the input voltage goes from negative to positive than it does when the input goes from positive to negative. Positive feedback results in hysteris. Fig. shows the circuit Diagram of the Schmitt trigger.



A Schmitt trigger circuit employs a positive feedback. The output is fed back to the non-inverting terminal through a resistor. The positive feedback improves the performance of the device.

The Output Voltage swings in the negative direction whenever the input voltage exceeds the threshold voltage at an non-inverting input terminal. The Schmitt trigger has two different threshold voltage, An upper trigger voltage, V_{UT}.

and a lower trigger voltage V_{LT}.



Input & output waveforms of a Schmitt Trigger.

When the input is rising, it has to exceed V_{UT} to swing the output in the negative direction. When the input is falling it has to drop below V_{LT} to swing the output in the positive direction. This property is known as hysteresis. This makes the Schmitt Trigger less sensitive to small random noise voltages. If the input signal rises just above V_{UT}, it triggers a swing in the output to negative saturation. If at that instant, a small random

noise voltage causes the input to drop slightly below V_{UT}. the output does not switch, because once the output is negative, the input drops to V_{LT} to make the output swing. V_{UT} and V_{LT} are spaced for enough apart so that the expected noise voltage in the circuit will not be large enough to cause unwanted swinging back and forth of the output.

The value of the threshold voltage depends on the output voltage. If the output voltage is at its positive maximum that is $V_{OUT} = +V_{sat}$ then the threshold voltage is +ve. The value of the threshold voltage present at the non-inverting terminal is determined by the voltage divider formed by R_1 and R_F as:

$$V_{UT} = \left(\frac{R_1}{R_F + R_1}\right) \times (+V_{sat}) \quad \text{——(1)}$$

Similarly if the O/p voltage is at the negative saturation then there is negative - threshold voltage.

The value of the negative threshold voltage is given by.

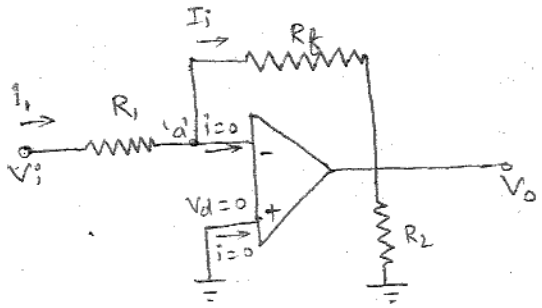
$$V_{LT} = \left(\frac{R_1}{R_F + R_1}\right) \times (-V_{sat}) \quad \text{——(2)}$$

The hysteresis voltage is defined as the difference of the two threshold voltage and is given by.

$$V_H = \left(\frac{\because R_1}{R_F + R_1}\right) \times (2V_{sat}) \quad \text{——(3)}$$

Q3 Derive the closed loop Voltage gain Equation for inverting and Non-Inverting Amplifier.

Sol^n Inverting Amplifier:



In an inverting amplifier, the non-inverting terminal of the op-amp is grounded and the input voltage as well as the feedback is fed to the inverting terminal. This is called the degenerative feedback System because the feedback is given to the inverting terminal. Any increase in the output voltage is immediately compensated by feeding a subsequent voltage to its input.

The closed loop gain, A_{CL} as follow.

For simplicity, assume an ideal op-amp. As $V_d = 0$ node 'a' is at ground potential and the current i_1 through R_1 is.

$$i_1 = \frac{V_i}{R_1} \qquad \text{——— (1)}$$

Also since op-amp draws no current, all the current flowing through R_1 must ~~be~~ follow through R_f. The o/p Voltage,

$$V_o = -i_1 R_f = -V_i \frac{R_f}{R_1} \qquad \text{——— (2)}$$

Hence the gain of the inverting amplifier (also referred as Closed loop gain) is.

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$$

Alternatively, the nodal Equation at the node 'a'.

$$\frac{V_a - V_i}{R_1} + \frac{V_a - V_o}{R_f} = 0$$

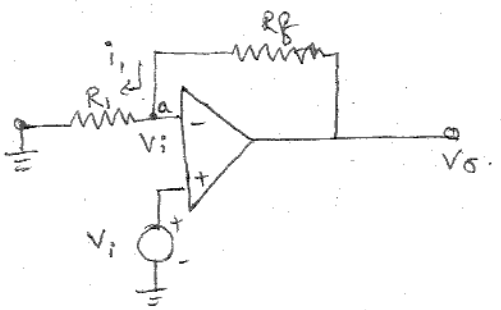
Where V_a is the Voltage at node 'a' Since node 'a' is at Virtual ground $V_a = 0$. Therefore, we get.

$$A_{CL} = \frac{V_o}{V_i} = \frac{-R_f}{R_1}$$

The -ve Sign indicates a phase shift of 180° b/w V_i and V_o. Also Since inverting input terminal is at Virtual ground the effective input impedance is R_1. The Value of R_1 Should be Kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit. A load resistor R_L is usually put at the O/p in actual practice otherwise the input impedance of the measuring device such as oscilloscope or DVM acts as the load. ~~The Calculation of load and output currents is shown~~ If however resistance R_1 and R_f in fig are replaced by impedance Z_1 and Z_f respectively. the the Voltage gain will be

$$A_{CL} = -\frac{Z_f}{Z_i}$$

Non-Inverting Amplifier:



If a Signal (ac or dc) is applied to the non-inverting i/p terminal and feedback is given as shown in fig. The circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feedback system as output is being fed back to the inverting input terminal.

As the differential Voltage V_d at the input terminal of op-amp is zero, the voltage at node 'a' in fig (a) is V_i same as the input voltage applied to non-inverting input terminal. Now R_f and R_1 forms a potential divider Hence,

$$V_i = \frac{V_o}{R_1 + R_f} \cdot R_1 \qquad \text{—— (1)}$$

and no current flows into the op-amp.

$$\frac{V_o}{V_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \qquad \text{—— (2)}$$

Thus for non-inverting amplifier the voltage gain

$$A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1} \qquad \text{—— (3)}$$

Q4. Explain the Working of.

i) Voltage to Current Converter.

ii) Triangular Wave Generator.

Sol" i) Voltage to Current Converter. (Transconductance Amplifier)

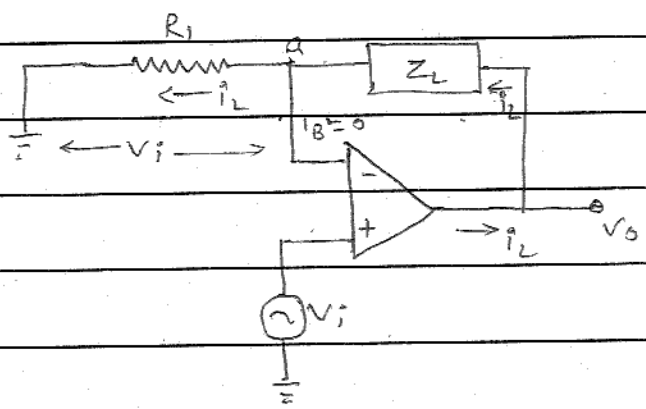
Transconductance Amplifier are Voltage - controlled current source (VCCS) in which an input voltage controls the output from the amplifier.

Transconductance amplifiers have extremely high input resistance and can be used in circuits where constant current is required.

For this there are two types of circuit possible.

V-I converter with floating load

" " " grounded "



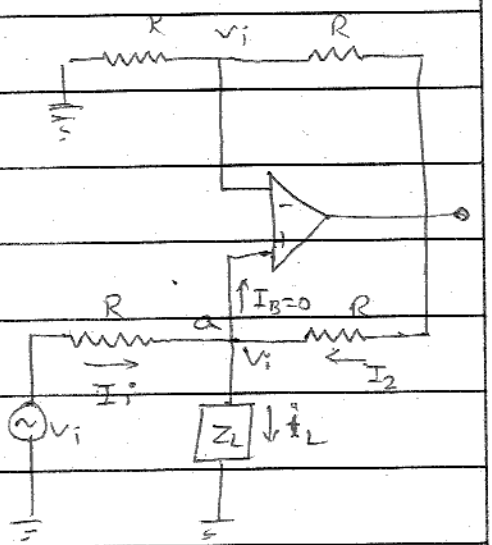


Fig (a) shows a voltage to current converter in which load Z_L is floating since voltage at node 'a' is V_i therefore

$$V_i = i_L R_1 \qquad (\text{as } I_B = 0)$$

or $$i_L = \frac{V_i}{R_1} \qquad \text{——— (1)}$$

That is the I/P voltage V_i is converted into an output current of V_i/R_1. It may be seen that the same current flows through the signal source and load and therefore, signal source should be capable of providing this load current.

A Voltage to-current converter with grounded load is in fig (b). Let V_1 be the voltage at node 'a'

writing KVL, we get.

$$i_1 + i_2 = i_L \qquad \text{——— (2)}$$

or $$\frac{V_i - V_1}{R} + \frac{V_o - V_1}{R} = i_L$$

$$V_i + V_o - 2V_1 = i_L R$$

Therefore $$V_1 = \frac{V_i + V_o - i_L R}{2} \qquad \text{——— (3)}$$

Since the op-amp is used in non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The O/P voltage is

$$V_o = 2V_1 = V_i + V_o - i_L R$$

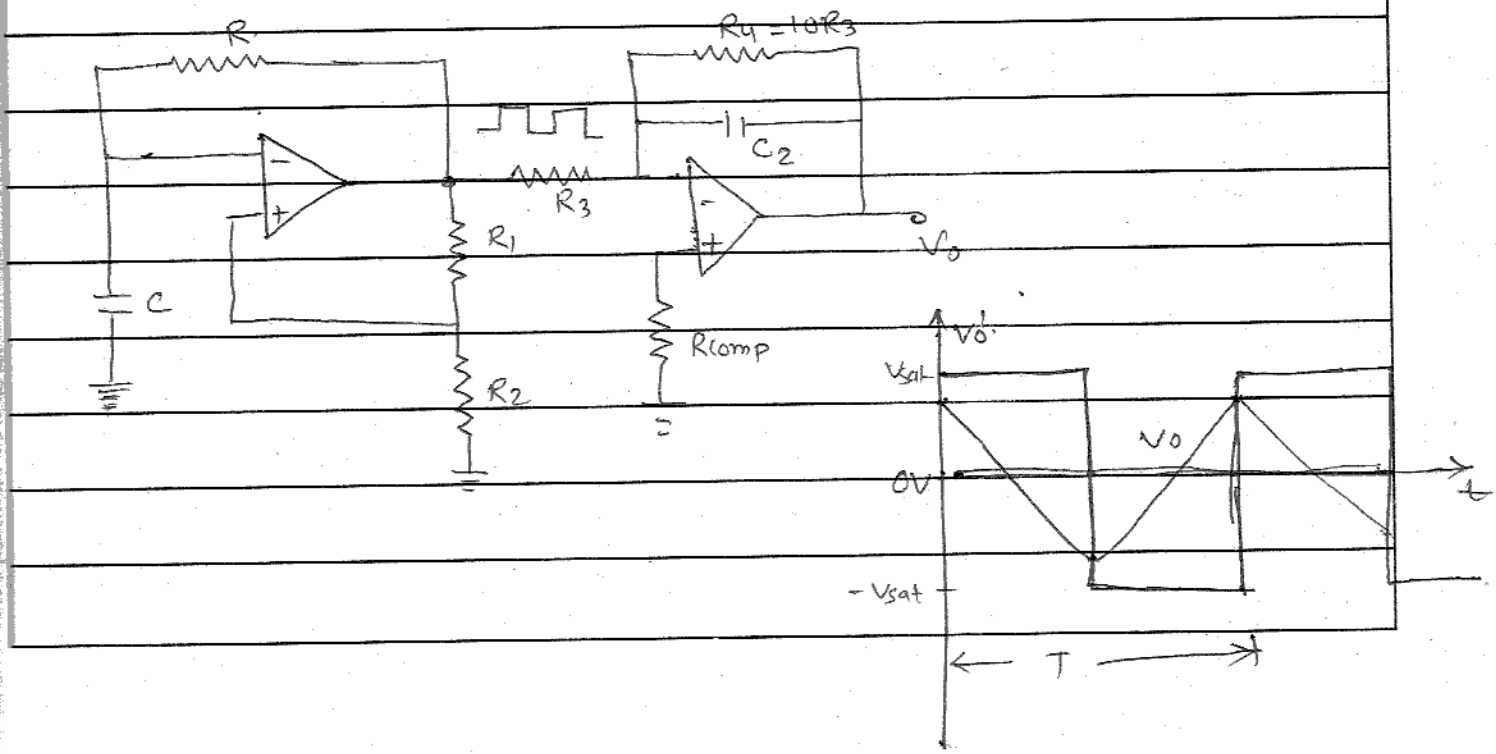
That is. $$V_i = i_L R$$

or $$i_L = \frac{V_i}{R} \qquad \text{——— (4)}$$

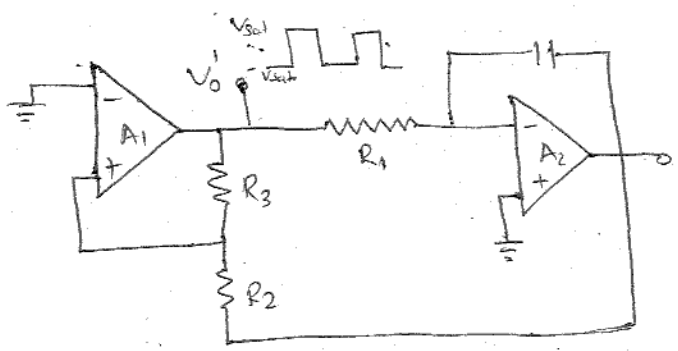
As the input impedance of a non-inverting amplifier is very high. this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and Zener diode tester.

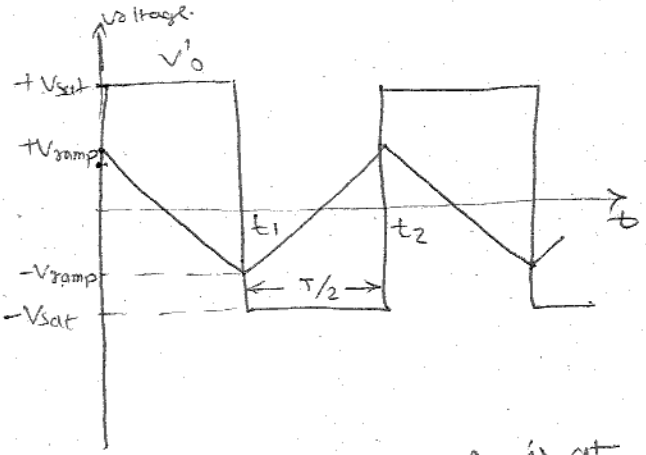
ii) Traingular Wave Generator.

A traingular coave can be simply obtained by integrating a Square coave as Shown in fig. (a) It is obvious that the frequency of the Square coave and traingular coave is the same as Shown in fig (b). Although the amplitude of the Square coave is constant at ± Vsat the amplitude of the triangular coave will decrease as the frequency increases. This is because the reactance of the Capacitor C_2 in the feedback circuit decreases at high frequencies A resistance R_4 is connected across C_2 to avoid the Saturation problem at low frequencies as in the case of practical integrator.



Another triangular wave generator using lesser number of components is shown. It basically consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of amplitude $\pm V_{sat}$ and is applied to the (-) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through a voltage divider $R_2 R_3$





Initially, let us consider the output of comparator A_1 is at $+V_{sat}$. The o/p of the integrator A_2 will be -ve going ramp as shown in fig. Thus one end of the voltage divider $R_2 R_3$ is at a voltage $+V_{sat}$ and the other at the negative going ramp of A_2 At a time $t = t_1$, when the negative going ramp attains a value of $-V_{ramp}$, the effective voltage at point P becomes slightly less than 0V. This switches the o/p of A_1 from +ve saturation to negative saturation level $-V_{sat}$. During the time when the o/p of A_1 from positive $-V_{sat}$, the o/p of A_2 increases in the +ve direction. At the instant $t = t_2$ the voltage at point P becomes just above 0V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform. It can be seen that the freq. of the square wave and triangular wave will be same, however the amplitude of the triangular wave depends upon the RC value of the integrator A_2 and the o/p voltage level of A_1. The O/P voltage of A_1 can be set to desired level by using appropriate Zener diode.

Q5 Explain Instrumentation Amplifier with a neat Diagram and derive its gain.

Soln In a Number of industrial and consumer applications, one is required to measure and control physical Quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. These physical Quantities are usually measured with the help of transducers. The o/p of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an Instrumentation amplifier are

i) high gain accuracy, ii) high CMRR, iii) low dc offset (vi) high gain stability with low temp coefficient v) low o/p impedance.

There are specially designed op-amp such as UA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD524, AD521, AD620, AD624 by Analog Device. LM 363,XX (XX → 10,1000,500) by National Semiconductor and INA 101, 104, 3626, 3629 by Burr-Brown.

Consider the basic Differential Amplifier in Fig (a) It can be easily seen that the o/p voltage V_o is given by

$$V_o = -\frac{R_2}{R_1}V_2 + \frac{1}{1+\frac{R_3}{R_4}}V_1\left(1+\frac{R_2}{R_1}\right) \qquad \left[V^+ = \frac{R_4}{R_3+R_4}V_1\right]$$

or $$V_o = -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}}\left(\frac{R_1}{R_2}+1\right)V_1\right] \qquad \text{—— (1)}$$

For $R_1/R_2 = R_3/R_4$ we obtain.

$$V_o = \frac{R_2}{R_1}(V_1 - V_2)$$

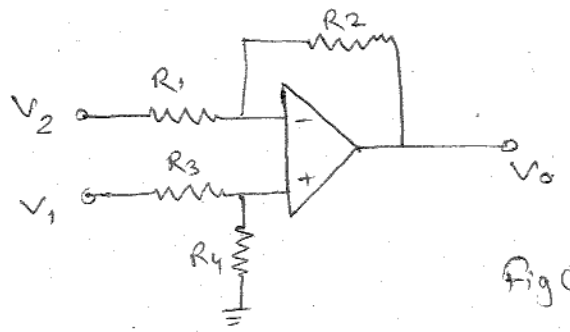
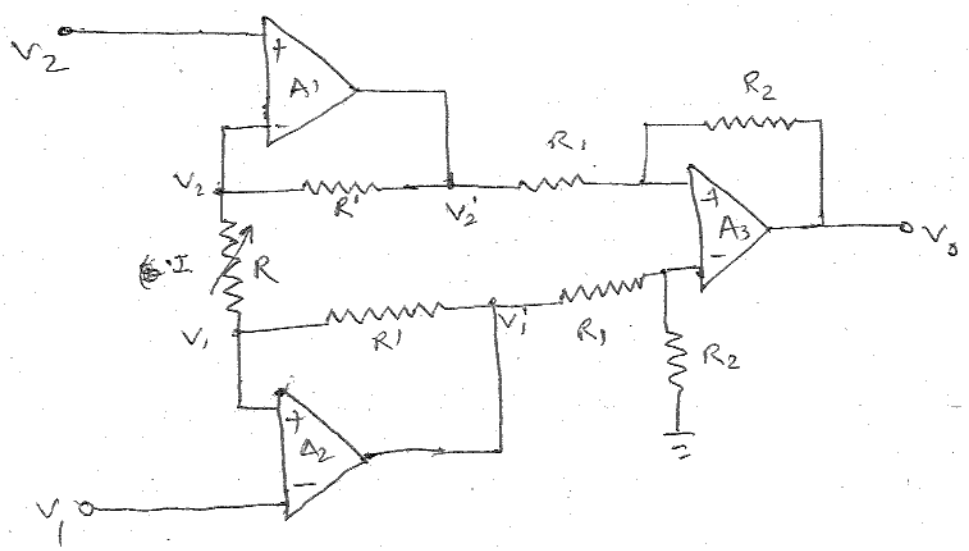


Fig (a)

In the circuit of fig (a) source V_1 sees an input impedance $= R_3 + R_4$ and the impedance seen by source V_2 is only R_1. This low impedance may load the signal source heavily. Therefore, high resistance buffer is used preceding each input to avoid this loading effect as shown in fig (b)



The op-amps A_1 and A_2 have differential input voltage as zero. For $V_1 = V_2$ that is under common mode condition, the voltage across R will be zero. As no current flows through R and R' the non-inverting amplifier. A_1 acts as voltage follower. So its output $V_2' = V_2$. Similarly op-amp A_2 acts as voltage follower having output $V_1' = V_1$. However if $V_1 \neq V_2$ current flows in R and R' and $(V_2' - V_1') > (V_2 - V_1)$

Therefore this circuit has differential gain and CMRR more compared to the single op-amp of Fig (a).

The output voltage Vo can be calculated as follow.

The voltage at the (+) i/p terminal of op-amp A_3 is $\frac{R_2 V_1'}{R_1 + R_2}$. Using superposition theorem.

$$V_o = -\frac{R_2}{R_1} V_2' + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1 + R_2}\right)$$

$$= \frac{R_2}{R_1}(V_1' - V_2') \quad \text{---} (3)$$

Since, no current flows into op-amp, the current I flowing (upwards) in R is $I = (V_1 - V_2)/R$ and passes through the resistor R'

$$V_1' = R'I + V_1 = \frac{R'}{R}(V_1 - V_2) + V_1 \quad \text{---} (4)$$

$$V_2' = -R'I + V_2 = -\frac{R'}{R}(V_1 - V_2) + V_2 \quad \text{---} (5)$$

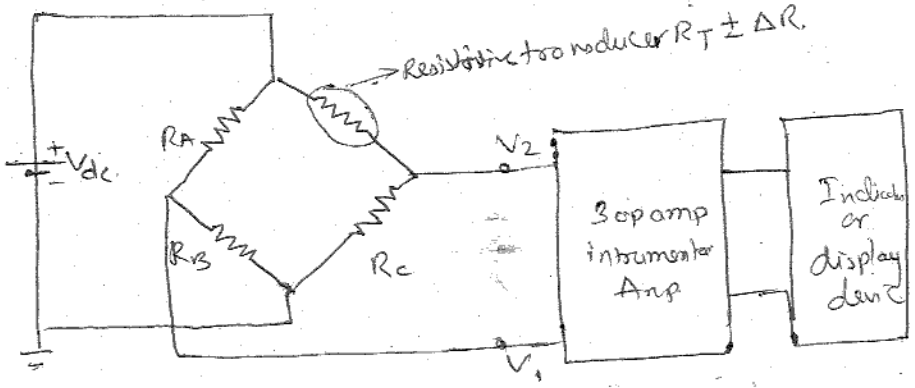
Putting the values of V_1' and V_2' in Eq^n (3) we obtain.

$$V_0 = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

$$V_0 = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2) \quad \text{——— (6)}$$

In Eq^n (6) if we choose $R_2 = R_1 = 25\ K\Omega$ and $R' = 2.5 K\Omega$, $R = 50 K\Omega$, then the gain of $\left(1 + 2 \times \frac{25 K\Omega}{50 K\Omega}\right) = 100$.

The difference gain of the I·A can be varied by replacing the resistance R by a potentiometer fig (b) The resistance R, however should never be made zero. as this will move the gain infinity. To avoid such situation in a practical circuit, a fixed resistance in series with a potentiometer is used in place of R.



Fig(c) I·A using Transducer bridge.

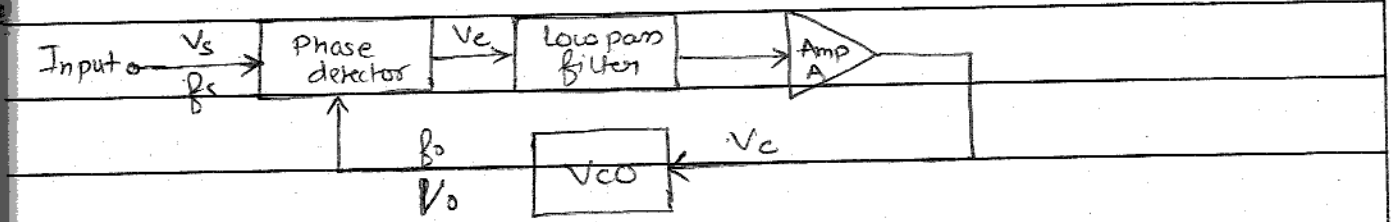
Fig (c) Shows a differential I·A using transducer bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured. The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1 = V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes. causing an unbalance in the bridge ($V_1 \neq V_2$). Thus differential voltage now gets amplified by the three op-amp differential instrumentation Amplifier.

There are a no. of practical applications of I·Amplifier. with the transducer bridge, such as temperature indicator, tempr controller, light intensity meter to name a few.

Part-B Unit-3

ARUPADAI VEEDU INSTITUTE OF TECHNOLOGY Sheet No.

1. Briefly Explain the block diagram of PLL and derive the Expression for lock range and Capture range.



The feedback System consist of:

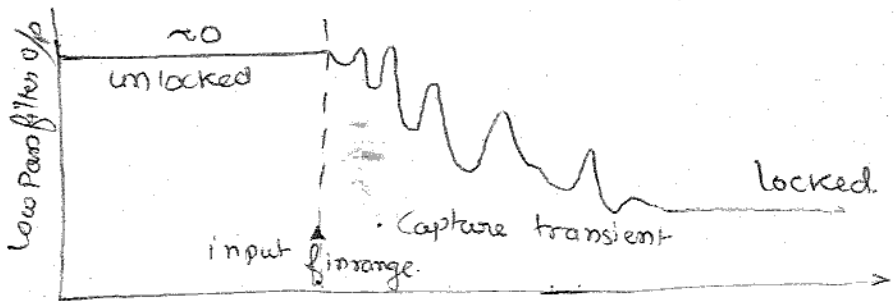
1) Phase detector / Comparator 2) A loop pass filter

3) An error amplifier 4) A Voltage Controlled Oscillator (VCO)

The VCO is a free running multivibrator and operates at a set frequency. This frequency is determined by an external timing Capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage Vc to an appropriate terminal of the Ic. The frequency deviation is directly proportional to the dc controlled voltage and hence it is called a "Voltage Controlled Oscillator or VCO

If an input Signal Vs of frequency fs is applied to the PLL, the phase detector compares the phase and frequency of the incoming Signal to that of the output Vo of the VCO. If the two Signals differ in frequency and/or phase an error voltage Ve is generated. The phase detector is basically a multiplier and produces the Sum (fs + fo) and difference (fs - fo) components

at its output. The high frequency component ($f_s + f_o$) is removed by the loco pass filter and the difference frequency component is amplified and then applied as control voltage V_c to VCO. The signal V_c shifts the VCO frequency in a direction to reduce the frequency difference b/w f_s and f_o. Once this action starts, we say that the signal is in the capacture range. The VCO continues to change frequency till its output frequency is exactly the output frequency f_o of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage V_c to shift the VCO frequency from f_o to f_s and thereby maintain the lock. Once locked PLL tracks the frequency changes of the input signal. Thus a PLL goes through three stages (i) free running (ii) capture and (iii) locked or tracking.



As capture starts, a small sine wave appears. This is due to the difference frequency b/w the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency ~~b/w~~ becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks.

A loco pass filter control s the capture range. If VCO freq is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. we say that the signal is out of the capture band. Once locked the filter no longer to restricts the PLL.

Lock in Range: When PLL is in lock, it can track frequency change in the incoming signal.

The range of frequency which the PLL can maintain lock with the incoming signal is called the lock range. It is denoted by $\pm f_0$

Derivation:

If ϕ radians is the phase difference b/w the signal and the VCO voltages, then the output voltage of the analog phase detector is given by,

$$V_e = K_\phi(\phi - \pi/2) \quad \text{——— (1)}$$

where K_ϕ is the phase angle to voltage transfer coefficient of the phase detector. The control voltage to VCO is,

$$V_c = AK_\phi(\phi - \pi/2) \quad \text{——— (2)}$$

where A is the voltage gain of the amplifier. This V_c shifts VCO frequency from its free running frequency f_0 to a frequency f given by,

$$f = f_0 + K_v V_c \quad \text{——— (3)}$$

Where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked in to signal frequency f_s then we have.

$$f = f_s = f_0 + K_v V_c \quad \text{——— (4)}$$

$$V_c = (f_s - f_0)/K_v = AK_\phi(\phi - \pi/2) \quad \text{——— (5)}$$

Thus $$\phi = \pi/2 + (f_s - f_0)/K_v K_\phi A \quad \text{——— (6)}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian

and $V_e(max) = \pm K\phi \cdot \pi/2$ from. The corresponding value of the maxm control voltage available to drive the VCO will be.

$$V_c(max) = \pm (\pi/2) K\phi A \quad \text{——— (7)}$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_0)max = K_V V_c(max) = K_V K\phi A (\pi/2) \quad \text{——— (8)}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_0 \pm (f - f_0)max = f_0 \pm K_V K\phi (\pi/2) A$$
$$= f_0 \pm \Delta f_L \quad \text{——— (9)}$$

where $2\Delta f_L$ will be the lock in frequency range and is given by,

$$\text{lock in range} = 2\Delta f_L = K_V K\phi A \pi \quad \text{——— (10)}$$

$$\Delta f_L = \pm K_V K\phi A (\pi/2) \quad \text{——— (11)}$$

The lock in range is symmetrically located with respect to VCO free running frequency f_0 for IC PLL 565.

$$K_V = \frac{8 f_0}{V}$$

where $V = +V_{CC} - (-V_{CC})$

Again $K\phi = \frac{1.4}{\pi}$

and:

Hence the lock in range from eqn (11) becomes.

$$\Delta f_L = \pm 1.8 f_0/V \quad \text{——— (12)}$$

* Capture Range:-

The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_0.

Derivation:-

When PLL is not initially locked to the signal the freq of the VCO will be free running frequency f_0. The phase angle diff. b/w the signal and the VCO output voltage will be.

$$\phi = (\omega_s t + \theta_s) - (\omega_0 t + \theta_0).$$
$$= (\omega_s - \omega_0) t + \Delta\theta \quad \text{——— (1)}$$

Thus the phase angle difference does not remain constant, but will change with time at a rate given by,

$$\frac{d\phi}{dt} = \omega_s - \omega_o \quad \text{——— (2)}$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta f$.

The loop pass filter (LPF) is a simple RC network having transfer fn.

$$T(jf) = \frac{1}{1 + j(f/f_1)} \quad \text{——— (3)}$$

where $f_1 = 1/2\pi RC$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) \simeq f_1/jf \quad \text{——— (4)}$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_o$. If $\Delta f > 3f$, the LPF transfer fn will be approximately

$$T(\Delta f) \simeq f_1/\Delta f = f_1/(f_s - f_o) \quad \text{——— (5)}$$

The voltage V_c to drive the VCO is

$$V_c = V_e \times T(f) \times A \quad \text{——— (6)}$$

or $$V_{c(max)} = V_{e(max)} \times T(f) \times A$$

$$= \pm K_\phi(\pi/2)\, A\, (f_1/\Delta f) \quad \text{——— (7)}$$

Then the corresponding value of the max^m VCO freq shift is.

$$(f - f_o)_{max} = K_V V_{c(max)} = \pm K_V K_\phi(\pi/2) A (f_1/\Delta f) \quad \text{——— (8)}$$

For the acquisition of signal frequency, we should put $f = f_s$, so that the maximum signal frequency range that can be acquired by PLL is.

$$(f_s - f_0)_{max} = \pm K_v K_\phi (\pi/2) A(f_1/\Delta f_c) \quad \text{——(9)}$$

Now $\Delta f_c = (f_s - f_0)_{max}$

$$(\Delta f_c)^2 = K_v K_\phi (\pi/2) \Delta f_1$$

$$\Delta f_L = \pm K_v K_\phi \cdot (\pi/2) A$$

we get $(\Delta f_c) \simeq \pm \sqrt{f_1 \Delta f_L}$ —— (10)

Therefore the total capture range is.

$$2\Delta f_c \simeq 2\sqrt{f_1 \Delta f_L} \quad \text{——(11)}$$

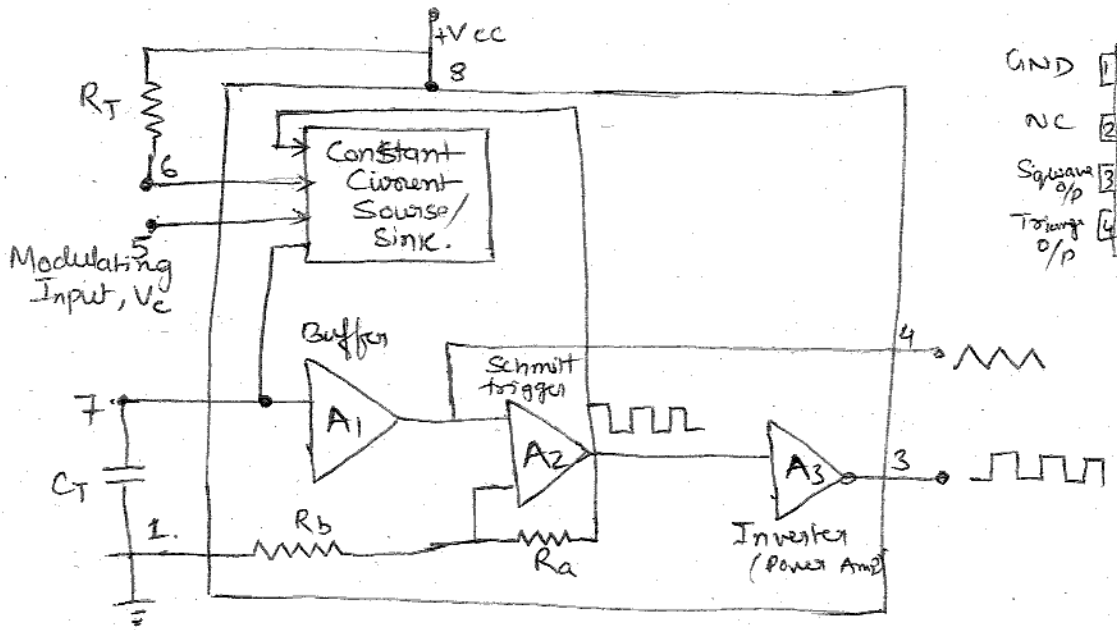
where the lock in range $= 2\Delta f_L = K_v K_\phi \Delta \pi$. In case of IC PLL 565. $R = 3.6\,K\Omega$ so the capture range is

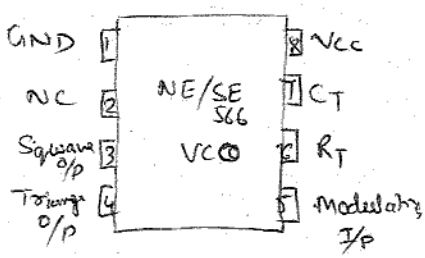
$$\pm \left[\frac{\Delta f_L}{2\pi(3.6\times 10^3)C}\right]^{1/2} \quad \text{——(12)}$$

where C is in farads.

Q2 With a neat functional diagram. Explain the operation of VCO Also derive an expression for f_0.

Soln



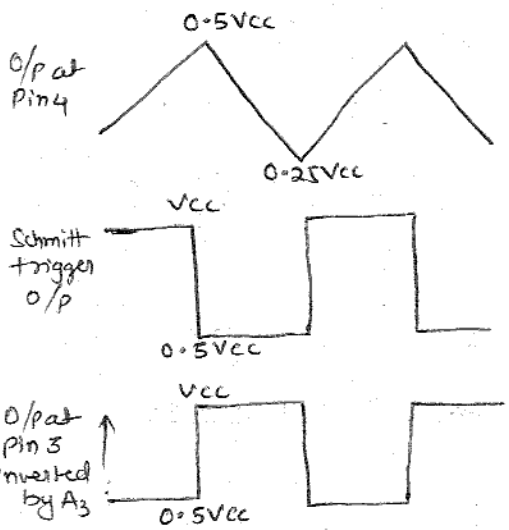


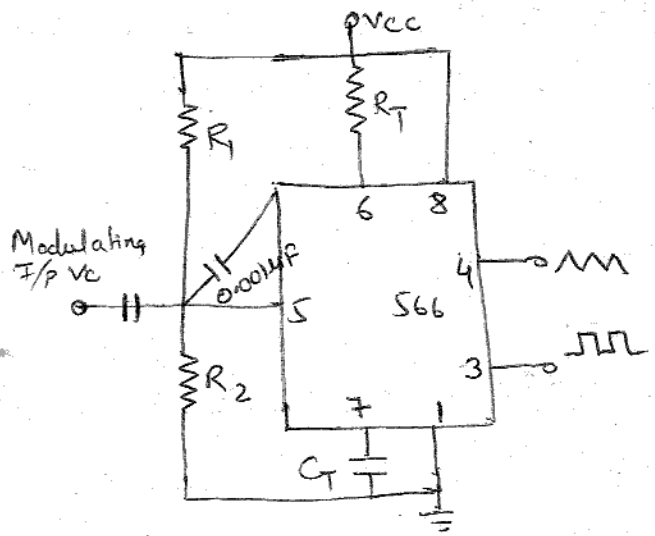
A common type of VCO available in IC form in Signetics NE/SE 566. The pin configuration and basic block diagram of 566 VCO are shown in fig. A timing Capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the Voltage V_c applied at the modulating input or by changing the timing Resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus if the modulating voltage at pin 5 is increased the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

A small capacitor of 0.01 uF should be connected between pin 5 and 6 to eliminate possible oscillations. A VCO is commonly used in converting low frequency signals such as EEG's EKG into an audio frequency range. Thus audio signals can be transmitted over telephone lines or a two way radio communication systems for diagnostic purpose or can be recorded on a magnetic tape for further reference.

The Voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via Buffer Amplifier A_1. The Output Voltage swing of the

Schmitt trigger is designed to Vcc and 0.5Vcc. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5Vcc to 0.25Vcc. In fig (c) when the voltage on the capacitor C_T exceeds 0.5Vcc during Charging, the output of the Schmitt trigger goes low (0.5Vcc) The capacitor now discharges and when it is at 0.25Vcc. the output of Schmitt trigger goes HIGH (Vcc). Since the Source and Sink currents are equal, capacitor charges and discharge for the same amount of time. Thus gives a triangular voltage waveform across C_T which is also available at pin 4. The Square wave output of the Schmitt trigger is inverted by inverter A_3 and is available at pin 3. The o/p waveforms are shown in fig.





The O/p freq of the VCO can be ~~derived~~ calculated as follows.

The total voltage on the capacitor changes from 0.25Vcc to 0.5Vcc Thus $\Delta V = 0.25 V_{CC}$. The capacitor chargers with a constant current source.

$$\text{So} \quad \frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

$$\text{or.} \quad \frac{0.25\,V_{cc}}{\Delta t} = \frac{i}{C_T}$$

$$\text{or} \quad \Delta t = \frac{0.25\,V_{cc} C_T}{i} \qquad \text{(1)}$$

The time period T of the triangular coaveform $\simeq 2\Delta t$. The frequency of oscillator f_o is.

$$f_o = \frac{1}{T} = \frac{1}{2\Delta t} = \frac{i}{0.5 V_{cc} C_T}$$

But $$i = \frac{V_{cc} - V_c}{R_T} \quad \text{——(2)}$$

where V_c is the voltage at pin 5, Therefor.

$$\boxed{f_o = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}}} \quad \text{——(3)}$$

The o/p freq of the VCO can be changed either by R_T, C_T or the voltage V_c at the modulating i/p terminal. The voltage V_c can be varied by connecting a $R_1 R_2$ circuit as shown (d)

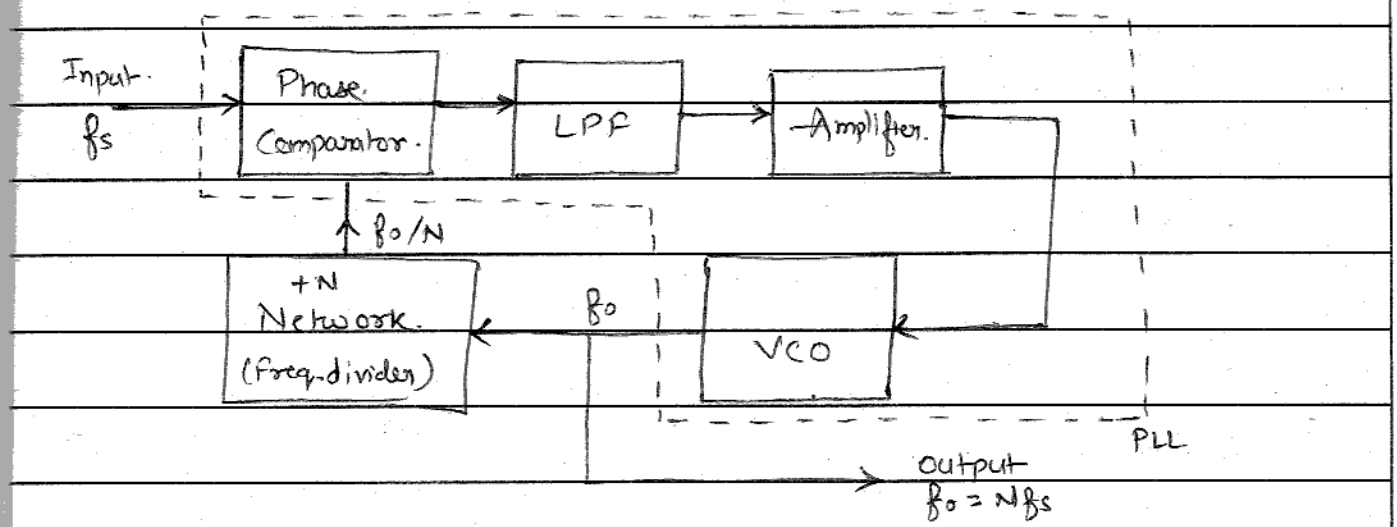
The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating freq. Now the modulating i/p voltage is usually varied from 0.75 Vcc to Vcc which can produce a frequency variation of about 10 to 1. with no modulating i/p signal : if the voltage at pin 5 is biased at (7/8) Vcc Eqn (3) gives the VCO output freques as.

$$f_o = \frac{2(V_{cc} - (7/8) V_{cc})}{C_T R_T V_{cc}}$$

$$= \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T} \quad \text{——(4)}$$

Briefly Discuss the applications of PLL

1) Frequency Multiplication / Division



The Block Diagram of a Frequency Multiplier using PLL - A divide by N network is inserted b/w the VCO output and the phase comparator I/p. In a locked state, the VCO output frequency fo is given by,

$$f_o = N f_s \quad \text{——— (1)}$$

The multiplication factor can be obtained by selecting a proper scaling factor N of the Counter. Frequency Multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics eg. Square wave, Pulse train etc, then VCO can be directly locked to the n-th harmonic of the input signal without Connecting any frequency divider in between. However as the amplitude of the higher order harmonics becomes less effective locking may not take place for high values of n.

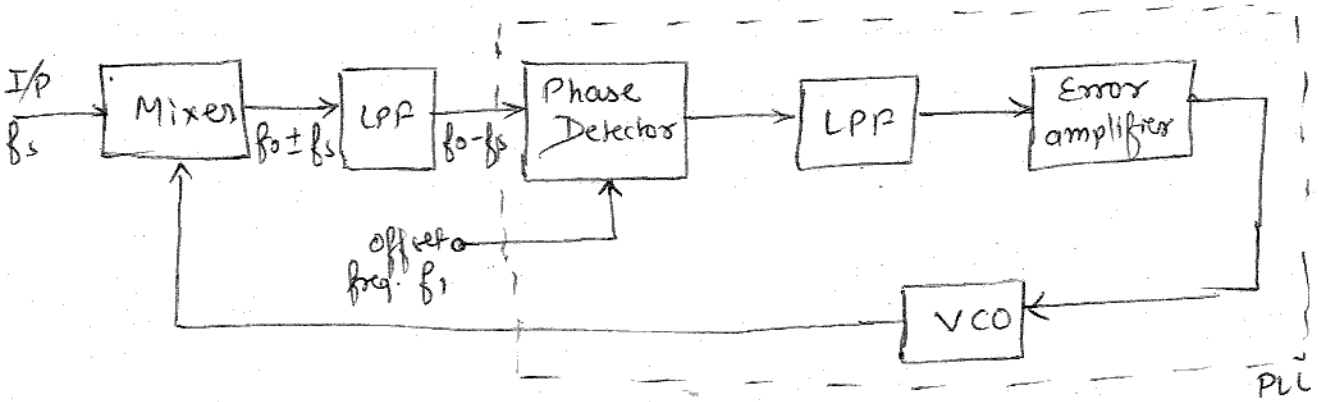
Typically n is kept less than 10.

The circuit of fig. can also be used for frequency division. Since the VCO output is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_o of VCO is now given by

$$f_o = \frac{f_s}{m}$$

2) Frequency Translation:

The frequency translation means shifting the frequency of an Oscillator by a small factor.



It consist of mixer, low pass filter and the PLL. The input freq. f_s which has to be shifted is applied to the mixer. Another input to the mixer is the output voltage of VCO, f_o. Therefore the output of mixer contains the sum and difference signal ($f_o \pm f_s$) The low pass filter connected at the output of mixer rejects the ($f_o + f_s$) signal and gives only ($f_o - f_s$) signal at the output. The ($f_o - f_s$) signal is applied to the phase detector. Another input for phase detector is the offset freq. f_1.

In the locked mode, the VCO o/p frequency is adjusted to make two input frequencies of phase detector equal. This gives.

$$f_o - f_s = f_1 \quad \text{and.}$$

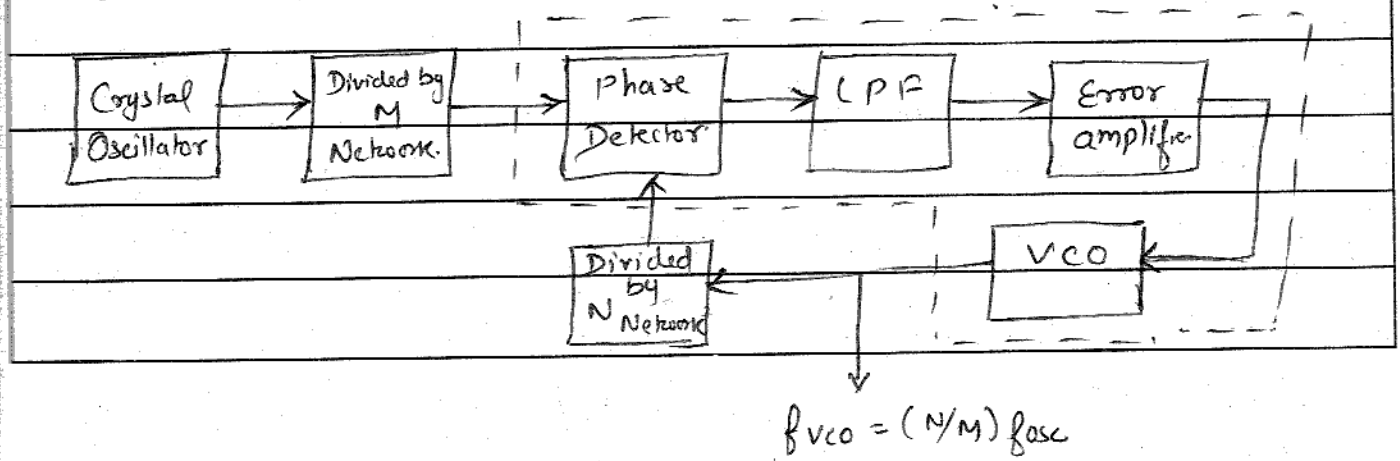
$$f_o = f_s + f_1$$

By adjusting 'offset freq f_1' we can shift the frequency of the Oscillator to the desired value.

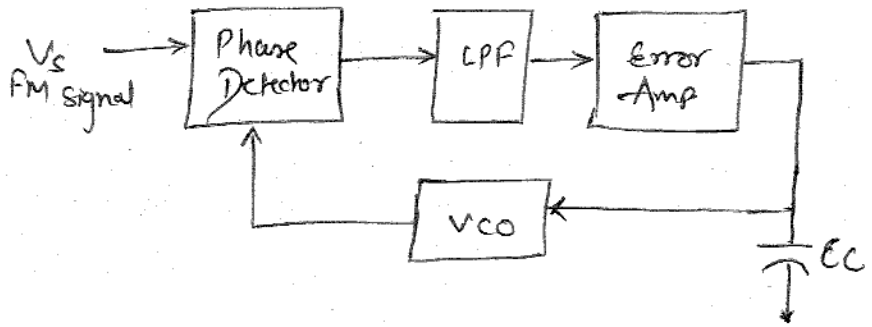
Frequency Synthesizer :-

The PLL can be used as the basic for freq. Synthesizer that can produce a precise series of frequencies that are derived from a stable crystal controlled oscillator. It is similar to frequency multiplier circuit except that divided by M Network is added at the input of phase lock loop. The frequency of the crystal-controlled oscillator is divided by an integer factor M by divider network to produce a freq f_{osc}/M, where f_{osc} is the frequency of the crystal controlled oscillator. The VCO frequency f_{vco} is similarly divided by factor N by divided network to give fregency equal to f_{vco}/N. when the PLL is locked in on the divided-down oscillator frequency, we will have $f_{osc}/M = f_{vco}/N$, so that $f_{vco} = (N/M) f_{osc}$

By adjusting divider counts to desired value large number of frequences can be produced all derived from the Crystal controlled oscillator.

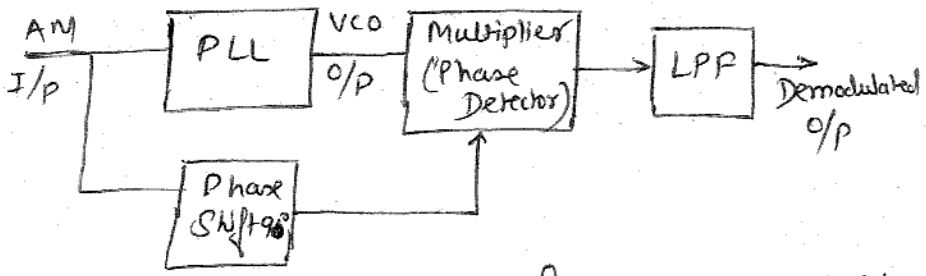


4) FM Demodulator:



The PLL can be very easily used as an FM detector or demodulator. When the PLL is locked in on the FM signal, the VCO freq. follows the instantaneous frequency of the FM signal, and the error voltage or VCO control voltage is proportional to the deviation of the input frequency from the centre frequency. Therefore the a-c component of error voltage or control voltage of VCO will represent a true replica of the modulating voltage depends on the linearity between the instantaneous frequency deviation and the modulation frequency. Should remains in the locking range of PLL to get the faithful replica of the modulating signal. If the product of the modulation frequency fm and the frequency deviation exceeds the $(\Delta f_c)^2$. the VCO will not be able to follow the instantaneous freq. variation of the FM signal.

5) AM Detection:



The PLL is locked to the carrier freq of the incoming AM signal. Once locked the output freq. of VCO is same as the carrier frequency, but it is in unmodulated form. The modulated signal with 90° phase shift and the unmodulated carrier form o/p of PLL are fed to the multiplier. Since VCO o/p is always 90° out of phase with the incoming AM signal under the locked condition, both the signals applied to the multipliers are in same phase. Therefore the output of the multiplier contains both the sum and the difference signals. The LPF connected at the o/p of the multiplier rejects high frequency

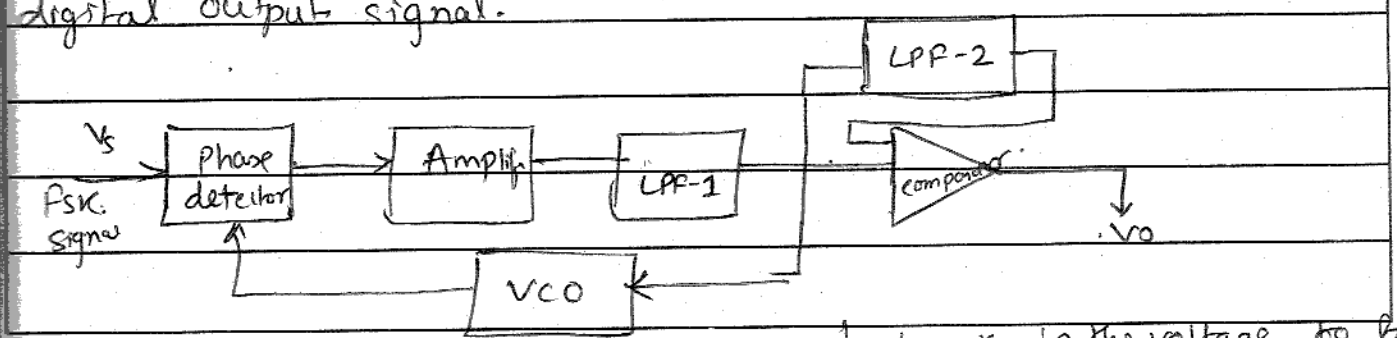
component gives demodulated output. As PLL follow the input frequency with high accuracy, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

◇ Frequency Shift Keying (FSK) Demodulator:-

In digital data communication, binary data is transmitted by means of a carrier frequency. It uses two different carrier frequency for logic 1 and logic 0 states of binary data signal. This type of data transmission is called a frequency shift keying (FSK). In this data transmission, on the receiving end two carrier frequencies are converted into 1 and 0 to get the original binary data. This process is called as FSK Demodulation.

A PLL can be used as a FSK Demodulator

It is similar to the PLL demodulator for analog FM signals except for the addition of a comparator to produce a reconstructed digital output signal.



$V_{C1} = (f_1 - f_0)/K_V$

$V_{C2} = (f_2 - f_0)/K_V$

where K_V is the voltage to freq. transfer coefficient of the VCO.

Part - B

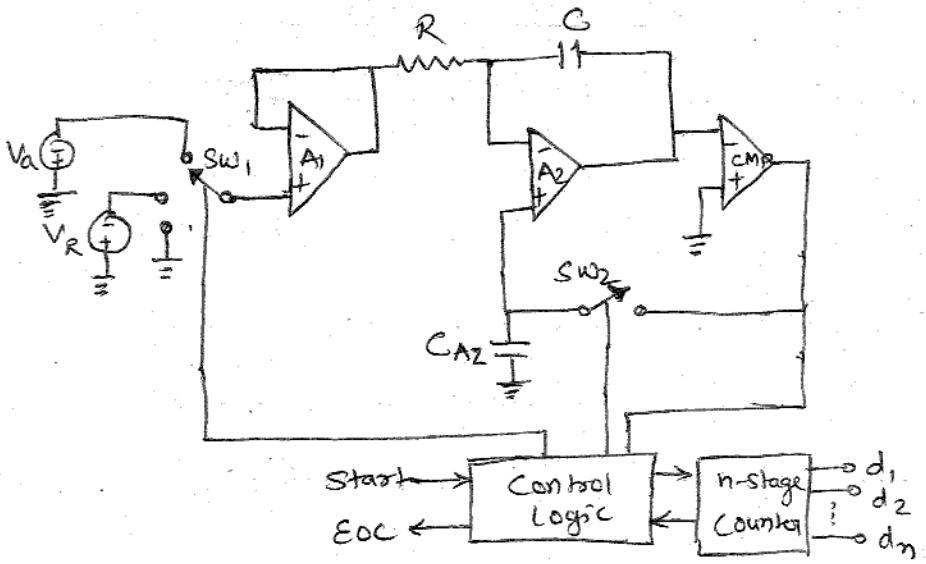
1. What is integrating type Converter ? Explain the Operation of dual slope ADC.

The integrating type of ADCs do not require a S/H circuit at the input. If the input changes during conversion the ADC output code will be proportional to the value of the input averaged over the integration period.

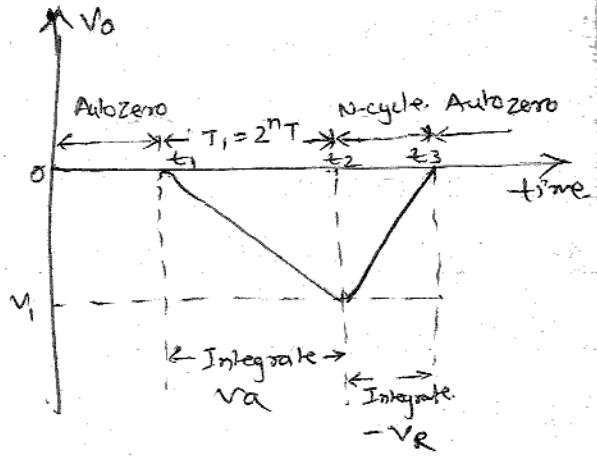
Dual Slope ADC :-

Fig (a) shows the functional diagram of the dual-slope or dual-ramp converter. The analog part of the circuit consists of a high input impedance buffer A1, precision integrator A2 and a voltage comparator. The converter first integrates the analog input signal Va for a fixed and duration of 2^n clock periods as shown in fig. (b) Then it integrates an internal reference voltage V_R of opposite polarity until the integrator output is zero. The number N of clock cycles required to return the integrator to zero is proportional to the value of Va averaged over the integration period. Hence N represents the desired output code. The circuit operates as follows.

Before the START command arrives the switch SW_1 is connected to ground and SW_2 is closed.



(a)



(b)

Any offset voltage present in the A_1, A_2, comparator loop after integration, appears across the capacitor C_{AZ} till the threshold of the comparator is achieved. The capacitor C_{AZ} thus provides automatic compensation for the input offset voltages of all the three amplifiers later, so when SW_2 opens C_{AZ} acts as a memory to hold the voltage required to keep the offset nulled. At the arrival of the START command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero. The circuit uses an n-stage ripple counter and therefore the counter resets to zero after counting 2^n pulses. The analog voltage V_a is integrated for a fixed number 2^n counts of clock pulses after which the counter resets to zero. If the clock period is T, the integration takes place for a time $T_1 = 2^n \times T$ and the output is a ramp going downwards as shown in fig (b)

The counter resets itself to zero at the end of the interval T_1 and the switch SW_1 is connected to the reference voltage $(-V_R)$. The output voltage V_o will now have a positive slope. As long as V_o is negative the output

of the Comparator is positive and the control logic allows the clock pulse to be counted. However, when V_o becomes just zero at time $t = t_3$, the control logic issues an end of conversion (EOC) command and no further clock pulses enter the counter. It can be shown that the reading of the counter at t_3 is proportional to the analog i/p voltage V_a.

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clock rate}} \quad \text{——— (1)}$$

and $$t_3 - t_2 = \frac{\text{digital count } N}{\text{Clock rate}} \quad \text{——— (2)}$$

For an integrator.

$$\Delta V_o = (-1/RC) \cdot V (\Delta t) \quad \text{——— (3)}$$

The voltage V_o will be equal to V_1 at the instant t_2 and can be written as.

$$V_1 = (-1/RC)\ V_a (t_2 - t_1)$$

The voltage V_1 is also given by.

$$V_1 = (-1/RC)\ (-V_R)\ (t_2 - t_3)$$

So. $$V_a (t_2 - t_1) = V_R (t_3 - t_2)$$

Putting the values of $(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$, we get.

$$V_a (2^n) = (V_R) N \quad \text{——— (4)}$$

or $$V_a = (V_R)\ (N/2^n) \quad \text{——— (5)}$$

The following important observations can be made:

1) Since V_R and n are constant, the analog voltage V_a is proportional to the count reading N and is independent of R, and T.

2) The dual-slope ADC integrates the input signal for a fixed time hence it provides excellent noise rejection of ac signals whose periods are integrals multiples of the integration time. T_1. Thus ac noise superimposed on the input signal such as 50Hz power line pick up will be averaged during the input integration time so choose clock period T, so that $2^n T$ is an integral multiple of the line period $(1/50)$ second = 20 ms.

3) The main disadvantage of the dual slope ADC is the long conversion time. For instance if $2^n = T = 1/50$ is used to reject line pick-up the conversion time will be 20 ms.

Dual slope converter are particularly suitable for accurate measurement of slowely varying signals, such as thermocouples and weighing scales. Dual slope ADC also form the basic of digital panel meters and multimeters.

Dual slope converters are available in monolithic form and are available both in microprocessor compitable and in display oriented versions. The former provide the digital code in binary form whereas the display oriented version present the output code in a format suitable for the direct drive of LED displays. The Datel Intersil ICL 7109 is a monolithic 12 bit dual slope ADC with microprocessor compatibility.

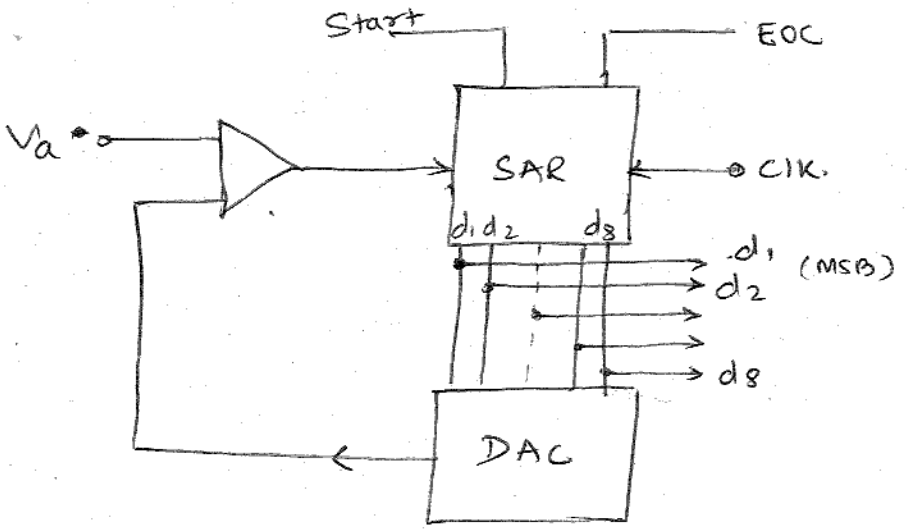
Explain the principle of operation of successive Approximation ADC.

The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods. An eight bit converter could require eight clock pulses to obtain a digital output. Fig(1) shows an eight bit converter. The circuit uses a successive approximation register (SAR) to find the required value of each bit by trial and error. The circuit operates as follows.

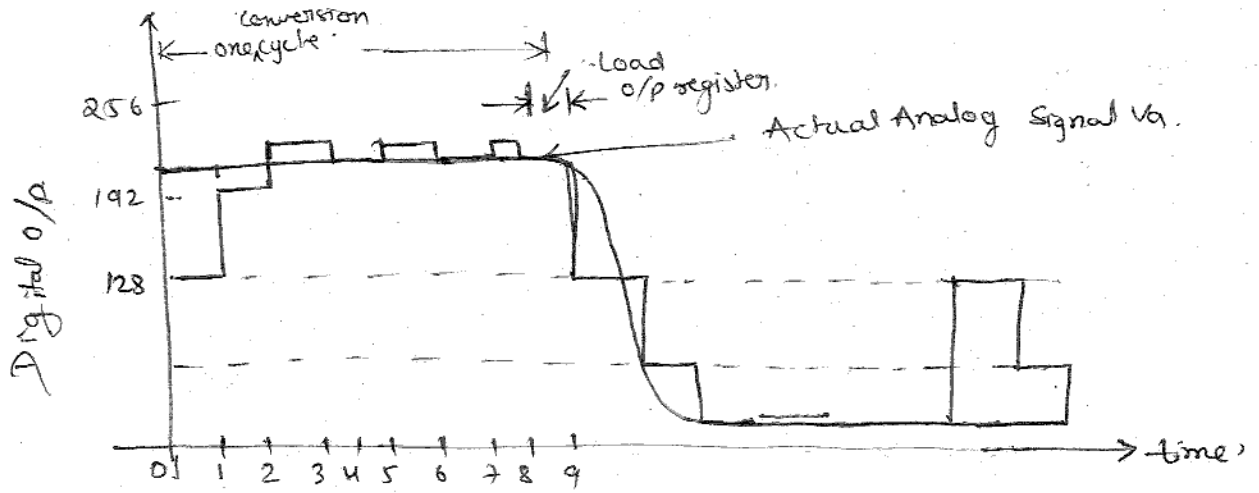
With the arrival of the START command the SAR sets the MSB $d_1 = 1$ with all other bits to Zero. So that the trial code is 10000000. The output V_d of the DAC is now compared with analog input V_a. If V_a is greater than the DAC Output V_d then 10000000 is less than the correct digital representation. The MSB is left at 1 and the next lower significant bit is made 1 and further tested.

However if V_a is less than the DAC output then 10000000 is greater than the correct digital representation. So reset MSB to 0 and go to next lower Significant bit. This procedure is repeated for all subsequent bits, one at a time, until all bits

positions have been tested. Whenever the DAC output crosses Va, the comparator changes state and this can be taken as the end of conversion (EOC) command. Fig (a) shows a typical Conversion sequence and Fig (b) shows the associated wave forms.

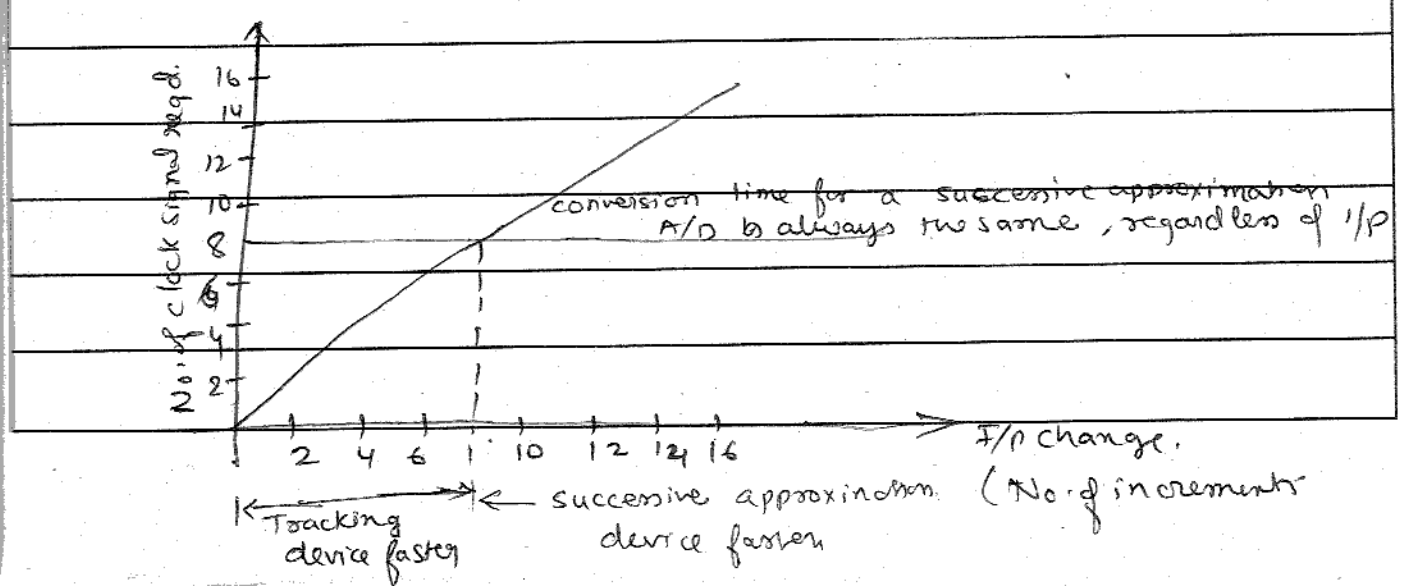


Correct digital representation.	Successive approximation register o/p. Vd at different stages in the conversion.	Comparator o/p
	1 0000000	1 (Initial o/p)
11010100	1 1000000	1
	1 1100000	0
	1 1010000	1
	1 1011000	0
	1 1010100	1
	1 1010110	0
	1 1010101	0
	1 1010100	



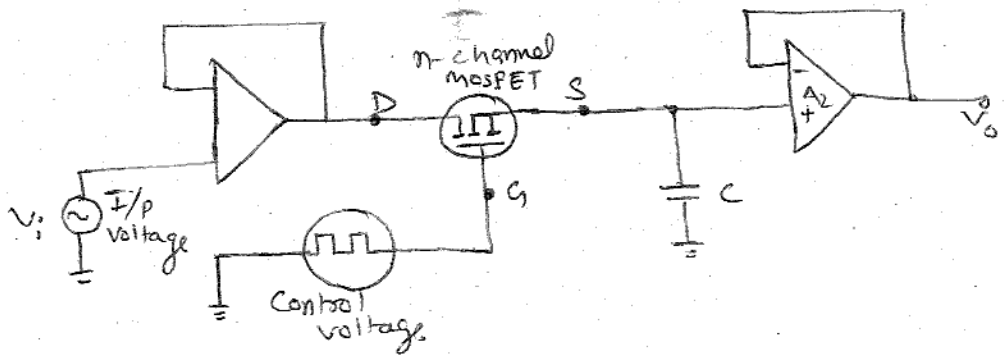
It can be seen that the D/A output voltage becomes successively closer to the actual analog input voltage. It requires eight pulses to establish the accurate o/p regardless of the value of the analog i/p. However one additional clock pulse is used to load the output register and reinitialize the circuit.

A comparison of the speed of an eight bit tracking ADC and an eight bit successive approximation ADC is made in fig. (c). Given the same clock freq., we see that the tracking circuit is faster only for small changes in the input. In general the successive approximation techniques is more versatile and superior to all other circuits discussed so far. Successive Approximation ADCs are available as self contained ICs. The AD7592 is a 28 pin dual inline CMOS package is a 12-bit A/D converter using successive approximation technique



Q3 With neat sketch explain the operation of Sample and hold circuit.

Sol^n A Sample and hold circuit samples an input signal and holds onto its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in fig. (a). The n-channel E MOSFET works as a switch and is controlled by the control voltage V_c and the capacitor C stores the charge. The analog signal V_i to be sampled is applied to the drain of E-MOSFET and the control voltage. V_c is applied to its gate. When V_c is positive the E MOSFET turns on and the capacitor C charges to the instantaneous value of input V_i with a time constant $[(R_o + r_{DS(on)}]C$.

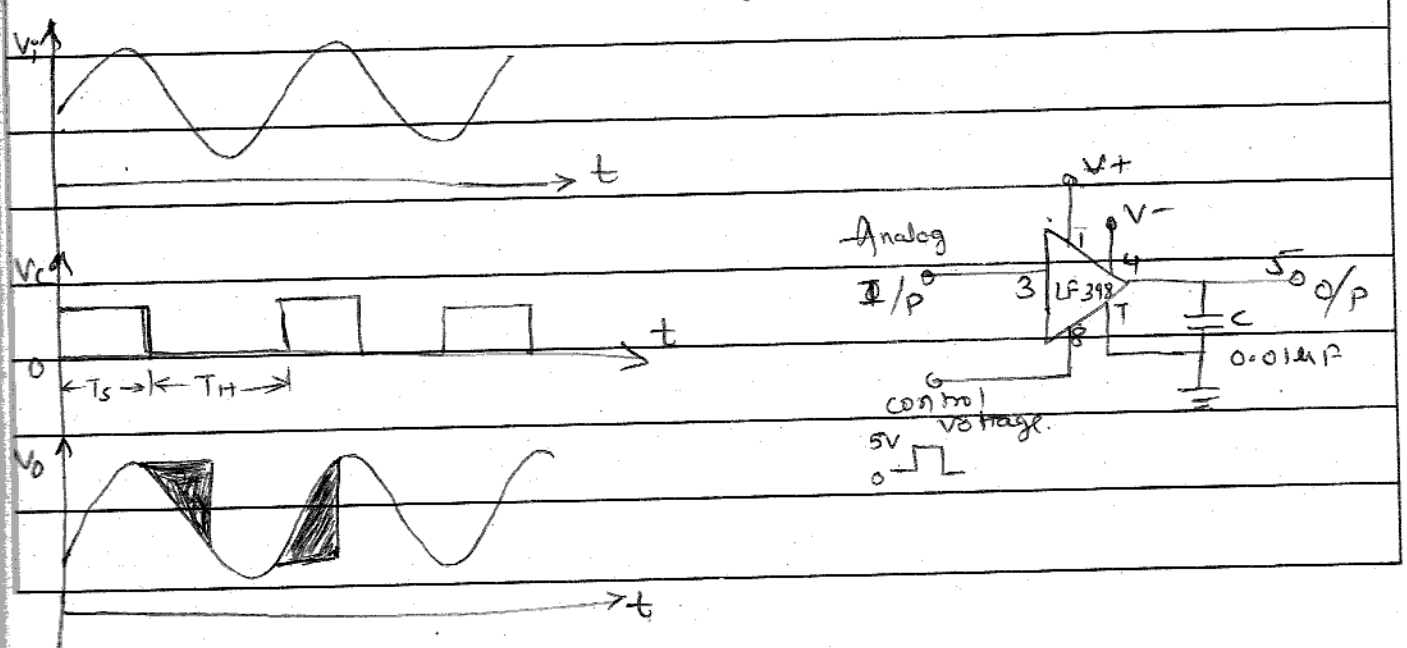


Here R_o is the output resistance of the voltage follower. A_1 or r_{DS} (ON) is the resistance of the MOSFET when ON. Thus the input voltage V_i appears across the Capacitor C and then at the output through the voltage follower A_2. The waveforms are shown in fig (b).

During the time when control voltage V_c is zero the E MOSFET is off. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot

discharge The Capacitor holds the Voltage across it. The Time period T_s, the time during which voltages across the Capacitor is equal to input voltage is called Sample period. The time period T_H of V_c during which the Voltage across the Capacitor is held constant is called hold period. The frequency of V_c during which the Voltage across the Capacitor is held constant is called hold period. The frequency of the control Voltage. Should be Kept higher than (at least twice) the input so as to retrive the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar or Teflon should be used to retain the Stored Charge. Specially designed Sample & Hold IC of make Harris Semiconductor HA2420. National Semicondutor such as LF198, LF398. are also available

A typical diagram of the LF398 is shown in fig.

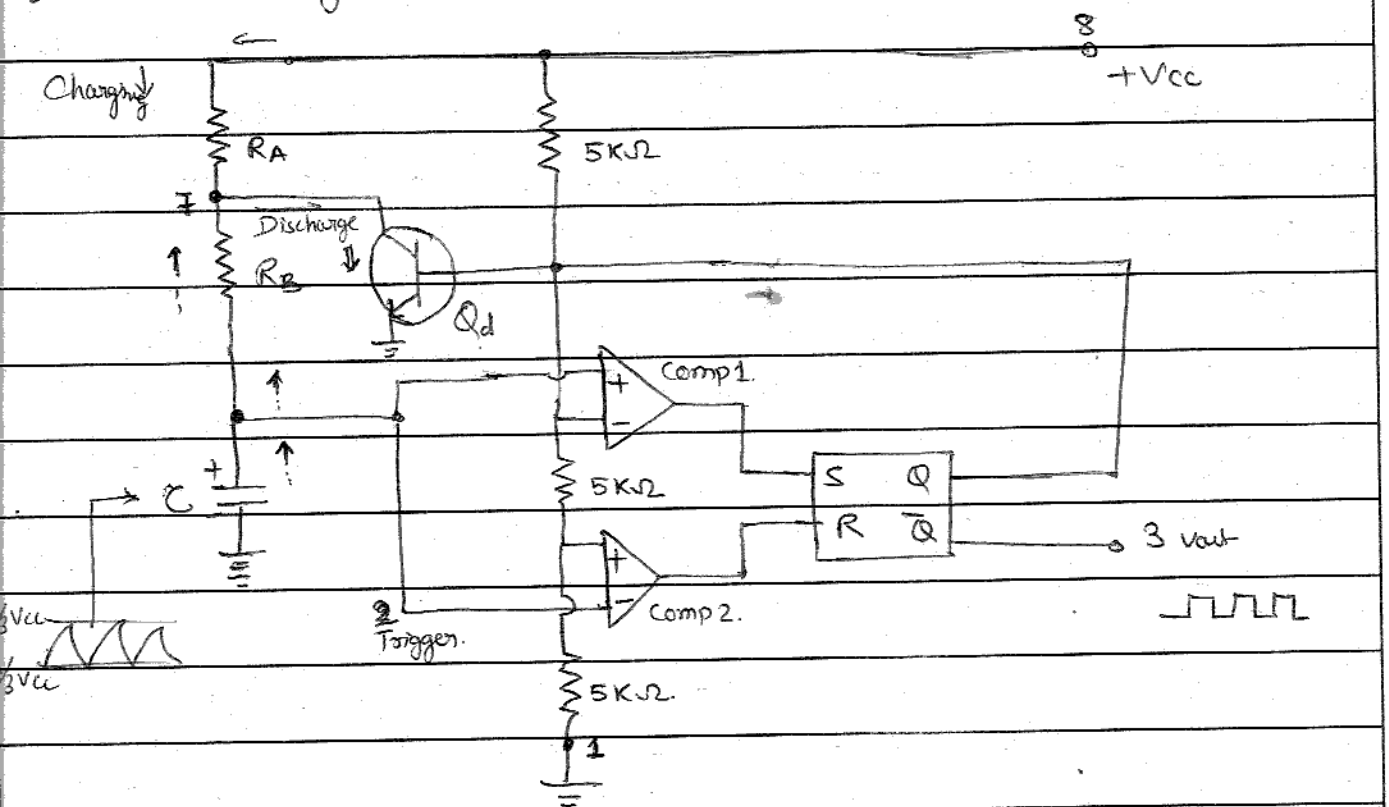


Explain the Astable mode of operation using 555 timer?

Astable Operation:-

The IC555 connected as an astable multivibrator The threshold i/p is connected to the trigger i/p. Two external resistance R_A, R_B and a capacitor C is used in the circuit.

This circuit has no stable state the ckts changes its state alternately. Hence the operation is also called free running non-sinusoidal Oscillator.



Operation:

When the flip-flop is set Q is high which drives the transistor Qd in Saturation and the Capacitor get discharged Now, the capacitor voltage is nothing but the trigger voltage. So while discharge, when it becomes less than 1/3 Vcc, comparator 2 o/p goes high this

reset the flip-flop hence Q goes low and $\bar{Q}$ goes high.

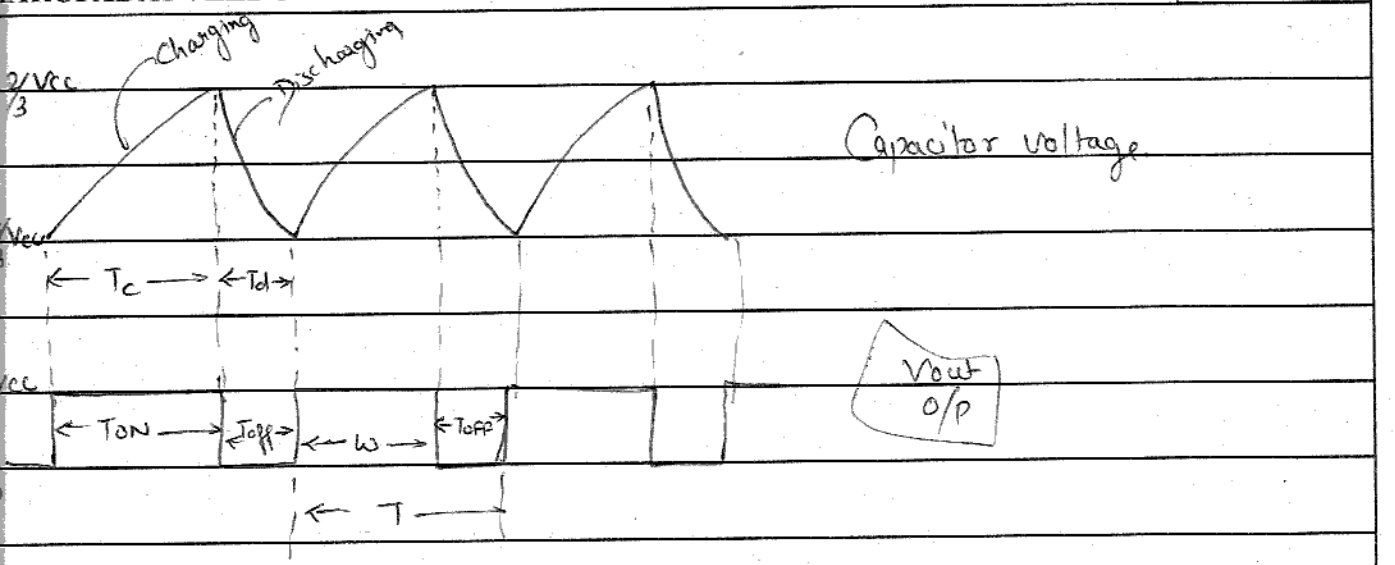
The low Q makes the transistor OFF. Thus capacitor starts Charging through the resistances R_A, R_B and V_{cc}. The Charging Path is shown by thick arrow in the Fig. (A) & As total resistance in the charging path is $(R_A + R_B)$, the Charging time const. is $(R_A + R_B)C$.

Now the capacitor voltage is also a threshold voltage while charging capacitor voltage increases i.e. the threshold voltage increases when it exceeds $2/3\ V_{cc}$ then the comp 1 o/p goes high ~~and~~ which sets the flip-flop the ~~flip-flop~~ o/p Q becomes high and o/p at pin 3 i.e. Q becomes low high Q drives transistor Qd in saturation and capacitor starts discharging through resistance R_B and transistor Qd. This path is shown by dotted arrow. Thus the Charging time Cont is R_BC. when capacitor voltage becomes less than $1/3\ V_{cc}$. comp 2 o/p goes high, resetting the F-F - The cycle repeats.

Thus when Capacitor is charging, o/p is high. while when it is discharging the o/p is low. The o/p is a rectangular wave. The capacitor voltage is exponentially rising and falling.

Duty cycle:-

Generally the charging time cont. is greater than the discharging time cont. Hence at the o/p, the waveform is not symmetric. The high o/p remains for longer period than low o/p - the ratio of high o/p period and low o/p period is given by a mathematical parameter called duty cycle. It is defined as the ratio of ON time i.e. high o/p to the total time of one cycle. As shown in waveform fig.



W = time for O/p is high = T_{ON}

T = Time of one Cycle.

D = Duty cycle = $\frac{W}{T}$

$$\% D = \frac{W}{T} \times 100\ \%$$

The Charging time for the Capacitor is given by

T_c = Charging time = $0.693 (R_A + R_B) C$

while the discharging time is given by,

$T_d = 0.693 R_B C$

Hence the time for one cycle is:

$T = T_c + T_d = \infty$

$$T = 0.693 (R_0 + R_A + R_B) C$$

while.

$W = T_c = 0.693 (R_A + R_B) C$

$$\% D = \frac{W}{T} \times 100 = \frac{0.693 (R_A + R_B) C}{0.693 (R_A + R_B) C} \times 100$$

$$\therefore \%D = \frac{(R_A + R_B)}{(R_A + 2R_B)} \times 100$$

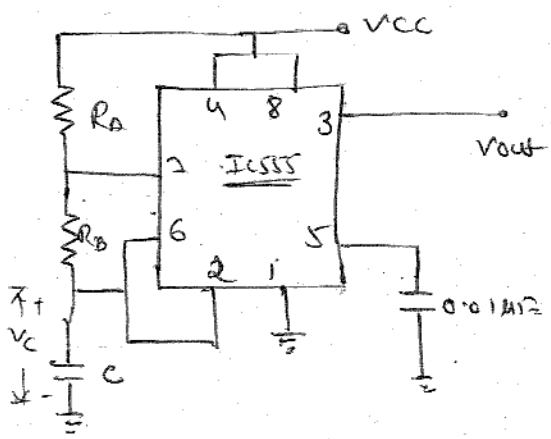
while the frequency of oscillation is given by.

$$f = \frac{1}{T} = \frac{1}{0.693\,(R_A + R_B)\,C}$$

$$\therefore \boxed{f = \frac{1.44}{(R_A + 2R_B)\,C} \text{ Hz}}$$

Schematic Diagram:

Fig shows the Schematic Diagram of astable time ckt. It shows only the external comp. R_A, R_B and R_C. The pin 4 is tied to pin 8 and pin 5 is grounded through a small Capacitor.



The important Applⁿ of astable Multivibrator is voltage controlled Oscillator

Applⁿ

1) Square wave generator
2) VCO
3) FSK generator
4) Flasher ckt.

Q3 Explain in detail about Class A and Class B Power Amplifiers.

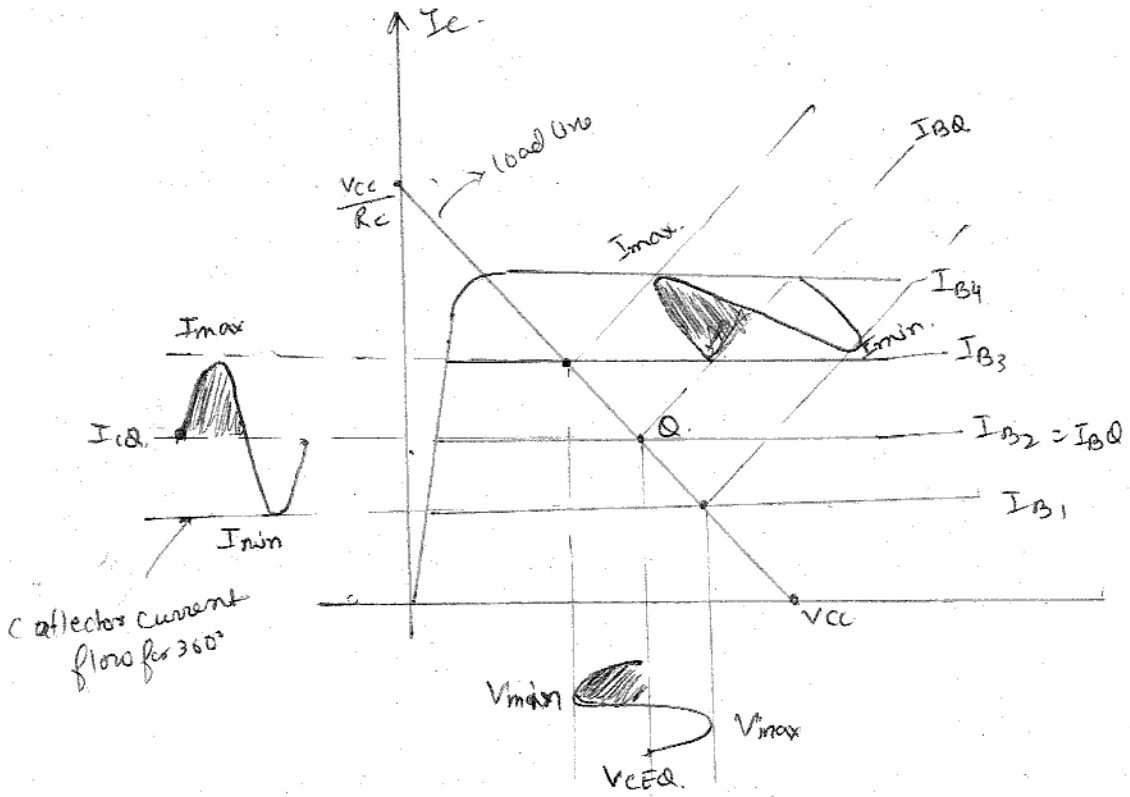
Class A

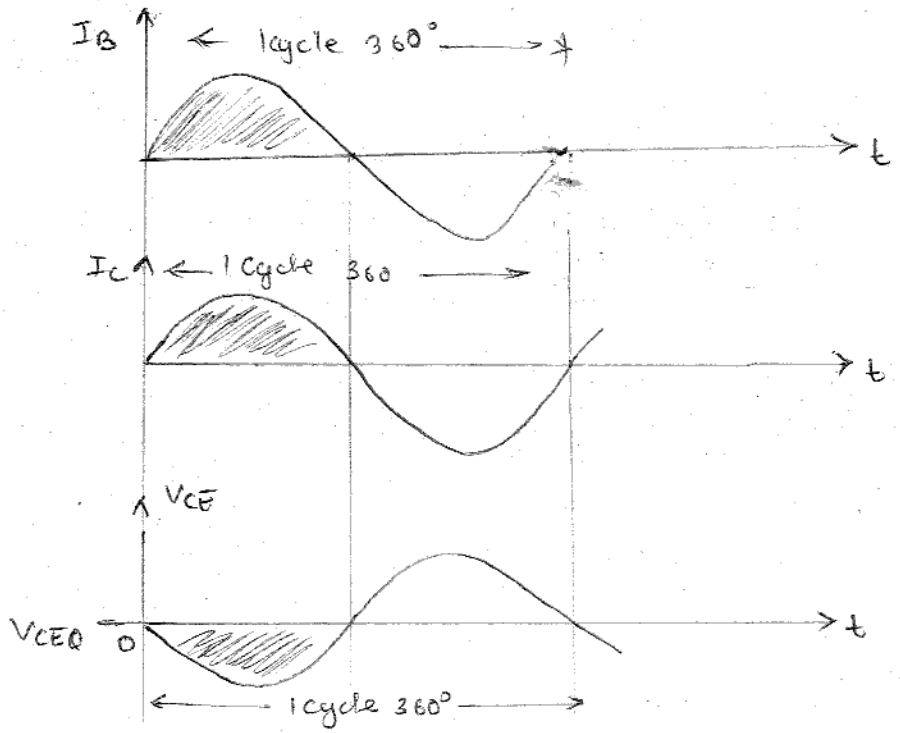
The power ampl. is said to be class A amplifier if Q point and the i/p signal are selected such that the o/p signal is obtained for a full I/p cycle. For this, position of the Q point is approximated at the mid point of the load line.

For all values of i/p signal the transistor remains in the active region and never enters into cut-off or saturation region. When an ac i/p signal is applied the collector voltage sinusoidally hence the collector current also varies sinusoidaley the collector current flows for 360° (full cycle) of the I/p signal. In other words, the angle of the collector current flow is 360° ie one full cycle.

The current and voltage waveforms for a class A operation are shown with the help of O/p characteristics and the load lines.

As shown in fig. for full i/p cycle full o/p cycle is obtained Here S/g is faithfully reproduced at the o/p without any distortion. The efficiency of class A operation is very small.

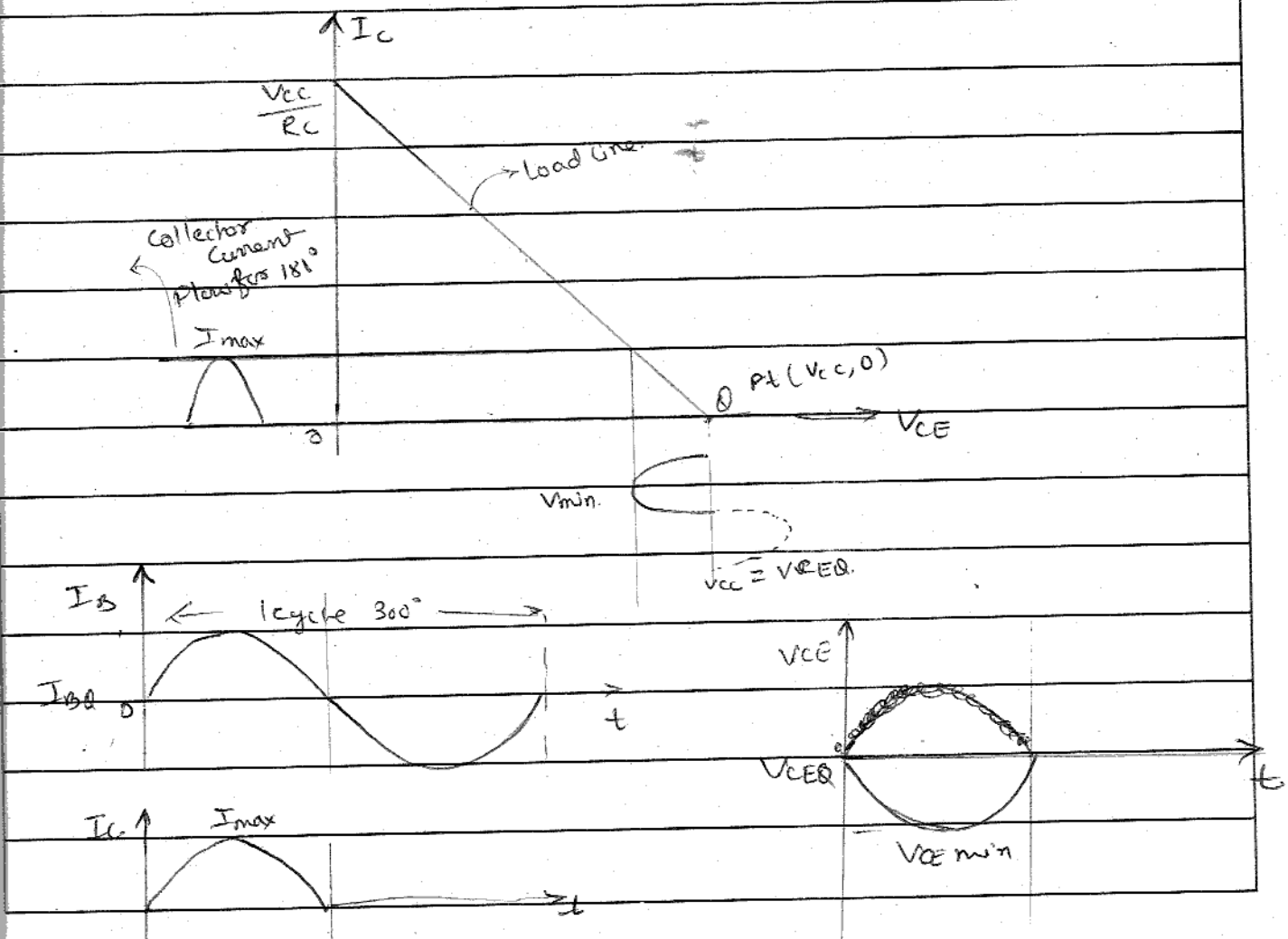




Class B Ampl.:-

The power ampl. is said to be class B ampl. if the Q point and the i/p signal are selected, such that the o/p signal is obtained only for one half cycle for a full i/p cycle. for this operation, the Q point is shifted on x-axis ie. transistor is biased to cut-off.

Due to the selection of Q point on the x-axis, the transistor remains in the active region, only for the +ve half cycle of the i/p signal Hence this half cycle is reproduced at the o/p. But in a negative half cycle of the i/p signal the transistor enters into a cut-off region and no signal is produced at the o/p. The Collector current flows only for 180° (half cycle) of the I/p signal. In other word, the angle of the Collector current flow is 180° i.e one half cycle.



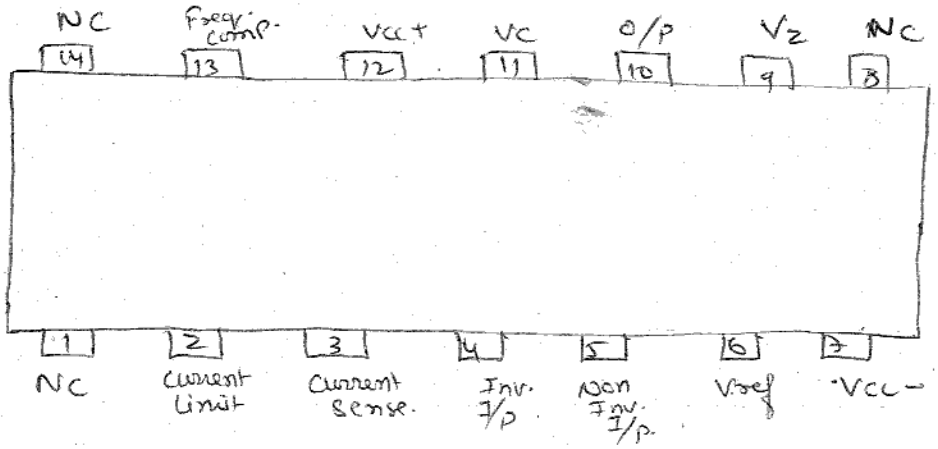
As only a half cycle is obtained at the O/p for full I/p cycle, the output signal is distorted in this mode of operation. To eliminate this distortion, practically two transistors are used in the alternate half cycle of the I/p signal. Thus overall a full cycle of O/p signal is obtained across the load. Each transistor conducts only for a half cycle of the I/p signal.

Efficiency of class B is much higher than class A

Q3 Explain in detail the T23 IC general purpose voltage regulator.

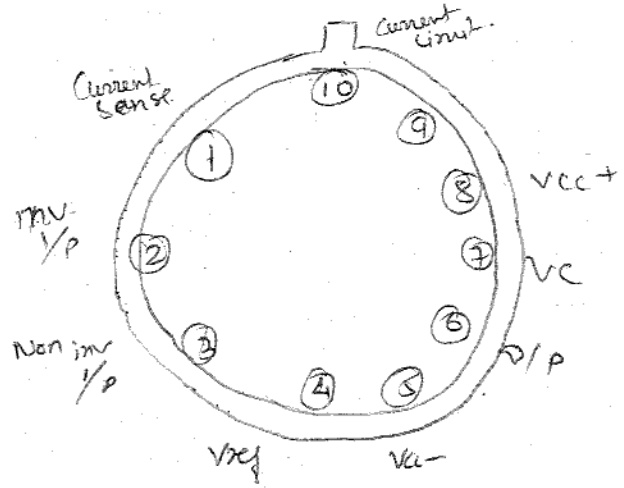
Soln It is a monolithic linear integrated circuit in different physical package.

The pin diagram along with the various packages is shown in fig.



J or N dual in line package (top view)

(V-plug in package) (top view)



(b)

Important features of IC 723:-

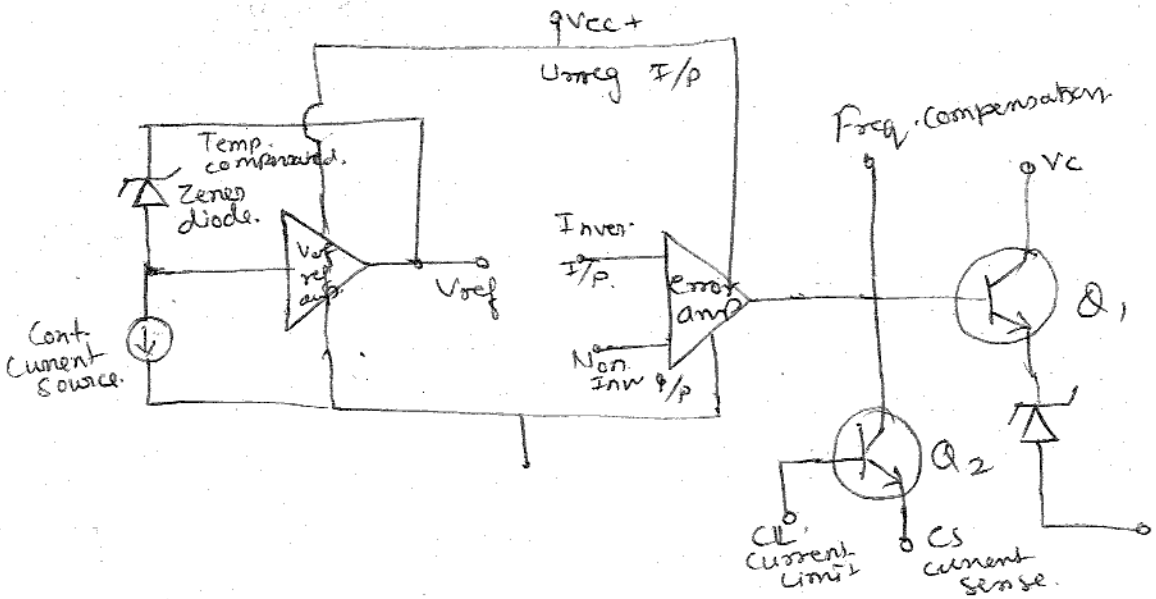
1) It works as voltage regulator at o/p voltage ranging from 2 to 37 volts at current upto 150 mA.
2) It can be used at load current greater than 150mA with use of suitable NPN or PNP external pass transistor.
3) I/p and o/p short-circuit protection is provided.
4) It has good line and load regulation (0.03%)
5) Wide variety of applications of series, shunt, switching and floating regulator.
6) Low temp drift and high ripple rejection.
7) Low standby current drain.
8) Small size lower cost.
9) Relative ease with which power supply can be designed.
10) It provides a choice of supply voltage.

Internal structure:-

The functional block Diagram of IC 723 can be divided into four major blocks.

1) Temp compensated voltage reference source, which is zener diode.
2) An op-amp circuit used as an error amplifier.

3) A series pass transistor capable of an 150mA o/p current
4) Transistor used to limit o/p current.



Temp. compensated zener diode cont. current source and reference ampl. constitutes the reference element. Output voltage is compared with this temp compensated reference potential of the order of 7 volts for this, Vref is connected to the non-inverting I/p of the error ampl.

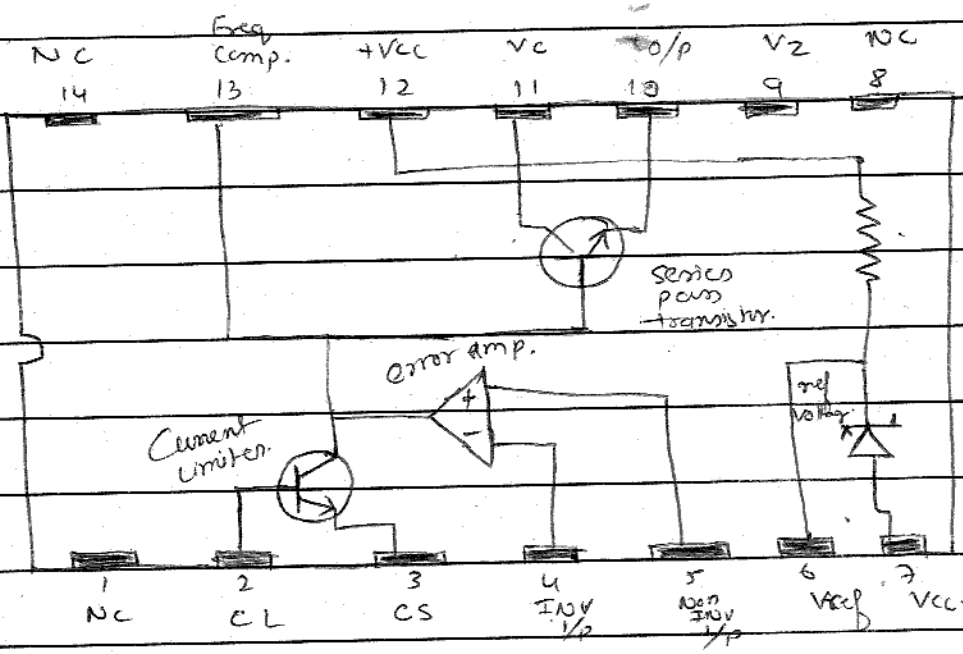
This error amplifier is high gain differential amplifier. It's inverting I/p is connected to the either whole regulated o/p voltage or part of that from outside for later case a potential divider of two scaling resistor is used. Scaling resistors help in getting multiplied reference voltage or scaled up reference voltage.

Error amplifier controls the series pass transistor Q_1 which act as variable resistor. The series pass transistor is a small power transistor having about 800 mW dissipation. The unregulated power supply source is connected to collector of series pass transistor.

Transistor Q_2 acts as current limiter in case of short circuit condition. It senses drop across R_{sc} placed in series with regulated o/p voltage externally.

The frequency compensation terminal controls the frequency response of the error ampl. The reqd. roll-off is obtained by connecting a small capacitor of 100 pF b/w freq. compensation and inverting I/p terminal.

The internal structure can be represented in more simplified form as shown in fig.



Both non-inverting and inverting terminals of the error ampl. are available on outside pins of IC 723. Due to this device becomes versatile and.

Flexible to use. Only restriction is that internal reference voltage is 7 volts and therefore we have to use two different ckt for getting regulated o/p of below 7 volts and above 7 volts.

Application:

1) Basic low-voltage regulator
2) Low voltage High current Regulator
3) Basic positive Hig voltage Regulator
4) Positive High voltage High current Regulator.
5) Negative Voltage Regulator.

Q5 Draw and explain the operation of switching regulator Give its adv.

Sol^n The operating principle of switching regulator is completely different than that of linear regulators. The switching regulator are also called as switched mode regulators.

Such a switching regulator requires an external transistor and a chock The series pass transistor in such a regulator is used as a controlled switch and is operated in cut-off region or saturation region. Hence the power transmitted across such a transistor is in the form of discrete pulse rather than a steady flow of current.

When the transistor is operated in the cut-off region there is no current and dissipates no power. while when it is operated in the saturation region, a negligible voltage drop appears across it and hence dissipates very small power, providing maximum current to load. In any case, the power dissipated in the transistor is very small. Almost the entire power gets transmitted

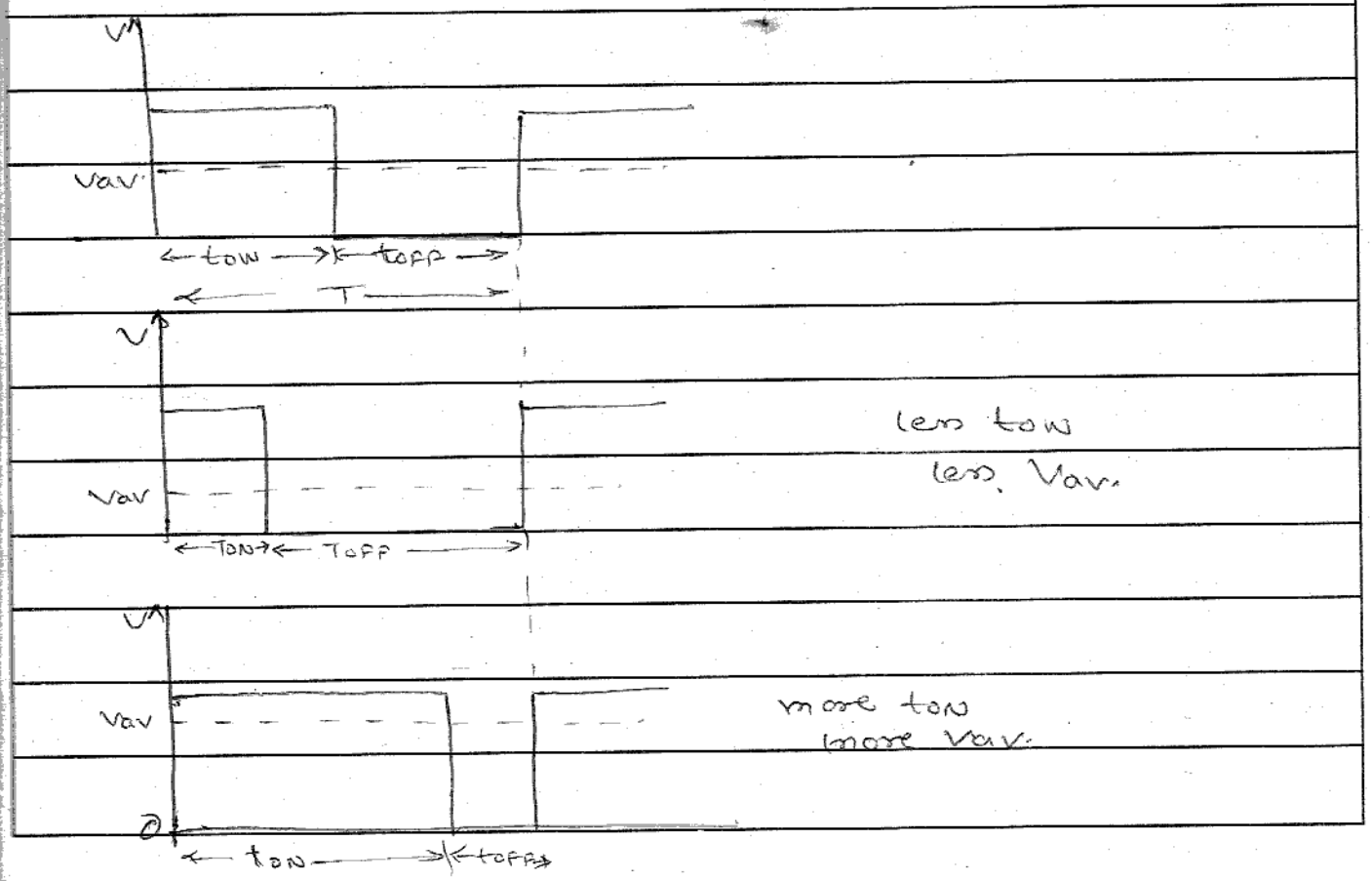
to the load. Hence the efficiency of the switching regulator is always very high.

So switching regulator use the fact that if duty cycle of the pulse waveform is varied the avg value of the voltage also changes proportion al to it.

Mathematically it can be expressed as,

$$\text{duty cycle } \delta = \frac{t_{ON}}{t_{ON} + t_{OFF}}$$

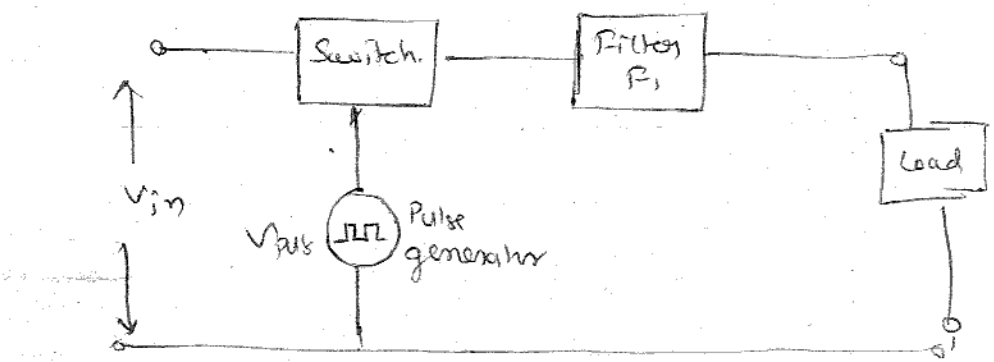
$$\boxed{\delta = \frac{t_{ON}}{T} = t_{ON} f}$$



Pulse Width modn

The basic Switching regulator consists of four major compone-

a) voltage source.
b) Switching transistor
c) Pulse generator, V_{pulse}
d) Filter F_1



Basic Switching regulator.

A voltage Soure V_{in} is a dc supply which is a battery un regulated voltage.

It has to satisfy the requirement as.

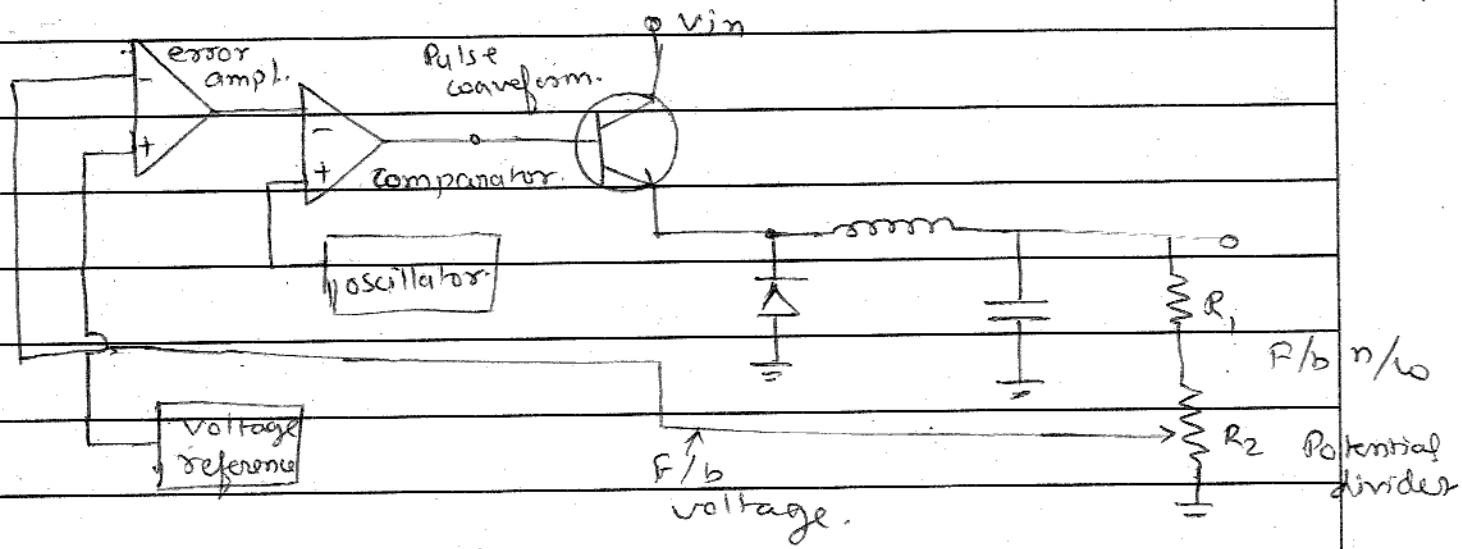
i) It has to supply required power and the losses associated with the regulator.

ii) It must be high to satisfy the mini requirements of the regulator.

iii) It must be larger to supply sufficient dynamic range of line and load changes.

The switch is generally a transistor. The pulse generator o/p makes it on and off. The pulse generator produces a required pulse waveform. the most effective-range pulse waveforms frequency is 20kHz. the typical operating frequency range 10 to 50 KHz the filter f_1 may be RC, RL or RLC most commonly used filter is RLC, it converts the pulse waveforms obtain from to switch into a dc o/p waveform.

Functional Block Diagram of Switching generator



The part $R_2/R_1 + R_2$ of the o/p is f/b to the inverting i/p of error ampli It is compared with the refference voltage. The difference is amplified and given to the comparator inverting terminal.

The Oscillator generates a triangular waveform at a fixed frequency it is applied to the non-inv terminal of the Comparator. The o/p of the comparator is high when the triangular voltage waveform is above the level of the error amplifying o/p. Due to this the transistor Q remains in cut off status. Thus the o/p the comparator is nothing but a requried pulse waveform.

The period of this pulse waveform is same as that of oscillator o/p say T the duty cycle. is

denoted as $\delta = \frac{t_{ON}}{T}$ or $t_{ON} f$. This duty cycle is controlled by the difference b/w the f/b voltage and the reference voltage.

When Q_1 is on in saturation state, $V_{CE(sat)}$ for Q_1 is zero. Hence entire i/p voltage V_{in} appears at point A. Thus the current flows through inductor L,

When Q_1 is OFF, L, still continues to supply current through itself to the load. The Diode D_1 provides the return path for the current.

The capacitor C_1 acts to smooth out the voltage and the vltge at the o/p is almost dc in nature. The o/p voltage V_o of the switching regulator is a function of duty cycle and the i/p voltage V_{in}. mathimatically expression

$$V_o = \frac{t_{ON}}{T} V_{in} = \delta V_{in}$$

Thus when T is cont. o/p is proportional to t_{ON} - This method is called PWM when t_{ON} is cont. the o/p is inversely proportional to the period T i.e. proportional to freq of the pulse waveform this method is called freq modn.

A high switching freq allows small values of L_1 and C_1 and thus reduces size, cost and weight. It also reduces the ripple at the o/p. But the efficiency decreases and electrical noise increases on the other hand low switching freq improve efficiency and reduce noise but require large filtering component. as a result of this, the range of operating freq. to get maxm efficiency is 10 to 50 KHz.