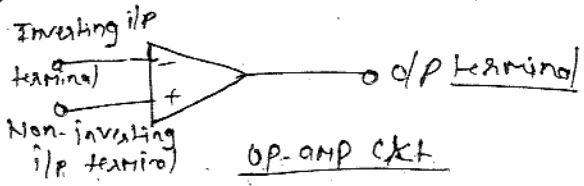
LIC

UNIT - I

1) The operational amplifier is a multi-terminal device which internally is quite complex. Op-amp's performance can be completely described by its terminal characteristics.

The circuit of op-amp is a triangle. It has two input terminal and one output terminal. The terminal with a (−) sign is called inverting i/p terminal and the terminal with (+) sign is called the non-inverting input terminal.



Op-amp ckt

2) Characteristics

(i) Open loop voltage gain, $A_{OL} = \infty$

(ii) Input impedance, $R_i = \infty$

(iii) Output impedance, $R_o = 0$

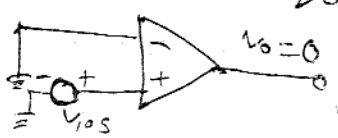
(iv) Bandwidth : $BW = \infty$

(v) Zero offset, i.e. $V_o = 0$ when $V_1 = V_2 = 0$

3) The common terminal of the V^+ and V^- sources is connected to a reference point or ground. The common point of the two supplies must be grounded, otherwise twice

the supply voltage will get applied and it may damage the op-amp.

(4) Inspite of the use of the compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminal to make o/p voltage zero. this voltage is called input offset voltage.



OFF-set voltage

(5) Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference b/w I_B^+ and I_B^-. This difference is called the offset current I_{os} and can be written as

$$|I_{os}| = I_B^+ - I_B^-$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Even with bias current compensation, offset current will produce an output voltage when the i/p voltage V_i is zero.

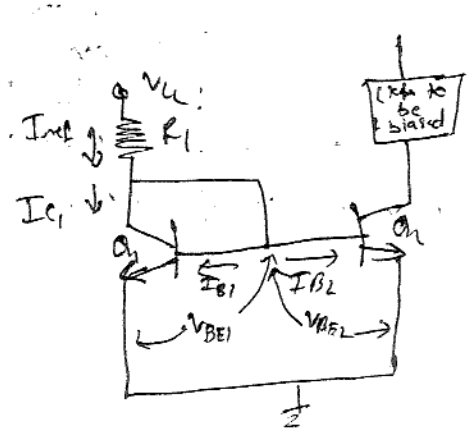
(6) The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit ρ for the differential amplifier amplifier. So, CMRR is given by

$$\rho = \left| \frac{A_{DM}}{A_{CM}} \right|$$

and is usually expressed in decibels (dB).

(7) A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector voltage. Transistor Q_1 and Q_2 are matched as the circuit is fabricated using IC technology.

(8) above and the bases and emitter of Q_1 and Q_2 are tied together and thus have same V_{BE}. In addition, transistor Q_1 is connected as a diode by shorting its collector to base



Current source

(9) (1) The value of the Resistance R required is sufficiently high and can not be fabricated economically in IC circuit.

(2) Widlar current source is suitable for low value of currents.

(10) It is a rate of change of o/p voltage with respect to time.

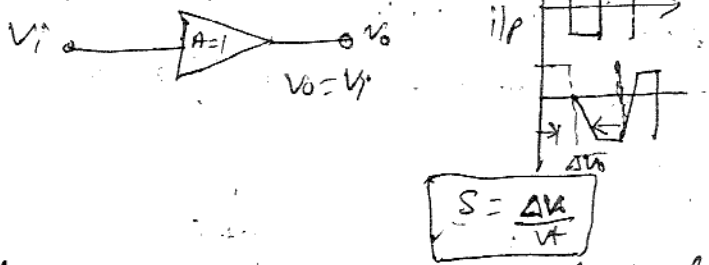
$$S = \frac{\Delta V_o}{\Delta t} \Big|_{V_{in}}$$

It is cause due to limited charging rate of compensating capacitor

$$C = I/V$$

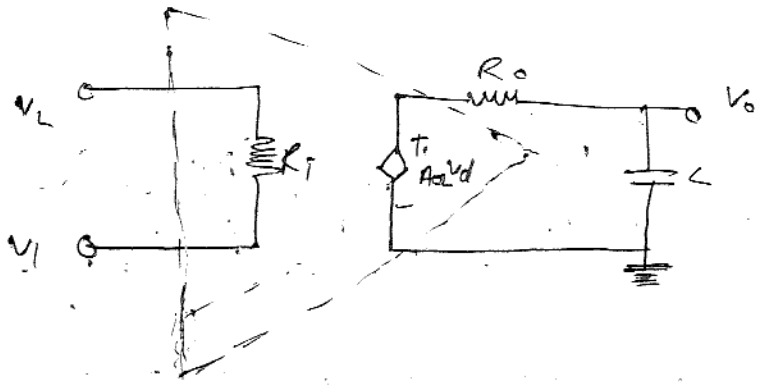
Slew rate whose maxm internal capacitor charging current is known

$$\frac{dv_c}{dt} = I/C$$



Ideally slew rate should be infinit for better performance of op-amp.

(11)



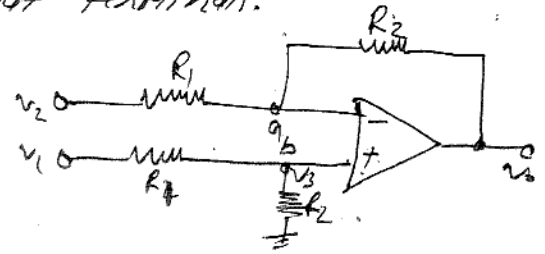
(12) In application where one desires large bandwidth and lower closed loop gain, suitable compensation techniques are used i.e frequency compensation.

Two types of F.C

(i) External compensation (ii) Internal compensation.

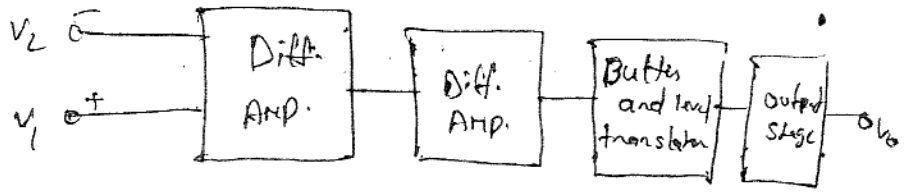
- Dominant-pole compensation
- pole-zero compensation.

(13) A circuit that amplifies the difference b/w two signal is called a difference or differential amplifier. It is provide high gain to the difference mode signal and cancel the common mode signal. it is able to suppress any undesired noise which is common to both of the input terminals.



Type

(17)



(18) 741, 741C, 741A, 741E, 741S. 741SC.

741 — Military grade op amp
741C — Commercial grade op-amp
741A — Improved version of 741
741E — Improved version of 741C
741S — Military grade op-amp with higher slew-rate.
741SC — Commercial grade op-amp with higher slew-rate.

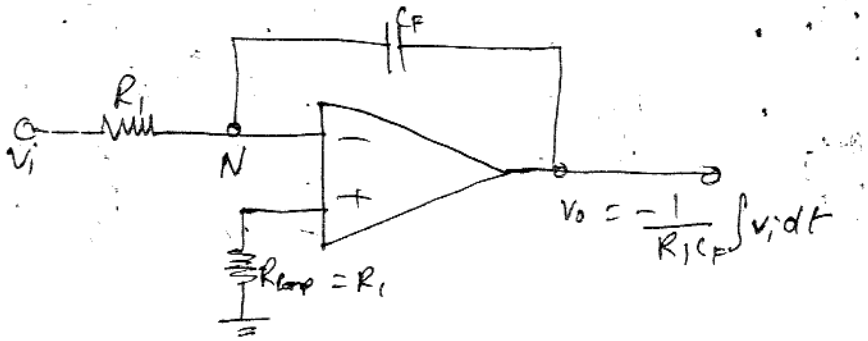
(20) The open circuit voltage gain of an op-amp should be as large as possible and this is achieved by cascading gain stages. However, this increases the phase shift too and amplifier becomes more susceptible to breaking out into oscillations.

(19) R_E is replaced by a constant current transistor circuit in which R_1, R_2 and R_3 can be adjusted to give the same quiescent condition for the transistor Q_1 and Q_2. The modified circuit presents a very high effective emitter resistance R_E even for very small values of R_3.

UNIT-2

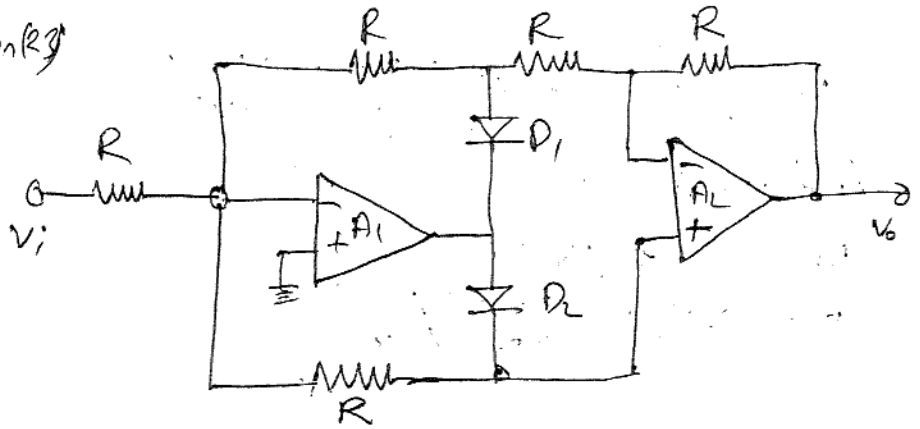
(1) Characteristics of instrumentation Amplifier
1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature coefficient
4. low dc offset
5. low output impedance

(4)



Op-amp integrator

(6) onRg

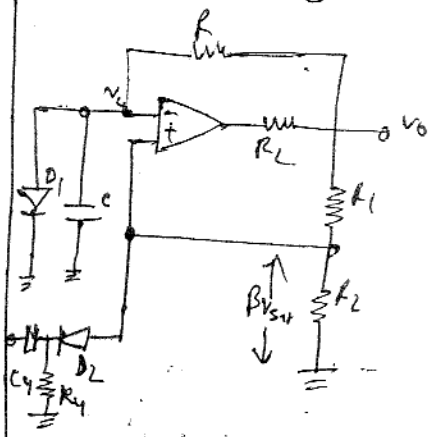


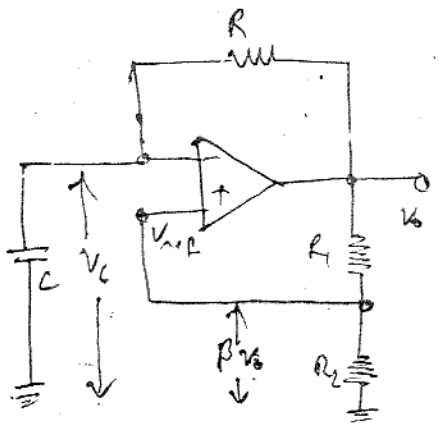
(25) (1) Monostable multivibrator has one stable state and the other is quasi stable state.

Gn astable multivibrator both the states are quasi stable.

(20) The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal

The principal of generation of square wave output is to force an op-amp to operate in the saturation region.





(21) Log amplifier —

$$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

$$V_{o\,comp} = \left(1 + \frac{R_2}{R_{TC}}\right) \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right)$$

Antilog amplifier

$$V_o = V_{ref}(10^{-k' V_i})$$

$$k' = 0.4343 \left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)$$

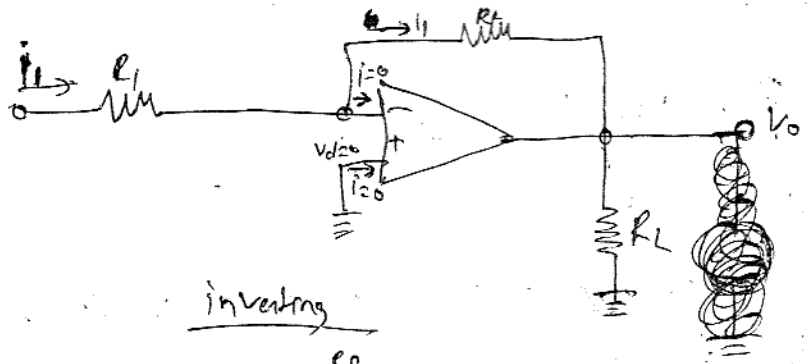
(22) Multivibrator — The electronic circuit which is used to generate the non-sinusoidal waveform are called multivibrator.

types

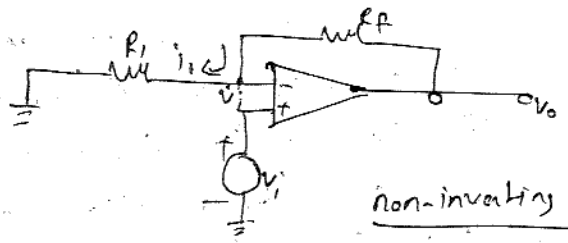
Monostable multivibrator

Astable "

(21)



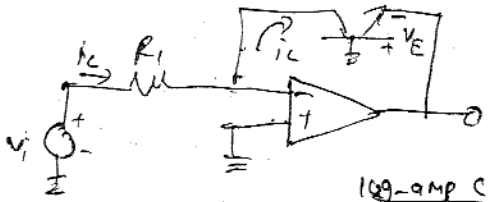
inverting



non-inverting

(20) (i) The function such as $\ln x$, $\log x$ or $\sin x$ can be performed continuously with log-amps. Log-amp can easily perform this function.

(ii) Log-amp can also be used to compress the dynamic range of a signal.

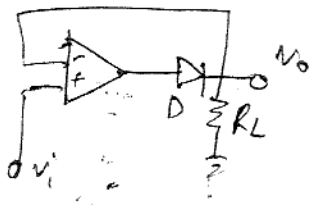


log-amp ckt

(19) Application of precision diode

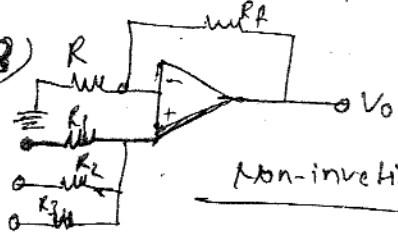
(i) Half-wave rectifier
(ii) Full-wave rectifier
(iii) Peak value detector
(iv) Clipper
(v) Clamper.

(18) The circuit acts like a voltage follower for input V_i and the output V_o follow the input voltage V_i during the positive half cycle. When V_i is negative or less than V_γ/A_{OL}, the Diode D is off and no current is delivered to the load R_L except for small bias current of the op-amp and the reverse saturation current of the diode is called Precision diode.



- Precision diode

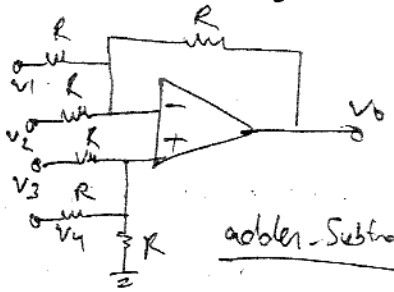
(7) - The op-amp is used in non-inverting mode
- The i/p impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source.
- A V to I converter is used for low voltage dc and AC voltmeter, LED and Zener diode tester.

(8) 

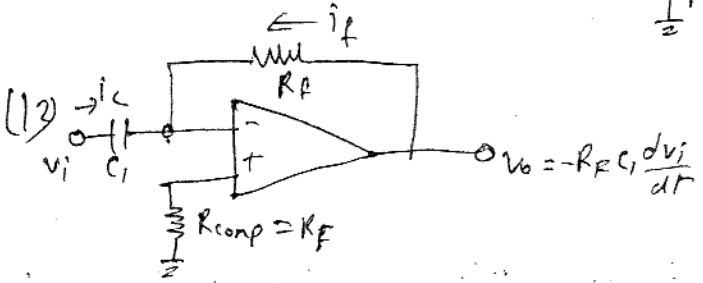
Non-inverting Summing amplifier

Equation - $V_o = \left(1+\frac{R_f}{R}\right)\frac{\left(\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}\right)}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}}$

(9) $V_o = V_{o1}+V_{o2}+V_{o3}+V_{o4}$
$= -V_1 - V_2 + V_3 + V_4$
$= (V_3+V_4)-(V_1+V_2)$



adder-Subtractor

(12) 

(13) (i) At high frequency, a differentiator may become unstable and break into oscillation.
(ii) The input impedance (X_{C_1}) decrease with the increase in frequency, thereby making the circuit sensitive to high frequency noise.

(15) Application of linear op-amp

- The output signal varies with the input signal in a linear manner.
- Some of the linear application - adder, subtractor, voltage to current converter and current to voltage converter, instrumentation amplifier, analog computation, power amplifier.

(16) Application of non-linear op-amp

- Rectifier, peak detector, clipper, clamper, sample and hold circuit, log and antilog amplifier, multiplier.
- Non-linear ckts are very useful in industrial instrumentation, communication and general signal processing.

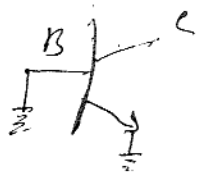
Precision Diode Rectifier

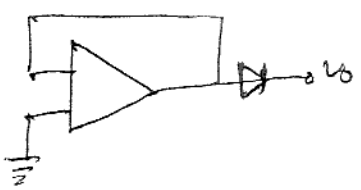
Cut in Voltage of diode ≃ 0.6 V

Ideal diode : cannot operate below cut in voltage

But precision diode rectifier can operate below the cut in voltage i.e in millivolt

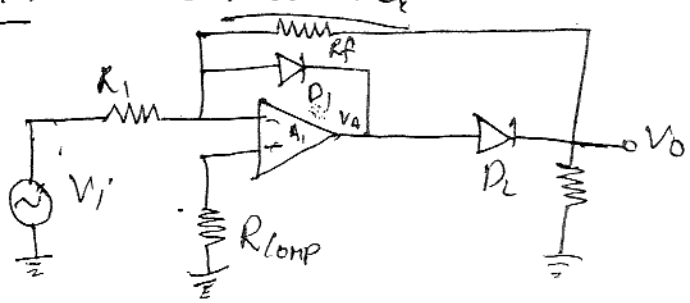
To make transistor to an diode—





this circuit is called precision diode by connecting a diode in the feedback path of an op-amp & this circuit is capable of rectifying input signal of milli-volt.

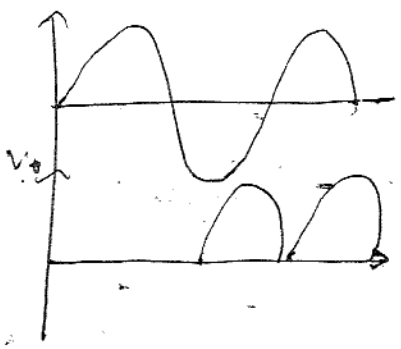
Half wave Rectifier



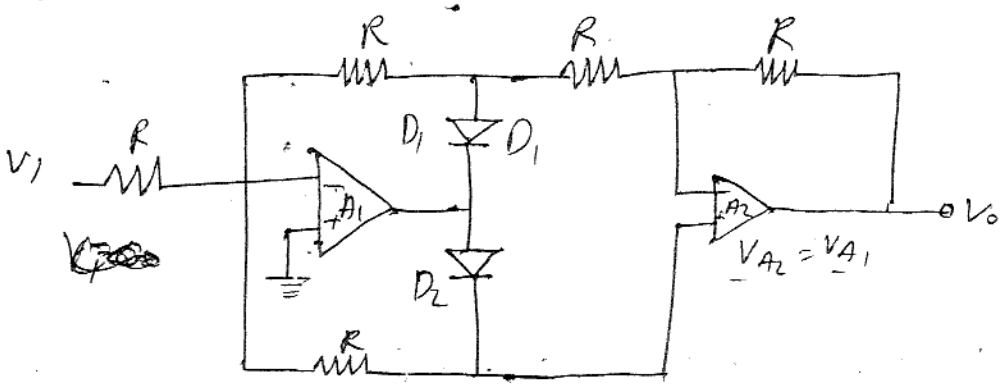
Analysis

$V_i > 0V$
↳ +ve
$D_1 \rightarrow$ conducts
$D_2 \rightarrow$ OFF
$V_o = 0$

$V_i < 0V$
$D_1 \rightarrow$ OFF
$D_2 \rightarrow$ ON
$V_o \rightarrow$ ON

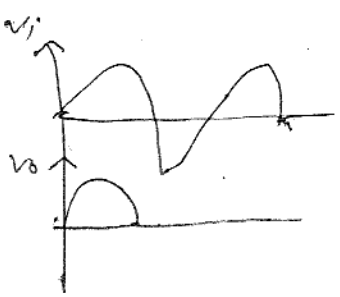


Full wave rectifier



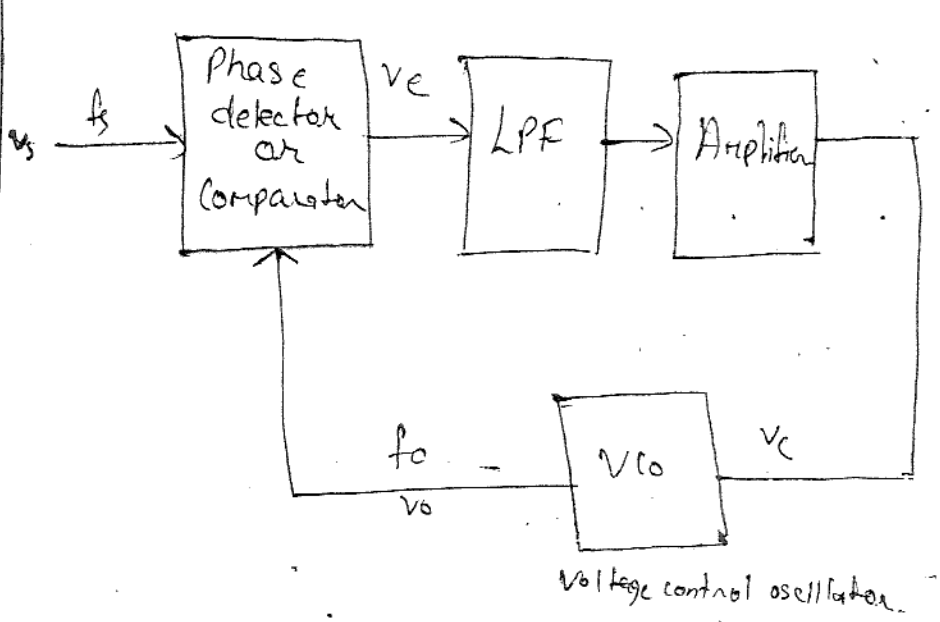
Both op-amp act as inverter so the o/p voltage V_o = input voltage.

When
$V_i > 0$
$D_1 \rightarrow$ ON
$D_2 \rightarrow$ OFF
$V_o = V_i$



UNIT-3

PLL (phase locked loop)



(1) Phase detector / comparator

O/P → (fs+fo) (fs-fo)

(fs+fo) → it filters the high frequency

V_c → dc voltage

[$V_o \propto V_c$]

Basic term in PLL

→ Lock-in range → fs = fo

UNIT-3

(2) and (11) The range of frequency over which the PLL can maintain lock with the incoming signal is called the lock range. The lock range is usually expressed as a percentage of f_o, the VCO frequency.

(4) A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_o}{\Delta V_c}$$

Here ΔV_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO.

(6) The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_o.

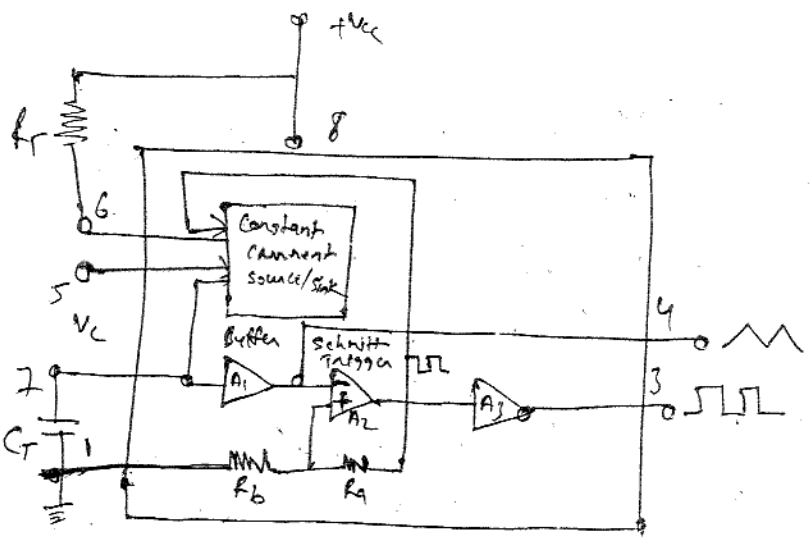
(7) Application of PLL

(1) Frequency multiplication/Division.
(2) Frequency Translation.
(3) AM detection
(4) FM demodulation
(5) FSK demodulator.

(8) and (21) The VCO is a free running multivibrator and operates at a set frequency is called free running frequency. This frequency

is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage V_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a VCO.

(14)



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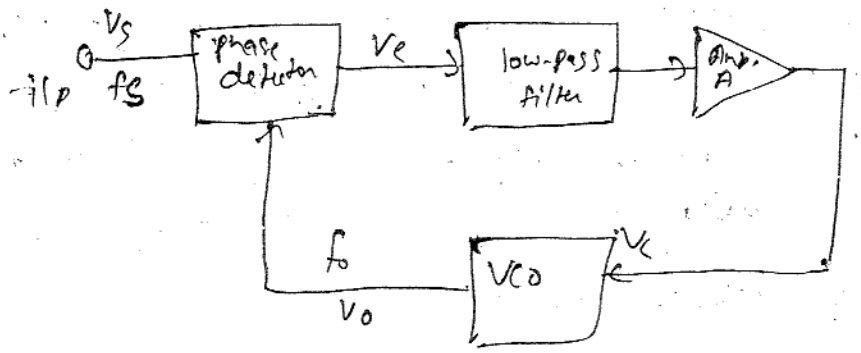


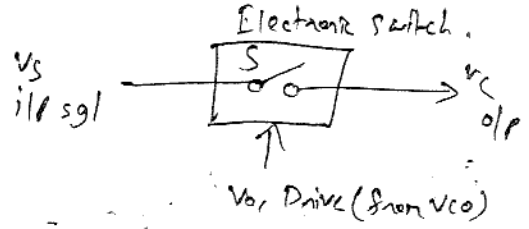
(17) Three stages

(1) Free running (2) capture (3) locked or tracking

(18) Phase detectors

(1) Analog P.D (2) Digital P.D.

(19) Switch type phase detector is used in analog phase detector. An electronic switch S is opened and closed by signal coming from VCO. The input signal is, therefore chopped at a repetition rate determined by VCO frequency. i.e the switch is only dependent on VCO.

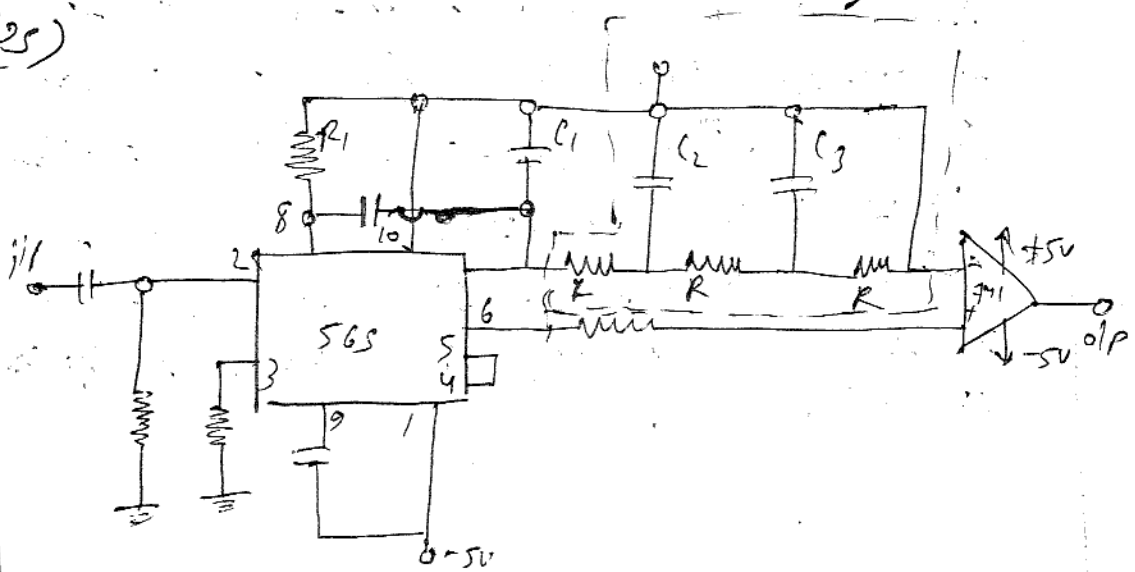


(20) Two problem

(1) The output voltage Ve is proportional to the input signal amplitude Vs. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.

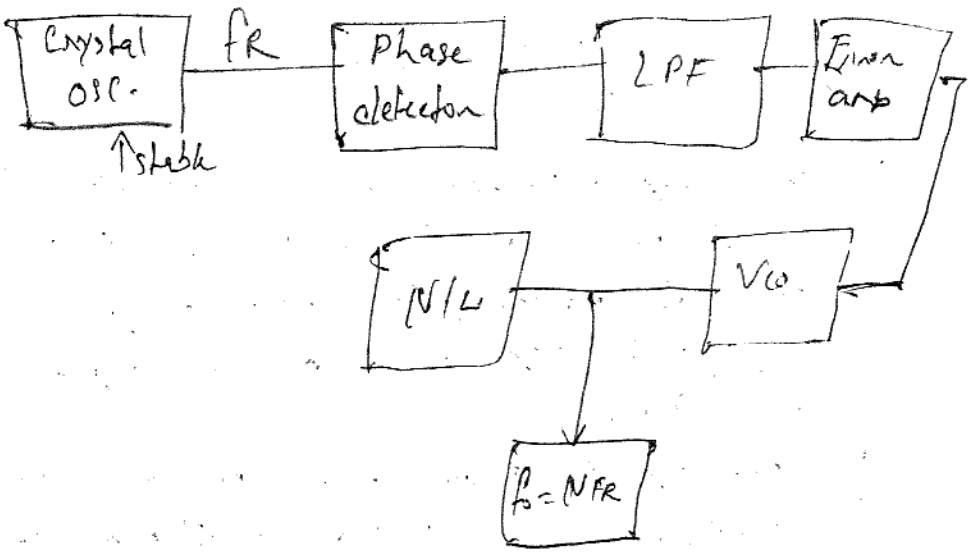
(2) The o/p is proportional to cos Φ and not proportional to Φ making it non-linear.

(25)



(23) In order to increase the ability of lock-in range, large capture range is required. A large capture range will make the PLL more susceptible to noise and undesirable signal."

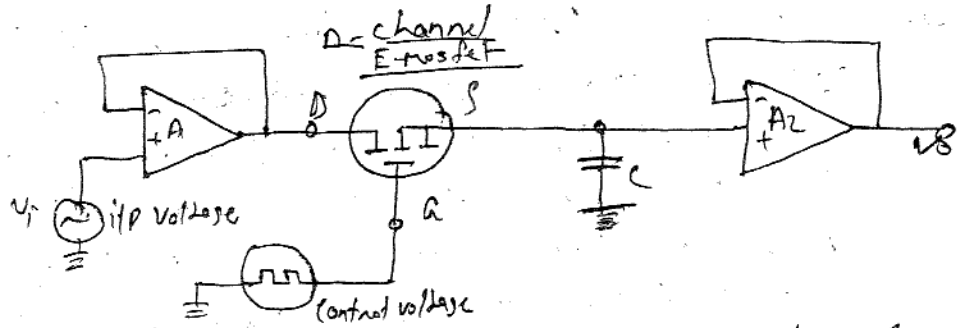
(24)



PLL can be used as the basis for frequency synthesizer that can produce precised frequencies from a single oscillator. Under locked condition o/p frequency of VCO is n times the reference frequency therefore it is possible to obtained multiples of reference frequency.

UNIT-4

(1) A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation system.



(2) The D/A converter is to convert digital signal into analog signal and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The o/p of a D/A converter is commonly a staircase. This staircase like digital o/p is passed through a smoothing filter to reduce the effect of quantization noise.

Classified

(1) Weighted Resistor DAC (2) R-2R ladder DAC (3) Multiplying DAC's (4) Monolithic DAC

(3) 8-op-amp comparators are required to build an n bit flash type A/D converter. A small amount of hysteresis is built into the comparator to resolve any problems that

might occur if both inputs were of equal voltage.

(4) R-2R ladder n/w DAC is better than weighted resistor DAC because a wide range of resistor are required in binary weighted resistor type DAC but in R-2R ladder type DAC only two values of resistor are required.

(6) Monolithic DAC consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. A monolithic DAC is the one whose analog o/p increases for an increases in digital i/p. If a DAC has to be monotonic, the error should be less than ±(1/2)LSB at each o/p.

(8) The most important dynamic parameter is the settling time. It represents the time it takes for the o/p to settle within a specified band ±(1/2)LSB of its final value following a code change at the input. It depends upon the switching time of the logic circuitry due to internal parasitic capacitance and inductance.

(11) The successive approximation technique uses a very efficient code search strategy to complete n-bit conversion in just n-clock periods. An eight bit converter would

required eight clock pulses to obtain a digital o/p. Circuit uses SAR to find the required value of each bit by trial and error.

(18) Weighted resistor DAC is the simplest DAC
→ The op-amp is connected in inverting mode, it can also be connected in non-inverting mode.
→ The op-amp is simply working as a current to voltage converter.
→ The polarity of the reference voltage is chosen in accordance with the type of the switch used.

(19) Integrating type converters are—
(i) charge balancing ADC.
(ii) Dual slope ADC.

(20) Integrating type ADCs perform conversion in an indirect manner by first changing the analog input signal to a linear function of time or frequency and then to a digital code. The two most widely used integrating type converters are—
(i) charge balancing ADC
(ii) Dual slope ADC.

(7) (a) Digital interfacing (b) Analog to digital converter circuits (c) Pulse modulating system. (d) Instrument-stabilized op-amp. (e) In analog demultiplexers.

(22) (1) The primary use of the sample and hold circuit to hold the sampled analog input voltage constant during conversion time of A/D converter.

(2) In case of multichannel ADCs, synchronization can be achieved by sampling signals from all channels at the same time.

(3) It also reduces the crosstalk in the multiplexer.

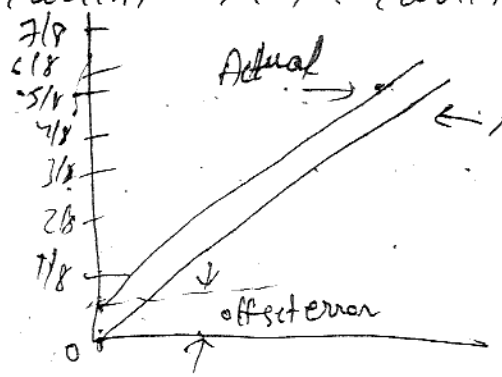
(23) Parameter of ADC

(1) Resolution, (2) Quantization error
(3) Convertion time.

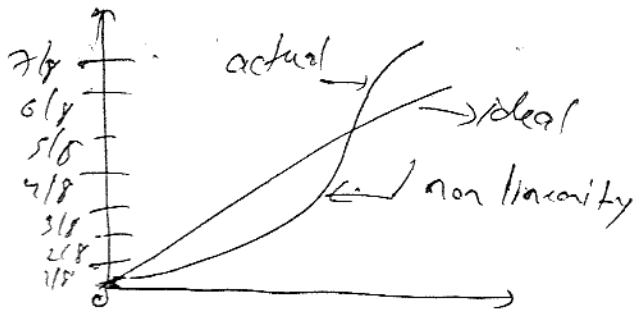
Parameter of DAC

1) Resolution. (2) Accuracy (3) monotonicity
(4) Convertion time (5) settling time (6) stability.

(24) Offset error — The offset error is defined as the non zero level of the o/p voltage when all inputs are zero. It is due to the presence of offset voltage in op-amp and leakage current in the current switches.



Linearity error – The error is defined as the amount by which the actual o/p differs from the ideal straight line o/p. It is mainly due to the errors in the current source resistor value.



(25) Suppose the binary o/p is 011 for all values of V_i btw 1/4 and 1/2 V. There is an uncertainty about the exact value of V_i when the o/p is 011. This uncertainty is specified as quantization error. Its value is $\pm \frac{1}{2}$ LSB.

it is given as,

$$Q_E = \frac{V_{FS}}{(2^n - 1)2}$$

(21) It is a time required for conversion of analog signal into its digital equivalent. It is also called as setting time. It depends on the response time of the switches and the o/p of the amplifier in DAC and in ADC is depends upon the conversion techniques and the propagation delay of the circuit components.

(22) It is a comparison of actual o/p voltage with expected o/p. It is expressed in percentage. Ideally, the accuracy of DAC should be, at worst ± 1/2 of its LSB. If the full scale o/p voltage is 10.2 V then for an 8-bit DAC accuracy can be given as—

$$\text{Accuracy} = \frac{V_{FS}}{(2^n - 1)2} = \frac{10V}{255 \times 2} = 20mV.$$

(18)

Single slope	Dual slope
1) It consists of a ramp generator and BCD or binary counters.	1) It consists of ramp generator, comparator, binary counter, o/p latch and reference voltage.
2) The analog input voltage V_{in} is applied to the positive terminal of the comparator.	2) Ramp generator input is switched b/w the analog input voltage V_i and a negative reference voltage, $-V_{REF}$.

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(2) The o/p of rectifier and filter circuit consists of ripples. The ripple is equivalent to periodic changes in input voltage. Due to the negative feedback, the ripple voltage gets attenuated by large amount. The factor by which it gets reduced is $1+AB$. Mathematically the o/p ripple of a voltage regulator is given by -

$$V_r(out) = \frac{V_r(in)}{1+AB}.$$

(3) or (6) Switching regulators operate the power transistor as a high frequency on/off switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulator.

(5) Two packages — (1) 8-pin circular style
(2) TO-99 can or 8-pin mini DIP or as 14-pin DIP.

(7) line regulation — It is defined as the change in the o/p voltage for a given change in the i/p voltage. It is expressed as a percentage of o/p voltage or in millivolts.

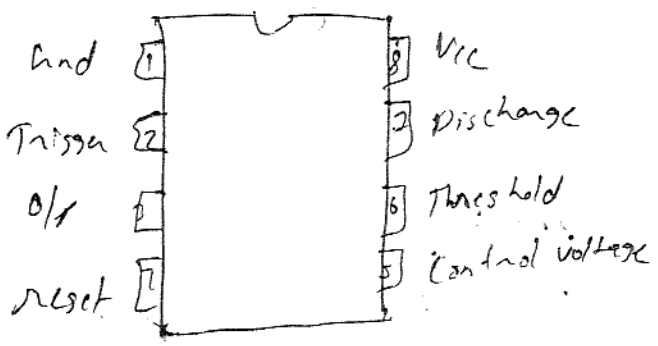
(10.) (i) 555 is a monolithic timer device which can be used to produce accurate & highly stable time delay. It can be used to produce time delay of few ms to several ms.

(ii) It has 2 - basic operating mode - astable & monostable.

(iii) Available in 3 packages - 8 pin metal can, 8-pin mini DIP, 14 PIN DIP. 14 pin package is IC 555 & 556.

(iv) O/P is capatible with TTL, CMOS & op-amp.

(11)



(22) (i) Very high value of resistors can be easily simulated using small value capacitors of the order of 10 pF.

(ii) The switched capacitor filters require no external reactive components like inductors and capacitors.

(iii) Accuracy is very high.

(iv) Overall cost of the system is low.

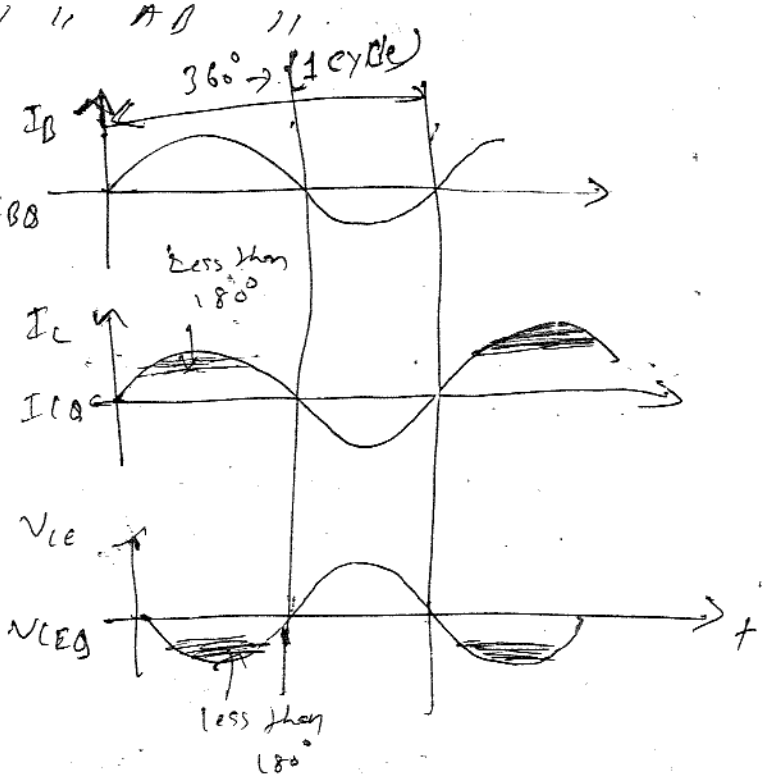
(v) Due to good temperature char., the system have good temperature stability.

(23) The power amplifiers are classified by their classes of operation. The class of operation represents the amount of the o/p signal varies over one cycle of operation for a full cycle of input signal.

For an amplifier, a quiescent point (Q point) is fixed by selecting the proper dc. biasing to the transistor used. The position of the Q point on the load line decides the class of operation.

→ (i) Class A amplifier.
(ii) " B "
(iii) " C "
(iv) " AB "

(24)



classified
the
amount
cycle
input

resent
the
used,
the load

(17) · types of voltage regulator

① Series regulator
② Switching "

(18) Duty cycle – Generally the charging time constant is greater than the discharging time constant hence at the o/p, the waveform is not symmetric. The high o/p remains for longer period than low o/p. The ratio of high o/p period and low o/p period is given by a mathematical parameter called duty cycle. It is defined as the ratio of ON time i.e high o/p to the total time of one cycle.

$$D = \frac{W}{T}$$

(19) The combined package of a LED and a photodiode is called an optocoupler. It is also called an optoisolator or an optically coupled isolator.

Advantage

(1) The response times of optocouplers is so small that they can be used to transmit data in the megahertz range.
(2) Capable of wide band signal transmission.
(3) Easy interfacing with logic device.
(4) Compact and light weight.
(5) Much faster than isolation transformers and relays.

(12) (i) FSK Generator
(ii) Pulse position modulation

(12) An isolation amplifier is an amplifier that offers an ohmic or electrical isolation b/w its input and o/p terminals. Isolation amplifiers are often used when there is a very large common-mode voltage difference b/w the input and o/p sides of the device. The isolation in the isolation amplifier is achieved by use of transformer or by use of optically coupled devices

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