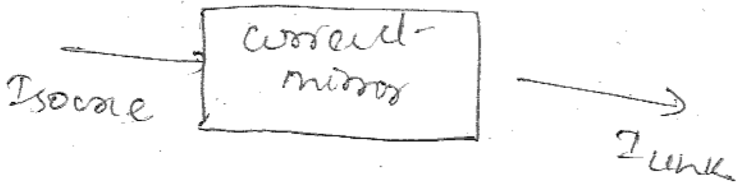
UNIT - I

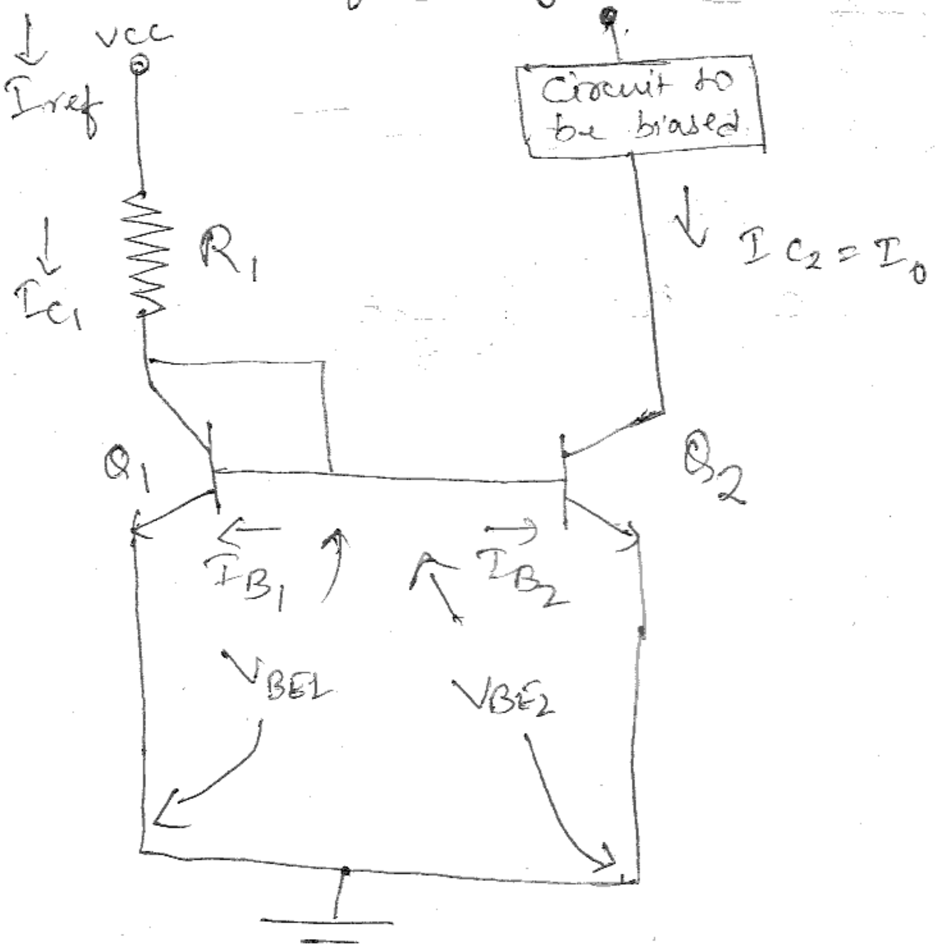
Current Source & Current Mirror

Current Mirror is the ckt whose o/p current is the replica of the current sent at its input.



Constant Current source :-

An Ideal constant current source is an Electric circuit that supplies a constant current to the load i.e. independent of voltage across the load.



Operation

1) Q_1 & Q_2 are matched as the circuit is fabricated using IC technology.

2) Base & Emitter of the transistors Q_1 & Q_2 are tied together, thus V_{BE} is same. i.e. $V_{BE_1} = V_{BE_2}$.

3) I_{ref} flows through diode of the transistor Q_1 and establishes the voltage across Q_1. This voltage appears between base & emitter of Q_2.

4) Since Q_1 is identical to Q_2

$$I_{BE_2} = I_{BE1} \simeq I_{ref}$$

5) As long as Q_2 is maintained in the active region.

$$I_{C_2} = I_O \simeq I_{ref}$$

6) Since the o/p current I_O is the reflection of the reference current I_{ref} the circuit is often reffered as current mirror.

Analysis

from the CKT

i) The base emitter voltages of 2 transistors are equal i.e, $V_{BE_1} = V_{BE_2}$

ii) The collector currents are also Equal : $I_{C_1} = I_{C_2}$

To find the reference voltage

$$~~V_{ref}~~ \; I_{ref} = I_{C_1} + I_{B_1} + I_{B_2}$$

$$I_{ref} = I_C + 2I_B$$

(Since $I_{C_1} = I_{C_2} = I_C$, $I_{B_1} = I_{B_2} = I_B$)

$$I_{ref} = I_C + \frac{2I_C}{\beta} = I_C\left(1 + \frac{2}{\beta}\right)$$

$$\Rightarrow I_C = \frac{I_{ref}}{\left(1 + \frac{2}{\beta}\right)}$$

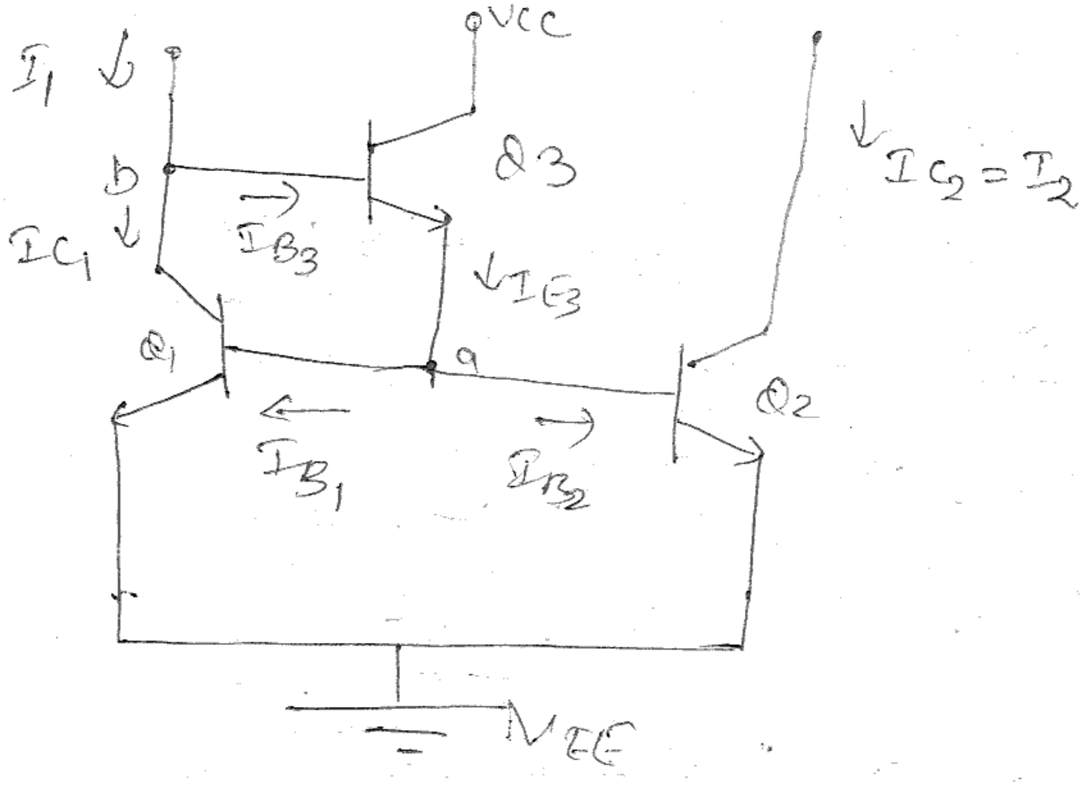
When the current gain β value is Extending 100, then $I_{C_2} = I_{C_1}$, which is approximately equal to I_{ref}

$$I_{C_2} = I_{C_1} \simeq I_{ref}$$

Modifying method I (Wilson current source)

By using the previous circuit we can analyse the value of β is large and thus the value of resistance is decreased. If the value of R is reduced then β will also be reduced. So that the value of $I_{C_1} \neq I_{C_2}$. They in order to maintain the equal value of the collector currents we go on for this modified circuit.

To overcome this problem the circuit may be modified by neglecting the resistor R and including a transistor in the circuit.



Analysis :-

Apply KVL at node 'b',

we get,

$$I_1 = I_{C_1} + I_{B_3} \quad -(1)$$

Since Q_1 & Q_2 are equal,

$$I_{B_1} = I_{B_2} = I_B \quad -(2)$$

The Emitter current $I_{E_3} = 2I_B$ — (3)

w.k.t

$$I_E = I_B + I_C \quad \& \quad I_C = \beta I_B$$

$$\therefore \quad I_{E_3} = (1+\beta) I_{B_3} \quad — (4)$$

from eqn (3)

$$2I_B = (1+\beta) I_{B_3} \quad — (5)$$

Now,

$$I_{C_1} = I_{E_1} = \beta I_B \quad — (6)$$

$$I_{C_2} = I_{E_2} = \beta I_B \quad — (7)$$

Sub (5) & (6) in (1)

$$I_1 = \beta I_B + \frac{2I_B}{(1+\beta)}$$

$$= I_B \left[\frac{\beta(1+\beta) + 2}{(1+\beta)}\right] \quad — (8)$$

Sub (8) in (7)

$$I_{C_2} = \beta \left[\frac{I_1(1+\beta)}{\beta(1+\beta)+2}\right]$$

Since $I_{C_2} = I_2$

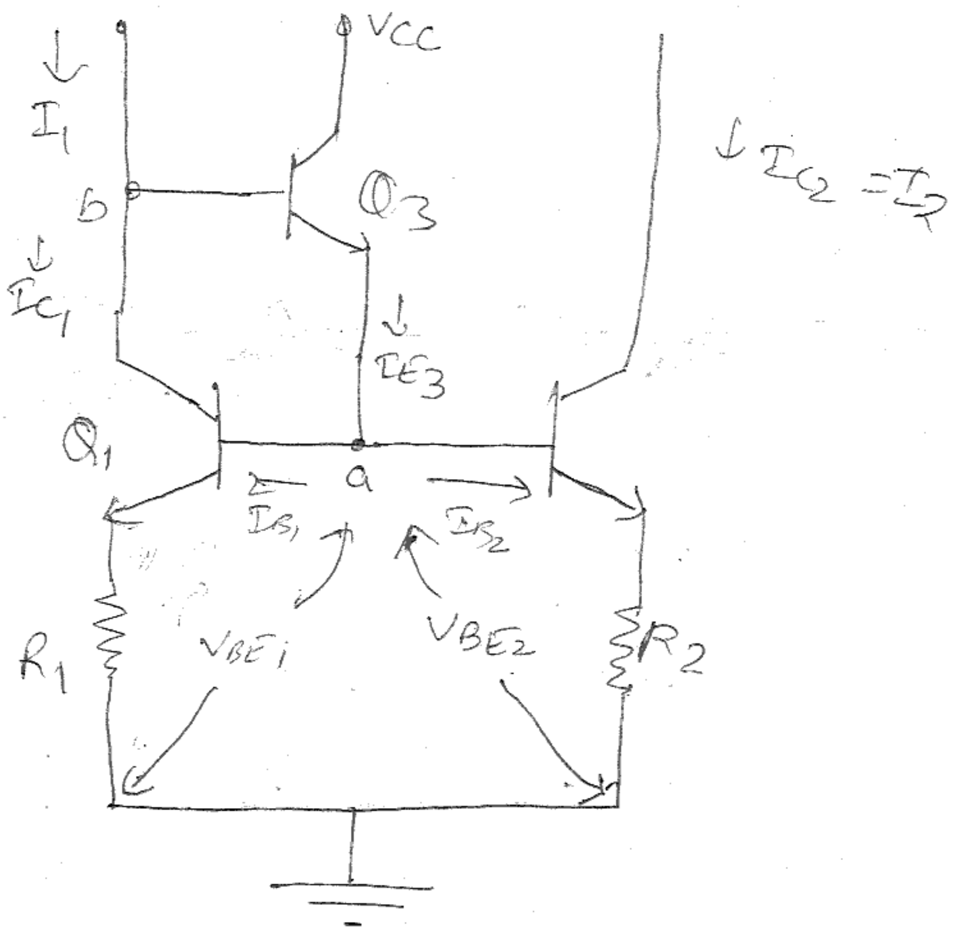
$$I_2 = \beta \left[\frac{I_1(1+\beta)}{\beta(1+\beta)+2}\right]$$

Thus the ratio of I_2 / I_1 is ~~given~~

$$\boxed{\frac{I_2}{I_1} = \frac{\beta(1+\beta)}{\beta(1+\beta)+2}}$$

~~to~~ much less dependent upon β in this modified circuit.

~~Mody~~ Modifying Method - II (widlar current source)



Analysis ;-

By neglecting the base currents & by considering the base values we get the ratio.

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE1} - V_{BE2})/\eta V_T} \quad (\because \eta = 1)$$

$$\ln\left(\frac{I_{C2}}{I_{C1}}\right) = \frac{V_{BE1} - V_{BE2}}{\eta V_T}$$

Since $\eta = 1$

$$V_T \ln\left(\frac{I_{C2}}{I_{C1}}\right) = V_{BE1} - V_{BE2} \quad \text{--- (1)}$$

Applying KVL.

$$V_{BE1} - V_{BE2} + I_1 R_1 - I_2 R_2 = 0 \quad \text{--- (2)}$$

V_B

Slew Rate

It is defined as the ~~rate~~ change of o/p voltage with respect to time.

$$S = \left.\frac{dV_o}{dt}\right|_{max}$$

$$V_s = V_m \cos\omega t$$

$$V_o = V_m \cos\omega t$$

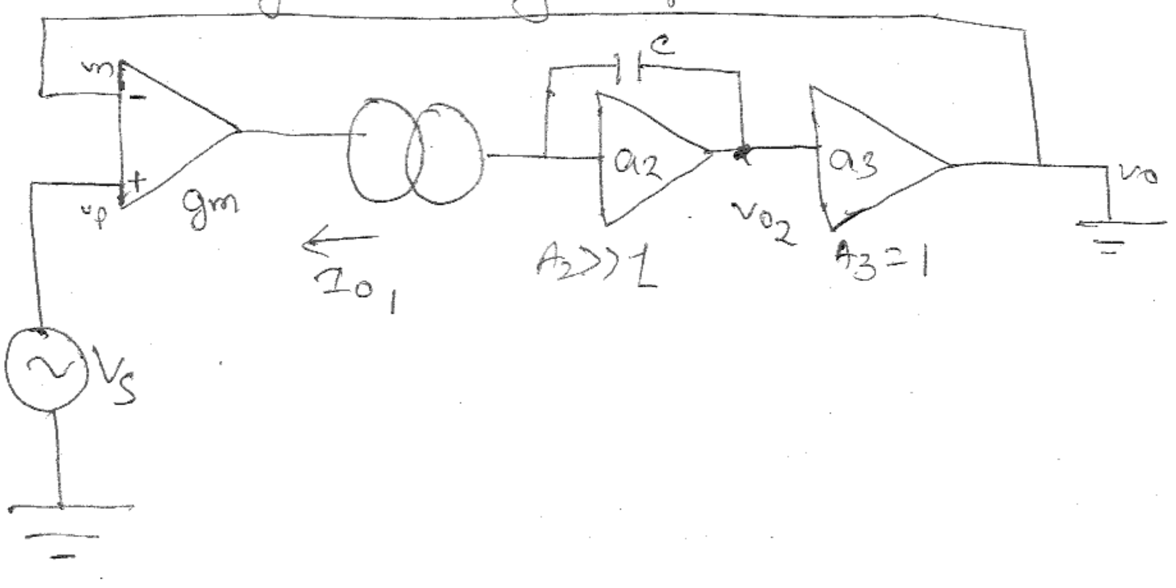
$$\frac{dV_o}{dt} = \omega V_m \sin\omega t$$

$$\left.\frac{dV_o}{dt}\right|_{max} = 2\pi f V_m \qquad \{\sin\omega t = 1\}$$

$$S = 2\pi f V_m$$

$$\boxed{f = \frac{S}{2\pi V_m}}$$

Considering a voltage follower circuit



$$\delta = \frac{I_{max}}{C}$$

$$I_{o1sat} = I_{max}$$

$$\Rightarrow \quad I_{o1} = C\frac{dV_o}{dt}$$

$$I_{o1} = g_m(V_p - V_n)$$

$$V_{o2} = Z_C\, g_m(V_p - V_n)$$

$$V_{o2} = \left(\frac{1}{j\omega C}\right) g_m(V_p - V_n)$$

op-amp gain $|a| = \dfrac{|V_o|}{|V_p - V_n|}$

$$= \left|\frac{V_o}{V_p - V_n}\right|$$

$$= \left(\frac{g_m}{\omega C}\right)$$

$$= \frac{g_m}{2\pi f C}$$

$$f_t = |a| f$$

$$= \frac{g_m}{2\pi \cancel{f} C} \cdot \cancel{f}$$

$$f_t = \frac{g_m}{2\pi C}$$

$$C = \frac{g_m}{2\pi f_t}$$

$$\delta = \frac{I_{o,(sat)}}{C}$$

$$\boxed{\delta = \frac{I_{o,sat}\, 2\pi f_t}{g_m}}$$

- → By increasing current.
- → increasing f_t.
- → Reducing g_m.

Frequency Compensation :-

The method of ~~modify~~ modifying loop gain frequency response of op-amp, so that it behaves like a single break frequency response which provides sufficient positive ~~face~~ phase margin is called frequency compensation technique.

i) Internal
↓
miller's Effect

External comp
- → Dominant pole compensation.
- → Pole-zero comp.

1) Dominant pole Compensation :-

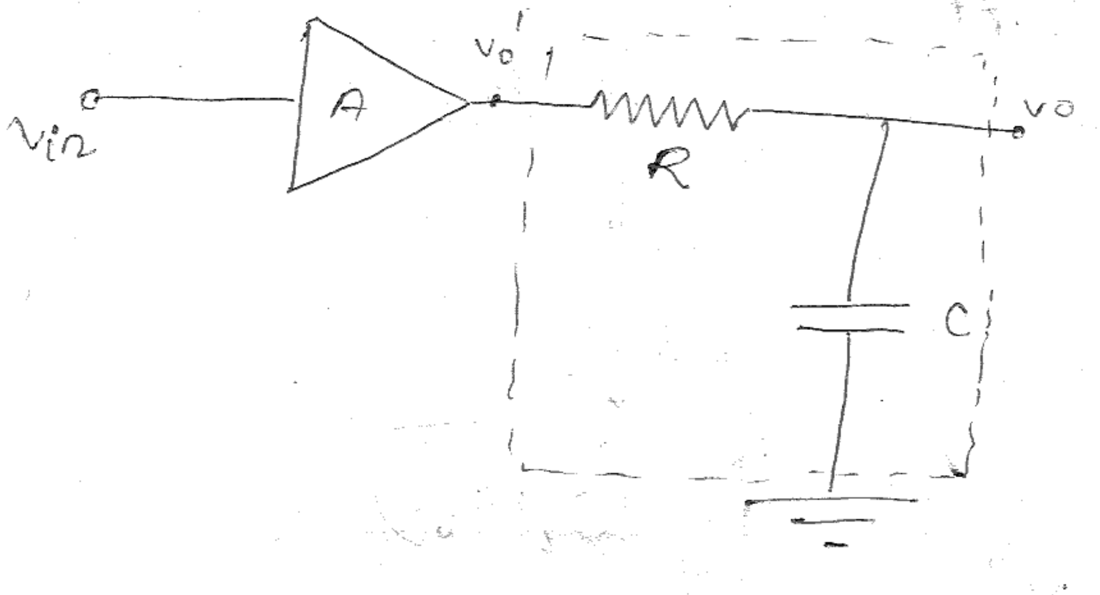
Consider an op-amp with three break frequencies and its loop gain is

$$A = \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$$

f_1, f_2, f_3 are break frequencies

$A_{OL} \rightarrow$ open loop gain

$f \rightarrow$ Carrier frequency.



The dominant pole means the pole with magnitude much smaller than the existing poles and hence the break frequency of the compensating network. In this loop gain the dominant pole is introduced by adding a compensating network which is nothing but a simple RC network is the ~~Sa~~ smallest compare to the Existing break frequency.

The transfer function of the compensating network is,

$$A' = \frac{V_o}{V_o'}$$

Using voltage divider Rule

$$A' = \frac{-jX_C}{R - jX_C}$$

$$= \frac{\frac{-j}{2\pi fC}}{R - (j/2\pi fC)}$$

$$V_o' = \frac{1}{\left(\frac{R}{\frac{-j}{2\pi fC}}\right) + 1}$$

$$A_1 = \frac{1}{1 + j2\pi fRC}$$

hoose

e

ating

let us consider, $f_d = \frac{1}{2\pi RC}$

$$\therefore A_1 = \frac{1}{1 + j\left(\frac{f}{f_d}\right)}$$

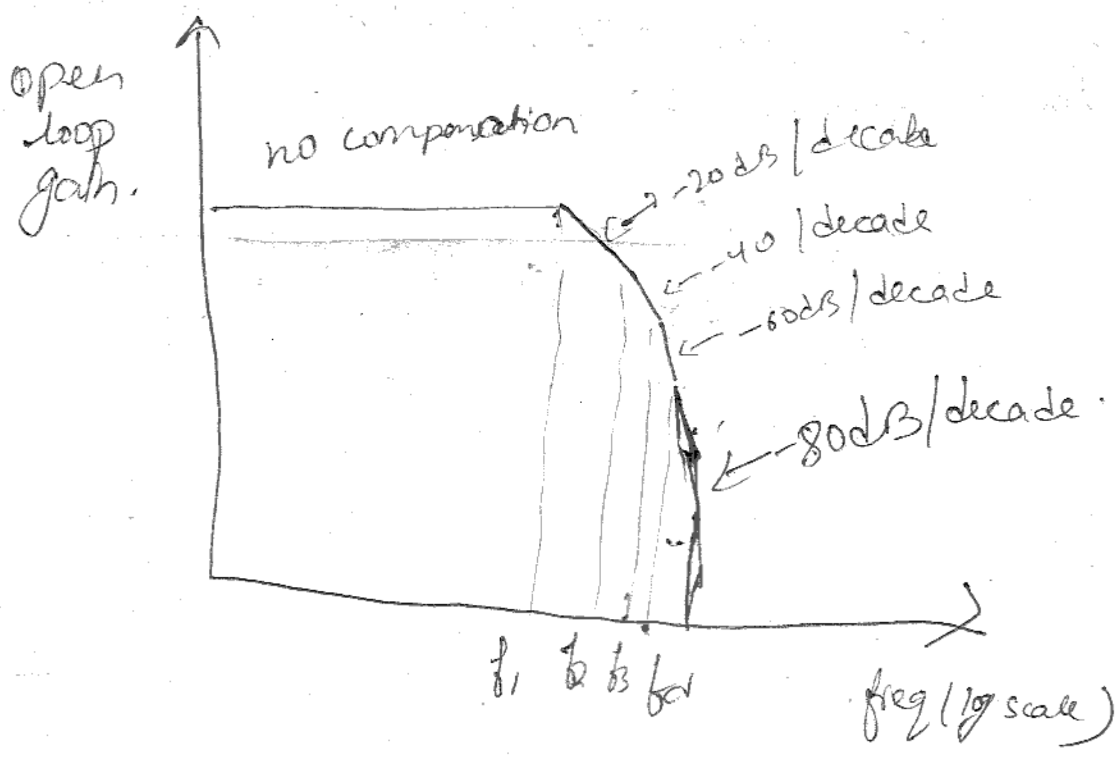
$f_d \rightarrow$ break frequency of compensating n/w

The compensating transfer function is

$$A' = A \cdot A_1$$

$$= \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)} \cdot \frac{1}{1+j\left(\frac{f}{f_d}\right)}$$

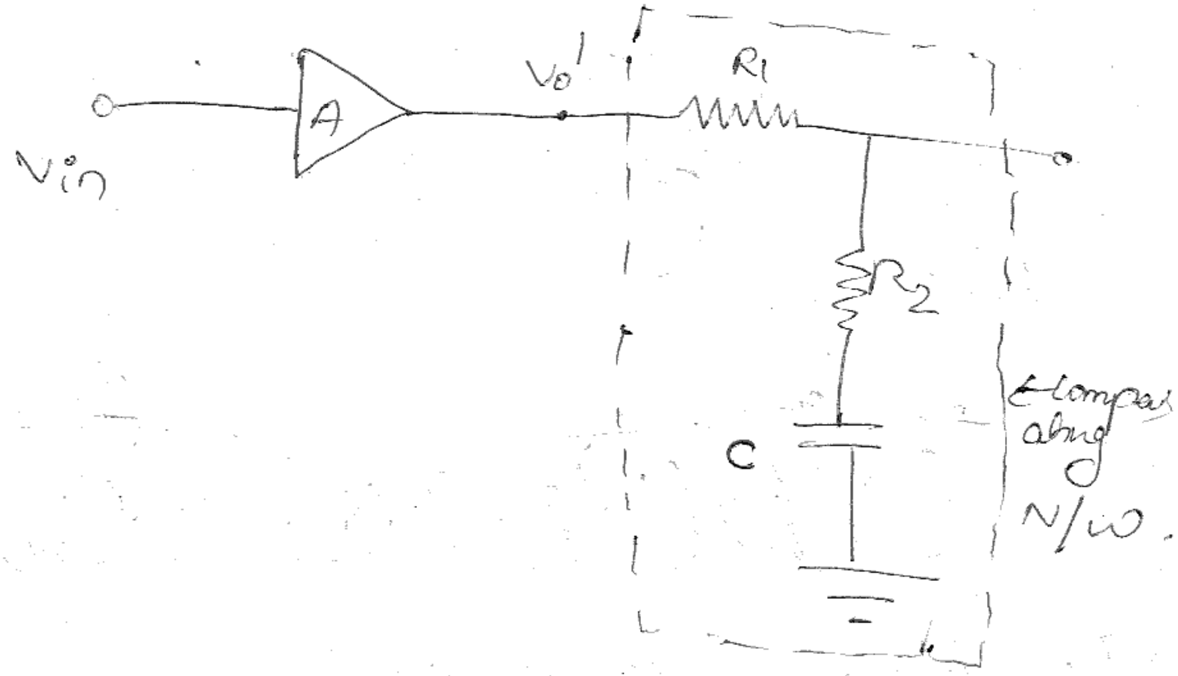
The frequency response curve is given by



disadvantages

1. Bandwidth will get reduced.

Pole - zero Compensation



Consider the same op-amp, described by the open loop gain A with three break frequencies

$$A = \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)}$$

In this method, the transfer function A is modified by adding a pole and zero with the help of compensating network.

The zero added is at higher frequen[cy] while a pole is at lower frequency.

The transfer function of compensating N/W

$$A_1 = \frac{V_0}{V_0'}$$

By voltage divider rule

$$A_1 = \frac{Z_2}{Z_1 + Z_2}$$

Here $Z_1 = R_1$; $Z_2 = R_2 - jX_{C_2}$

$$A_1 = \frac{R_2 - jX_{C_2}}{R_1 + R_2 - jX_{C_2}} = \frac{R_2 - \frac{j}{2\pi f C_2}}{R_1 + R_2 - \frac{j}{2\pi f C_2}}$$

$$= \frac{\left[\frac{R_2}{-j/2\pi f C_2}\right] + 1}{\frac{R_1 + R_2}{\left[-j/2\pi f C_2\right]} + 1}$$

Now,

WKT $-\frac{1}{j} = +j$

$$A_1 = \frac{1 + j2\pi f R_2 C_2}{1 + j2\pi f (R_1 + R_2) \cdot C_2}$$

Let $f_1 = \frac{1}{2\pi R_2 C_2}$ & $f_0 = \frac{1}{2\pi (R_1+R_2) C_2}$

$$A_1 = \frac{1 + j\left(\frac{f}{f_1}\right)}{1 + j\left(\frac{f}{f_0}\right)}$$

The value of R_1, R_2 and C_2 are so selected that, the break frequency for the zero, matches with the first corner frequency f_1 of the uncompensated system while the pole of the compensation Network at f_0 is selected in such a way to compensate transfer function A' passes through zero decibel at the second corner frequency f_2 of the uncompensated system.

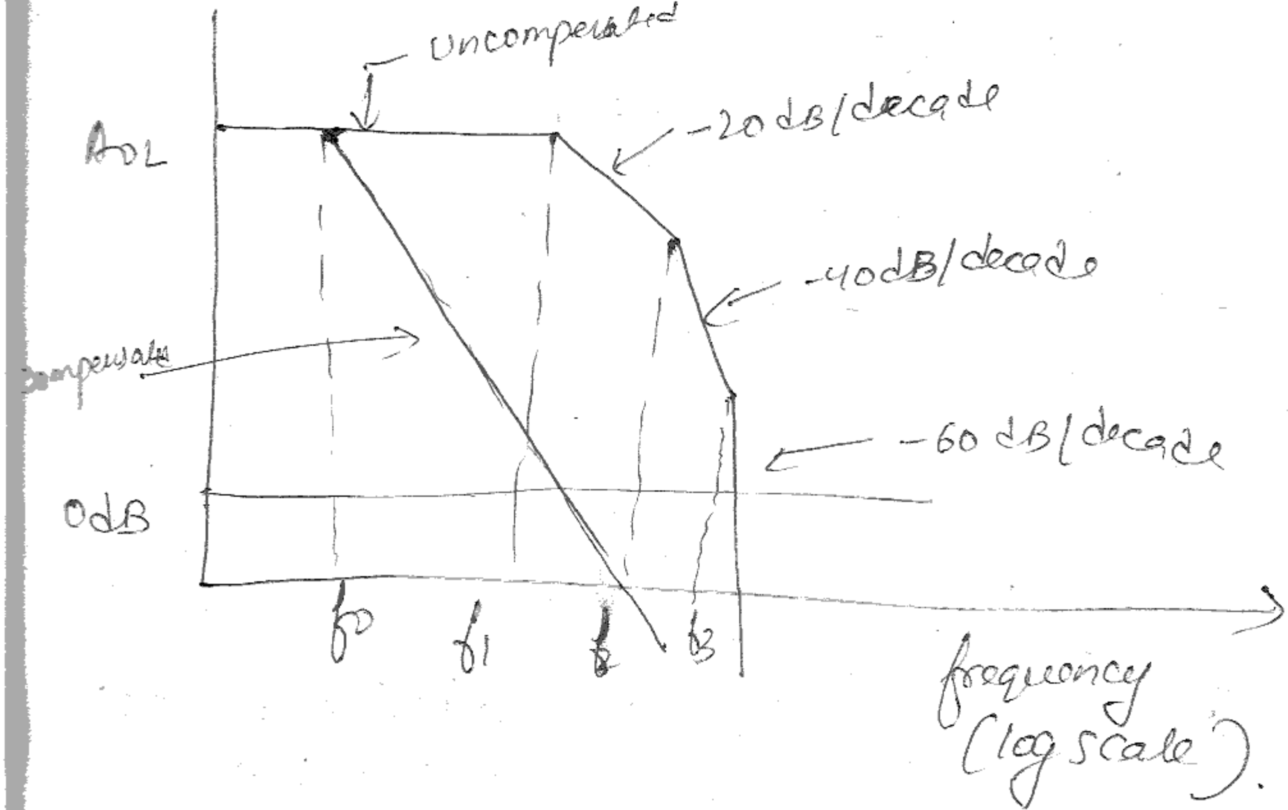
The resultant loop gain becomes

$$A' = A A_1$$

$$A_1 = \frac{A_{OL}\left(1 + j\frac{f}{f_1}\right)}{\left(1 + j\frac{f}{f_0}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

where $0 < f_0 < f_1 < f_2 < f_3$.

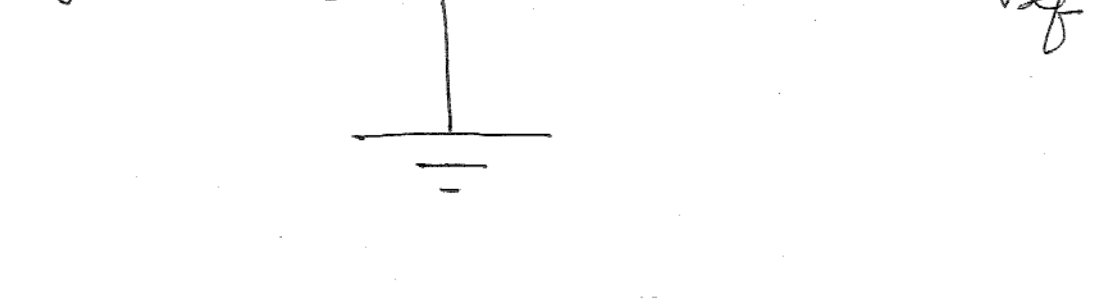
Frequency Response



UNIT - III

Analog multiplier and PLL

Analog multipliers :-



$V_{ref} = 10\ V$

$V_{out} = \frac{V_x V_y}{10}$

$V_x < V_{ref}$

$V_y < V_{ref}$

cases

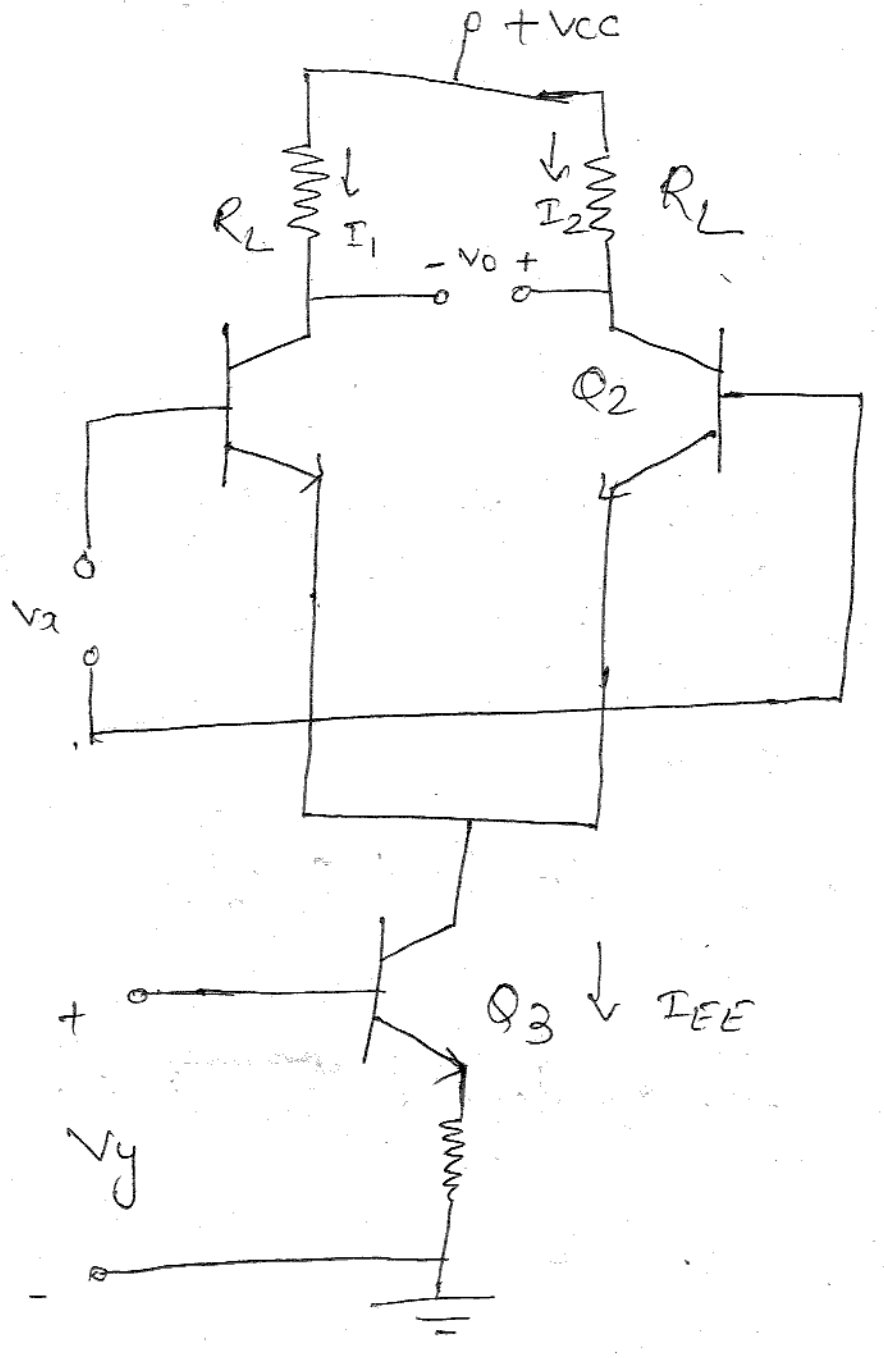
	V_x	V_y	
(i)	+	+	⇒ single quadrant multiplier
ii)	+	+/−	⇒ 2-quadrant multiplier
iii)	~~++/~~ + −	− +	⇒ 4 quadrant multiplier

Applications

1) used in freq. doubling.
2) frequency shifting.
3) Phase-angle detection.

Variable Transconductance Technique :-

The variable Transconductance Technique make use of the dependence characteristics of the transistors transconductance parameter on the Emitter current bias applied.



Analysis :-

The relationship b/w Vx and Vo is given by,

$$V_o = g_m R_L V_x \quad -(1)$$

where,

$$g_m = \frac{I_{EE}}{V_T} \quad (2)$$ is the transconductance stage.

Analysis :-

The collector current I_1 & I_2 are related to V_x by the relation,

$$\frac{I_1}{I_2} = e^{(V_x/V_y)} \quad — (3)$$

The transistors Q_1 & Q_2 are biased through the diode connected Q_A and Q_B which are driven by controlled current source I_A and I_B

Net bias voltage,

$$V_x = V_T \ln\left(I_B/I_A \right)$$

The eqn (2) depends on Emitter current I_{EE} which is turn is controlled by applying $\overline{II}$ voltage V_y to transistor Q_3.

$$V_y = I_E R_E$$

$$\Rightarrow V_O = \frac{I_{EE}}{V_T} \cdot R_L V_x$$

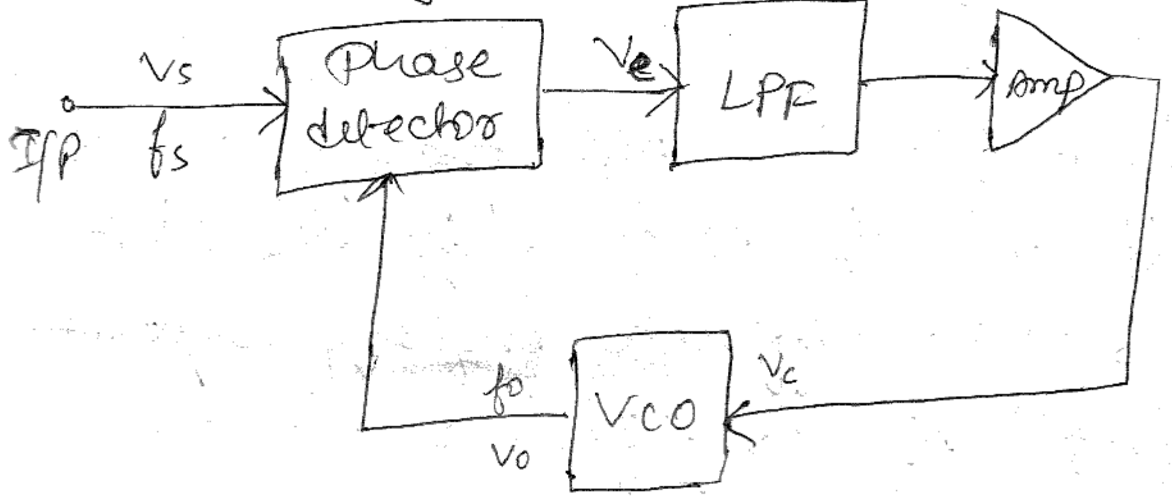
$$= \frac{V_y}{R_E V_T} \cdot R_L V_x$$

$$V_o = \left(\frac{R_L}{R_E V_T}\right) V_x \cdot V_y$$

$$\boxed{V_o = K \cdot V_x V_y}$$

PLL :-
Phase locked loop

Block diagram ;-



VCO :- It is free running multivibrator & operates at a set frequency fo called free running frequency. It can also be shifted to either side by applying a dc controlled voltage Vc.

The frequency deviation is directly proportional to the dc controlled voltage and hence it is called Voltage Controlled Oscillator.

Phase detector :- If an input signal V_s of the frequency f_s is applied to the PLL, the Phase detector compares the phase and the frequency of the incoming signal to that of the output V_o of the VCO. If the two signals differs in frequency or phase an error voltage V_e is generated.

Phase detector is basically a multiplier and produces the sum $(f_s + f_o)$ and difference $(f_s - f_o)$ at its output.

LPF :- The high frequency component $(f_s + f_o)$ is removed by the LPF and the difference frequency component $(f_s - f_o)$ is amplified and then ~~can~~ applied as a controlled voltage V_c to the VCO.

Application :-

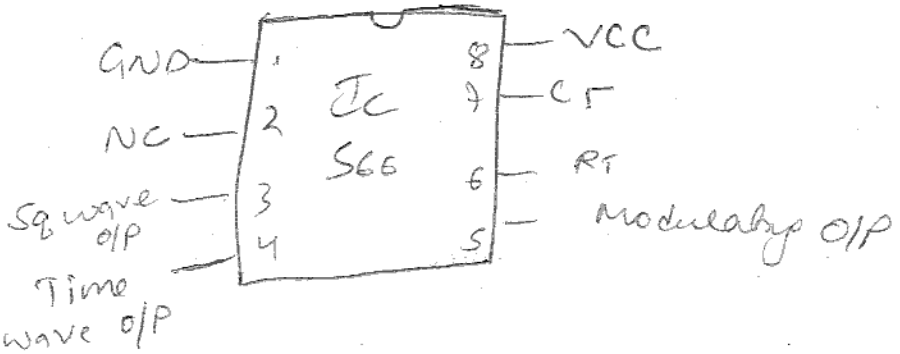
1) This technique of a Electronic frequency control is used in Satellite Communication Systems

2) Air some navigational system

3) FM communication Systems

4) PC

Voltage controlled Oscillator (VCO) :-



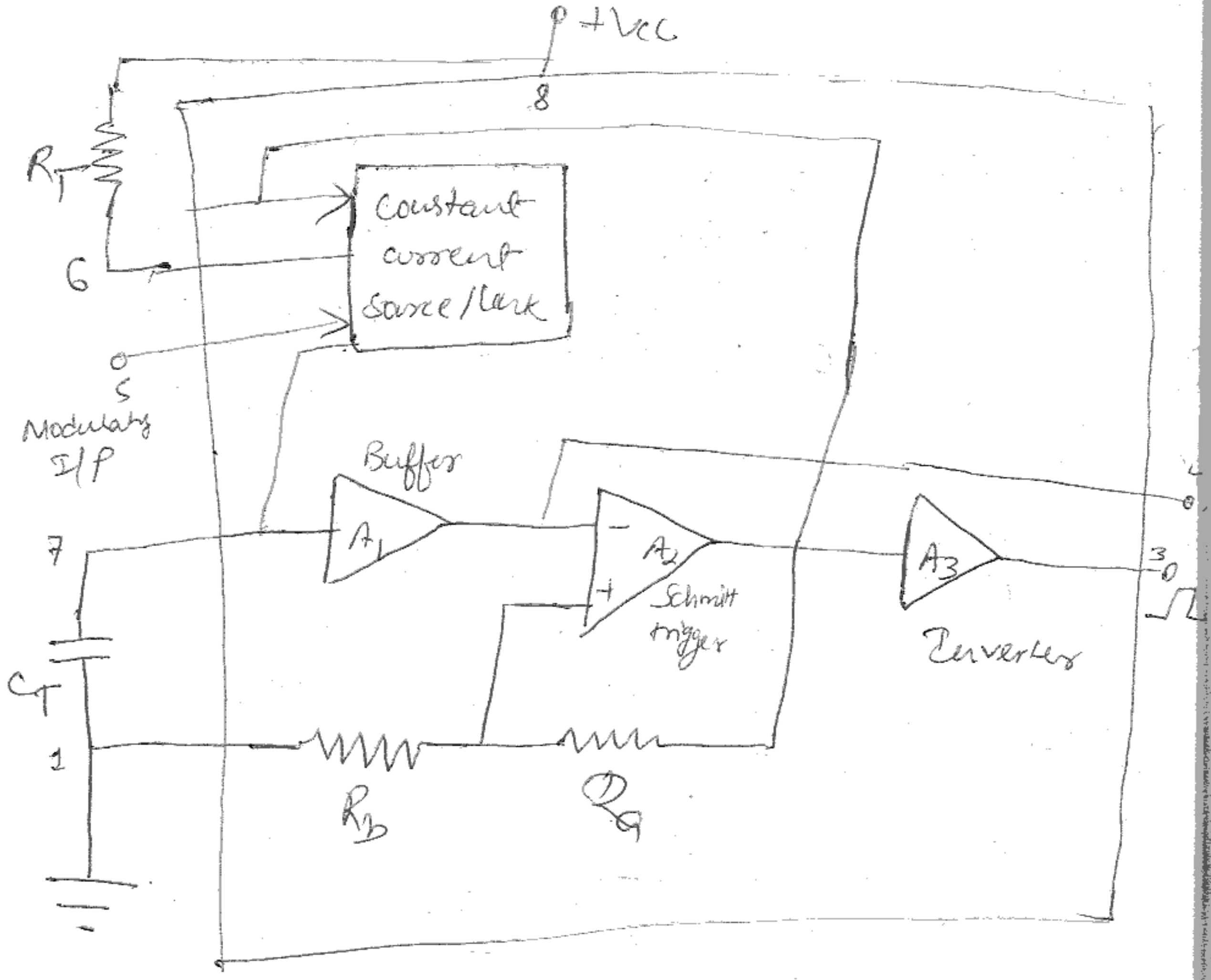
The total voltage across the capacitor changes from 0.25 Vcc to 0.5 Vcc

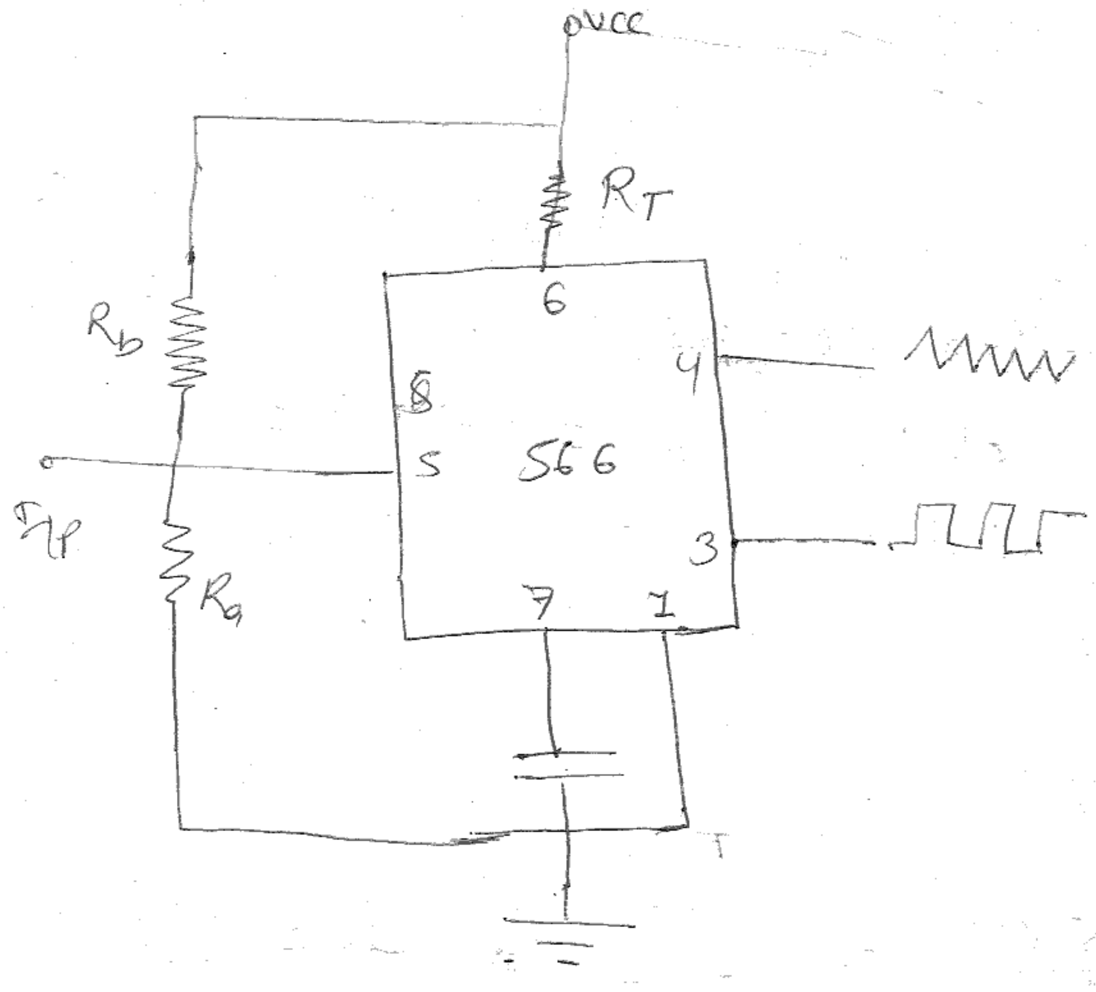
$\Delta V = 0.25 V_{cc}$

Thus the capacitor charges with constant current source, so

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T}$$

$$\frac{0.25 V_{cc}}{\Delta t} = \frac{i}{C_T} \Rightarrow \Delta t = \frac{0.25 V_{cc} \times C_T}{i}$$


+Vcc
8
R_T
6
Constant current source/sink
5
Modulating I/P
Buffer
A_1
7
C_T
1
A_2
Schmitt trigger
A_3
Inverter
3
R_b
R_a


Vcc
R_T
6
4
R_b
8
5
566
I/P
3
R_a
7
1

The total time period 'T' of the triangular waveform is $2\Delta t$.

$$\therefore \quad f_o = \frac{1}{T} = \frac{1}{2\Delta t}$$

$$= \frac{i}{0.5\, V_{CC}\, C_T}$$

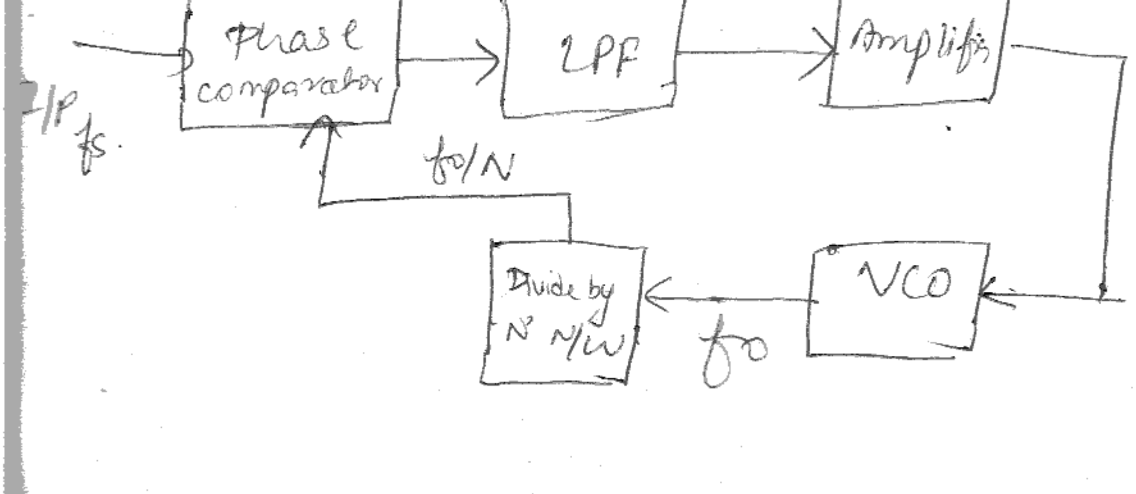
But the current source while is applied

$$i = \frac{V_{CC} - V_C}{R_T}$$

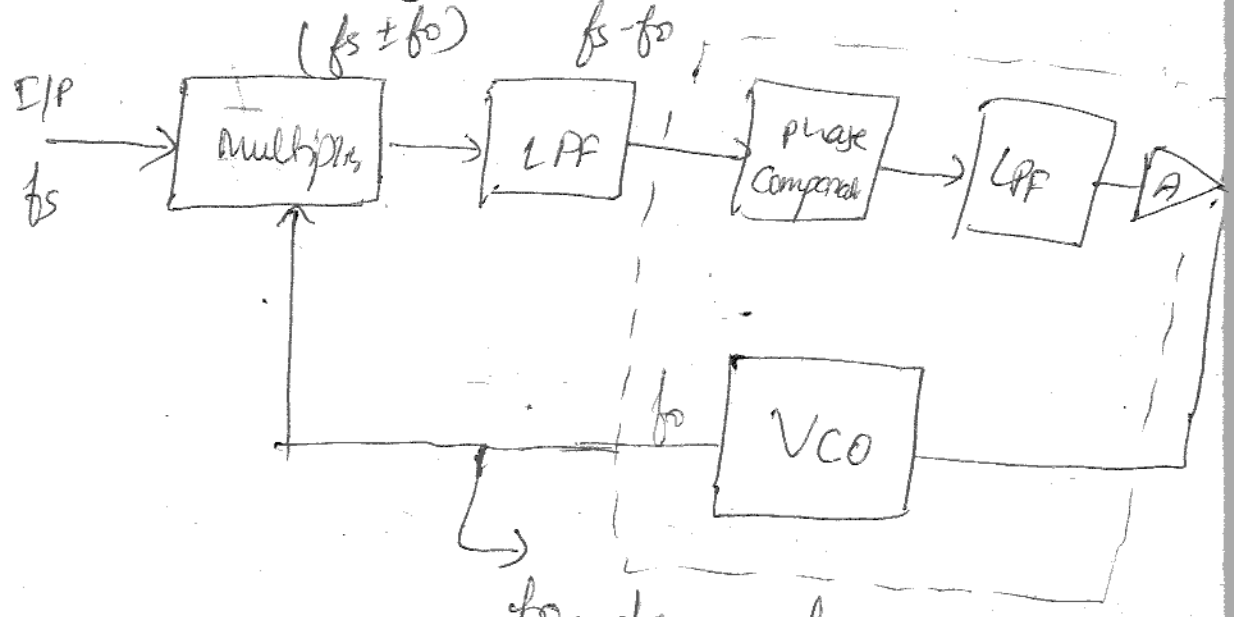
$$f_o = \frac{2(V_{CC} - V_C)}{V_{CC}\, R_T\, C_T}$$

Applications of PLL :-

1. Frequency Multiplication/ Division



2. Frequency Translation



$$f_o - f_s = f_1$$

$$f_o = f_1 + f_s$$