or,
$$y = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} \tag{7.101}$$

Hence the output

$$V_{HP} = y - v_i = \begin{bmatrix} 1 & 1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} - (1)\, v_i \tag{7.102}$$

The simulation of Eqs. (7.99) and (7.102) is shown in Fig. 7.18 having V_{HP} as output.

Similarly, the low-pass transfer function of Eq. (7.75) can be written in the same fashion as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} 0 & 1 \\ -1 & -1 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} v_i \tag{7.103}$$

and output

$$V_{LP} = \begin{bmatrix} -1 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix}$$

The simulation is as shown in Fig. 7.18.

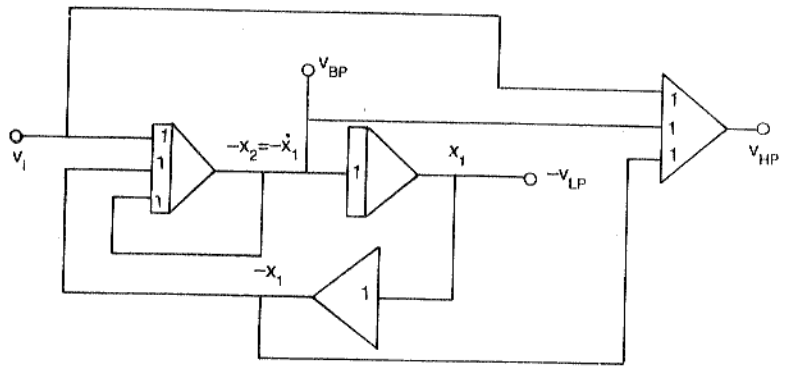

Fig. 7.18 Simulation of state variable filter

7.5 SWITCHED CAPACITOR FILTERS

Active *RC* filters using ICs have advantages of not using inductors and of offering easy implementation of various high performance low-pass, high-pass, band-pass and band-elimination filters. The resistor values needed for these filters are generally much too large for fabrication on a monolithic IC chip. Integrated (diffused) resistors have poor temperature and linearity characteristics. Large value resistors (≥ 10 kΩ) take up an excessive amount of chip area. This is the major reason that active filters have not previously been fully integrated in MOS technology. The switched capacitor filter offers an attractive alternative to the conventional *RC* active filter. A switched

capacitor filter shown in Fig. 7.19 is a three terminal element which consists of capacitors, periodic switches and operational amplifiers and whose open circuit voltage transfer function represents filtering characteristics. It is not possible to manufacture passive elements of an *RC* active filter with suitable values and quality in the same technology as the op-amps. For the range of frequencies within which the op-amp operates satisfactorily, it is not possible in MOS technology to implement *RC* products of sufficient magnitude and accuracy. On the other hand, in the case of switched capacitor filter, the *RC* products are set by capacitor ratios and the switch period. In MOS technology, the accuracy and the values of these quantities are suitable for the implementation of selective filters. The large resistor values required for active filter are easily simulated by the combination of small value capacitors (say 10 pF) and MOS switching transistors. The equivalent resistor value so obtained is high enough such that the filter capacitance value should be small enough to be easily incorporated on a monolithic IC chip. In this way, the complete active filter circuit can be obtained on a monolithic IC chip.

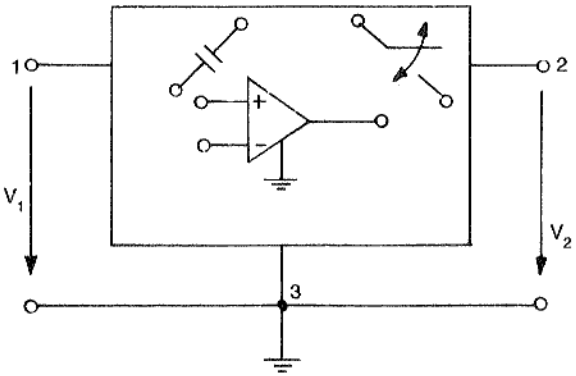

Fig. 7.19 Switched capacitor filter schematic

Thus, even a filter of relatively high order becomes an integrated circuit of a very small size, with a low power consumption and reliability and price which are potentially more favourable than those of passive *LC* and *RC* active filters. Further, the filters may be combined on the same substrate with other logic circuits, offering interesting prospects for the implementation of a complete system of analog and discrete signal processing.

7.5.1 Realization of Resistors by Single Capacitor

Consider the switched capacitor network in Fig. 7.20(a). The switch S is initially in position 'a', the capacitor C is charged to voltage V_1. The switch is then thrown to position 'b'. The capacitor C is discharged to the voltage V_2. Assume $V_2 < V_1$. The amount of charge that flows through the capacitor C is thus,

$$Q = C(V_1 - V_2) \tag{7.105}$$

If the switch 'S' is thrown back and forth every T_{ck} second, then the current i that flows through the capacitor C is equal to the rate at which the charge is transferred through the circuit via C and is given by,

$$i = \frac{Q}{T_{ck}} = \frac{C(V_1 - V_2)}{T_{ck}} = f_{ck} C(V_1 - V_2) \tag{7.106}$$

where T_{ck} is the clock period, $f_{ck} = 1/T_{ck}$ is the clock frequency. The clock frequency is assumed to be large compared to the signal frequency. Thus the size of an equivalent resistor R which would perform the same function as this circuit is given by,

$$R = \frac{T_{ck}}{C} = \frac{1}{f_{ck} C} \tag{7.107}$$

The MOSFET realization of Fig. 7.20(a) is shown in Fig. 7.20(b). When the gate voltage is high, an enhancement-type n-MOS is ***on*** and its resistance is of the order of 1 kΩ. When its gate voltage is low, the transistor is ***off*** and its resistance is about $10^{12}\Omega$. So an n-MOS can be used as an ***on/off*** switch. If the circuit of Fig. 7.20(b) driven by out-of-phase clock signals as shown in Fig. 7.20(c), the transistors

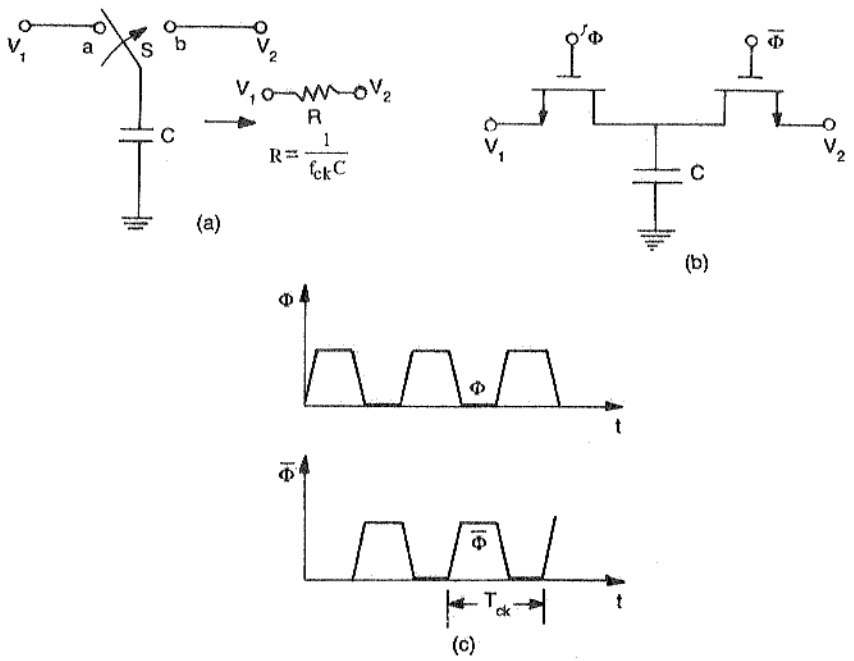

Fig. 7.20 (a) Switched capacitor network (b) n-MOS SPDT switch (c) Two phase nonoverlapping clock

will conduct on alternate half cycles, thus providing a single pole double throw switch (SPDT). This is known as switched capacitor I (SC – I).

The second form of switched capacitor circuit is shown in Fig. 7.21 (a). During the ***on*** period of switch S_1, the capacitor C is initialized, while during the ***on*** period of switch S_2, the net charge $C(V_1 - V_2)$ is transferred. As this delivery of charge occurs at every sampling interval T_{ck}, the average current i flowing through the capacitor is given by,

$$i = \frac{C(V_1 - V_2)}{T_{ck}} \tag{7.108}$$

Therefore, the equivalent resistance R that the circuit of Fig. 7.21 (a) can simulate is given by,

$$R = \frac{T_{ck}}{C} \tag{7.109}$$

The MOSFET implementation is shown in Fig. 7.21(b). This is known as switched capacitor II (SC – II).

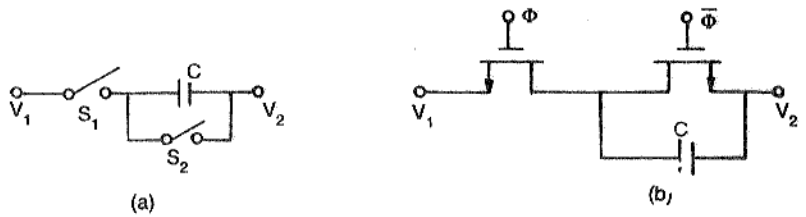

Fig. 7.21 (a) Switched capacitor network (b) MOSFET realization

The third form of switched capacitor network is shown in Fig. 7.22 (a). When the switch is in position aa′, the charge on the capacitor C is $C(V_1 - V_2)$. When the switch is placed in the alternate position bb′, the charge on the capacitor C is $-C(V_1 - V_2)$. The negative sign is due to the change of direction of current. The switch is thrown back and forth every T_{ck} seconds. Therefore, the total charge transmitted during the period T_{ck} is,

$$C(V_1 - V_2) - [-C(V_1 - V_2)] = 2C(V_1 - V_2) \tag{7.110}$$

The corresponding current flowing during time T_{ck} is given by,

$$i = \frac{2C(V_1 - V_2)}{T_{ck}} = \frac{V_1 - V_2}{R} \tag{7.111}$$

where the size of the equivalent resistor R which would perform the same function is given by,

$$R = \frac{T_{ck}}{2C} \tag{7.112}$$

The MOSFET realization of the circuit is shown in Fig. 7.22(b). This is referred to as switched capacitors III (SC – III). The advantage of this form of realization is that it doubles the effective sampling rate.

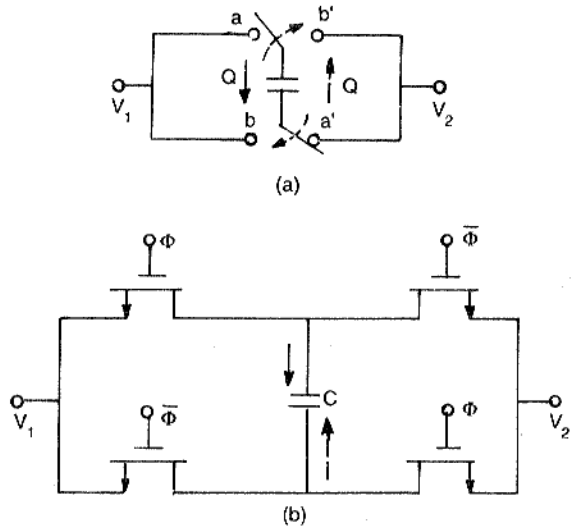

Fig. 7.22 (a) Switched capacitor network (b) MOSFET realization

Various other forms of switched capacitor circuits are shown in Fig. 7.23. The two phase clock will provide the complementary but non-overlapping clock pulses ϕ and $\bar{\phi}$. The clock frequency is assumed to be large compared to the signal frequency.

Consider the series switched capacitor circuit shown in Fig. 7.23(a). When ϕ is high, $\bar{\phi}$ is low, capacitor C will charge up to a voltage $(V_2 - V_1)$. The charge is suppled to the capacitor and is given by,

$$Q = C(V_1 - V_2) \tag{7.113}$$

When ϕ is low and $\bar{\phi}$ is high, C discharges back to zero. The current i flowing through capacitor C will be equal to the rate of charge transferred through the circuit via C and is given by,

$$i = \frac{Q}{T_{ck}} = \frac{C(V_1 - V_2)}{T_{ck}} = f_{ck}\, C\,(V_1 - V_2) = \frac{V_1 - V_2}{R} \tag{7.114}$$

where T_{ck} is the clock period, $f_{ck} = \dfrac{1}{T_{ck}}$ is the clock frequency and R is the equivalent resistance given by,

$$R = \frac{T_{ck}}{C} = \frac{1}{f_{ck}C} \tag{7.115}$$

In the circuit of Fig. 7.23(b) when ϕ is high, the series capacitor C is charged upto V_1 and the corresponding charge transfer that occurs

is $Q = CV_1$. When ϕ goes low and $\bar{\phi}$ goes high, the capacitor C charges up in the opposite direction to V_2. The charge transfer from the output of the circuit back into C is $Q = C_1\,(V_2 - V_1)$. The time average of this charge is the current flow i and is given by,

$$i = -\frac{Q}{T_{ck}} = -f_{ck}\,C(V_2 - V_1) = \frac{V_1 - V_2}{R} \tag{7.116}$$

where,

$$R = \frac{1}{f_{ck}C} \tag{7.117}$$

The two circuits just described use a series switched capacitor.

The circuit of Fig. 7.23(c) uses a shunt switched capacitor. The circuit is a modification of Fig. 7.21(b) with $V_2 = 0$. For this circuit,

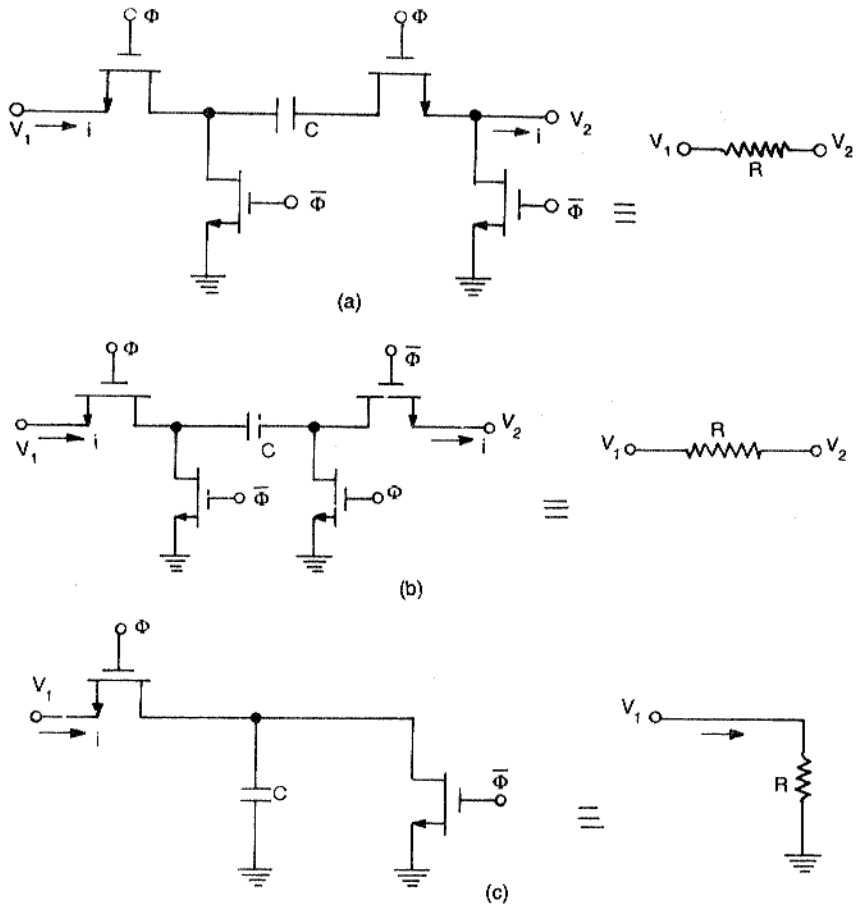

Fig. 7.23 (a) Noninverting series switched capacitor circuit (b) Inverting series switched capacitor circuit (c) Shunt capacitor circuit

capacitor C charges upto $Q = CV_1$ when ϕ is high, $\bar{\phi}$ is low. When ϕ goes low and $\bar{\phi}$ goes high, the capacitor C discharges to zero through the $\bar{\phi}$ transmitter. The current i is therefore given by,

$$i = \frac{Q}{T_{ck}} = \frac{CV_1}{T_{ck}} = f_{ck}\, CV_1 = \frac{V_1}{R} \tag{7.118}$$

where $$R = \frac{1}{f_{ck} C} \tag{7.119}$$

Various types of low pass, high-pass, band-pass and band-elimination active filter circuits can be implemented using switched capacitors to replace the resistors so that an all-capacitor filter circuit can be obtained. Since the capacitor, switch and op-amp all can be realized in MOS technology, a complete filter on a single IC chip can be easily achieved.

7.5.2 Switched Capacitor Integrator

The use of switched capacitor is shown in the simple example of an ordinary integrator of Fig. 7.24(a). The transfer function is

$$H = \frac{-1/sC_F}{R_1} = -\frac{1}{sR_1 C_F}$$

$$= -\frac{1}{j(f/f_o)} \tag{7.120}$$

where $f_o = 1/2\,\pi\, R_1 C_F$ and is the frequency at which the gain is unity. The resistor R_1 can be replaced by a switched capacitor C_1 as shown in Fig. 7.24 (b). The MOS version is shown in Fig. 7.24 (c).

Here $$R_1 = \frac{1}{C_1 f_{ck}} \tag{7.121}$$

where f_{ck} is the clock frequency. The unity-gain frequency f_o is therefore given by

$$f_o = \frac{C_1}{2\pi C_F} f_{ck} \tag{7.122}$$

By proper choice of f_{ck} and C_1/C_F ratio, it is possible to avoid the use of high capacitance values even if low values of f_o are desired.

Example 7.9

Design a switched capacitor integrator for f_o = 10 Hz. Compare the values with an RC integrator.

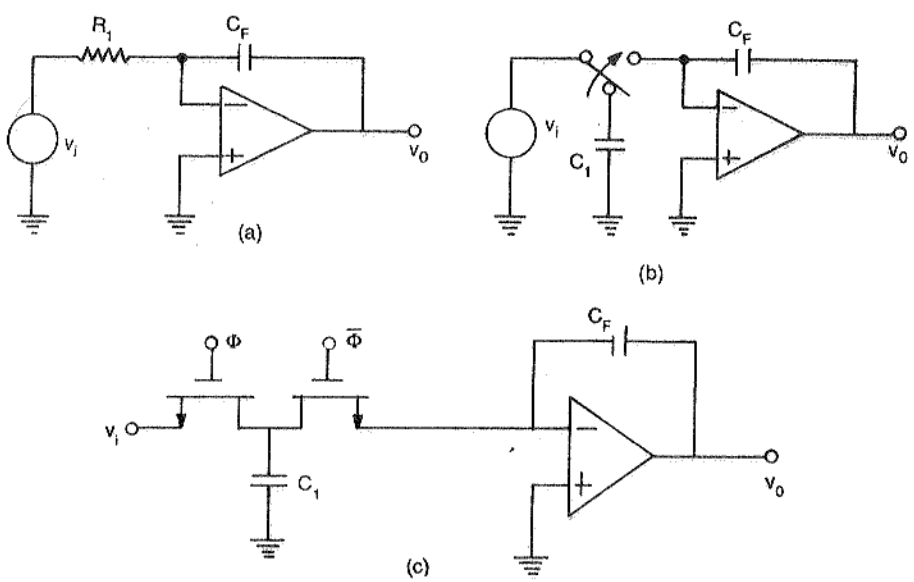

Fig. 7.24 (a) *RC* integrator (b) Switched capacitor version of (a). (c) CMOS version of (a)

Solution

For switched capacitor integrator, assume f_{ck} = 1 kHz. From Eq. (7.122), $C_F/C_1 = f_{ck}/2\,\pi\, f_o = 10^3/2\pi \times 10 = 15.9$

So, choose C_F = 15.9 pF and C_1 = 1 pF

For RC integrator, select R_1 = 1.6 MΩ.

Then $C_F = 1/2\,\pi \times 1.6 \times 1.6 \times 10 = 10$ nF

The values of R_1 = 1.6 MΩ and C_F = 10 nF are not quite practical for a monolithic circuit. From this, it is obvious that switched capacitor circuits are more practical so far as IC fabrication is concerned. So it can be seen that an SC integrator requires very low values of capacitances compared to lossy integrator.

If a resistor R_2 is placed in parallel with the feedback capacitor C_F of Fig. 7.25(a), a lossy or practical integrator is obtained. The transfer function for this circuit can be written as,

$$H(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)} = -\frac{R_2/R_1}{1 + j\omega R_2 C_F}$$

$$= -\frac{R_2/R_1}{1 + j(f/f_h)} \tag{7.123}$$

where, the corner frequency $$f_h = \frac{1}{2\pi C_F R_2} \tag{7.124}$$

The switched capacitor implementation of Fig. 7.25(a) is shown in Fig. 7.25(b) where resistors R_1 and R_2 have been replaced by switched

capacitors C_1 and C_2 and its MOS version is in Fig. 7.25(c).

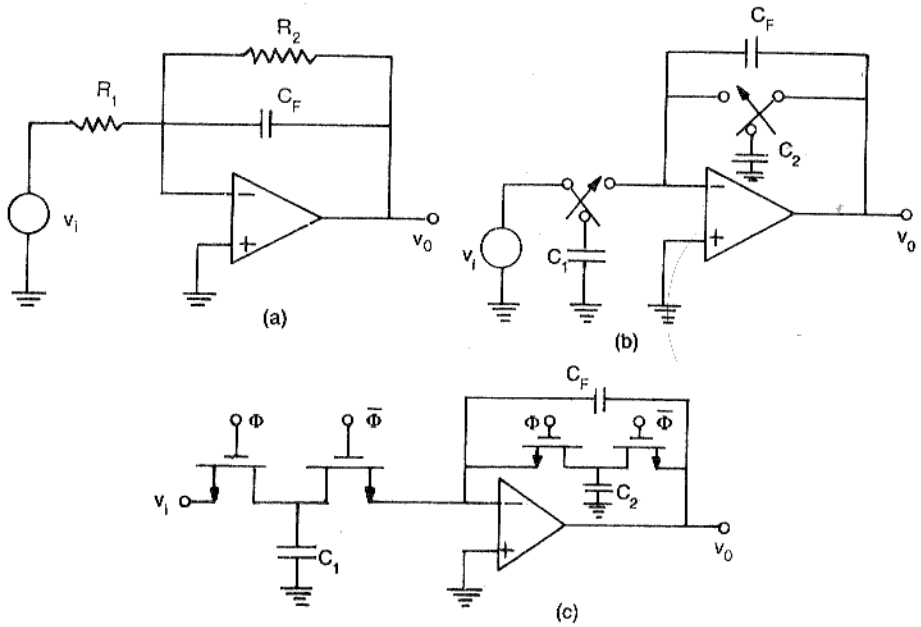

Fig. 7.25 (a) Lossy integrator (b) Switched capacitor version (c) CMOS version

$$R_2 = \frac{1}{f_{ck} C_2} \tag{7.125}$$

$$R_1 = \frac{1}{f_{ck} C_1} \tag{7.126}$$

So, $$\frac{R_2}{R_1} = \frac{C_1}{C_2} \tag{7.127}$$

and $$f_h = \frac{1}{2\pi C_F R_2} = \frac{1}{2\pi} \frac{C_2}{C_F} f_{ck} \tag{7.128}$$

Thus the transfer function can be rewritten as,

$$H(j\omega) = -\frac{C_1}{C_2}\left[\frac{1}{1 + j(f/f_h)}\right] \tag{7.129}$$

It is evident from the transfer function expression that the LP filter characteristics is a function of MOS capacitance ratio and the clock frequency.

Thus with the control of the clock frequency, the filter characteristic can be varied electronically. This also shows that SC filters are inherently a programmable type. In a similar fashion, other types of active filters without resistance can also be achieved.

Switched capacitor filters are available in IC version from several manufacturers. The MF6-100 (National Semiconductor) is a 6th order low-pass Butterworth filter fabricated by CMOS technology. A monolithic switched capacitor universal filter (National Semiconductor MF 10) can be designed to provide LP, HP, BP and notch characteristics.

Summary

1. An electric filter is a frequency selective circuit that allows a specified band of frequencies and attenuates the frequencies outside this band.
2. Filters are classified in a number of ways: analog or digital, passive or active, audio or radio frequency.
3. Passive filters use inductors. At audio frequencies, inductors are bulky, expensive and have poor electrical characteristics. Active filters use op-amps.
4. The commonly used filters are: Low pass (LP), High pass (HP), Band pass (BP) and Band reject (BR).
5. Filter behaviour is usually described by frequency response plot. The gain magnitude is usually expressed in dB. Critical frequency occurs when the gain drops by 3 dB below the pass band gain. The critical frequency is the dividing line between the stop band and the pass band.
6. Low pass filters pass low frequencies and stop high frequencies. High pass filters do just the opposite. Critical frequency occurs where the gain has dropped by 3 dB below the pass band. A band pass filter has a pass band between the two cut-off frequencies f_h and f_l and all signals outside this pass band are stopped. The band reject filter, also called a notch filter, performs exactly opposite to the band pass.
7. A first order low pass filter has a –20 dB decade roll-off rate. The roll-off rate increases with the order of the filter. An n-th order filter has a roll-off rate of –20 n dB/decade.
8. Higher order filters are made by cascading first and second order filters.
9. A low pass filter can be converted into a high pass filter or vice versa, simply by interchanging resistors and capacitors.
10. The important transfer functions derived are:

    First order low pass: $\dfrac{A_0\,\omega_h}{s + \omega_h}$

    General Second order filter:

$$\frac{A_0 Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_0)}$$

Second order low pass: $\dfrac{A_0 \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2}$

Second order high pass: $\dfrac{A_0 s^2}{s^2 + \alpha \omega_\ell s + \omega_\ell^2}$

Second order band pass: $\dfrac{-A_0 (\alpha \omega_0) s}{s^2 + (\alpha \omega_0) s + \omega_0^2}$

Second order notch: $\dfrac{A_0 (s^2 + \omega_0^2)}{s^2 + \alpha \omega_0 s + \omega_0^2}$

$|A_0|$ = pass band gain
ω_ℓ, ω_h = lower and upper cut-off frequency (radians/sec)
ω_0 = centre frequency
α = damping doefficient

11. Damping is determined by the amplifier's gain. Bessel filter is a heavily damped filter ($\alpha > 1.7$). It is very stable, but rolls-off very early in the pass band. Butterworth filters ($\alpha = 1.414$) gives maximally flat pass band. A Chebyshev filter ($\alpha < 1.4$) provides faster initial roll-off but gives poorest transient response.
12. A state variable filter uses three or four op-amps and provides low pass, high pass, band pass and notch filter characteristics simultaneously.
13. Resistors occupy large chip areas and can be replaced by a switched capacitor. In switched filter, RC products are set by capacitor ratios and the switch period. These filters are ideal for MOS technology.

Review Questions

7.1. Define an electric filter.
7.2. Classify filters.
7.3. Discuss the disadvantages of passive filters.
7.4. Why are active filters preferred?
7.5. List the commonly used filters.
7.6. Define pass band and stop band of a filter.
7.7. What is the roll-off rate of a first order filter?
7.8. Why do we use higher order filters?
7.9. On what does the damping coefficient of a filter depend?
7.10. What is a Sallen-Key filter?
7.11. Define Bessel, Butterworth and Chebyshev filters, and compare their response.
7.12. What are the important parameters of a band pass filter?
7.13. Define a Notch filter.
7.14. How do we get a notch filter from a band pass filter?
7.15. Define a state variable filter.

7.16. What is a switched capacitor? Discuss its importance.
7.17. Discuss various types of switched capacitors.
7.18. Give the circuit of a switched capacitor low pass filter.

PROBLEMS

7.1. Design a first order low pass filter for a high cut-off frequency of 2 kHz and pass band gain of 2.
7.2. Determine the order of the Butterworth low pass filter so that at $\omega = 1.5\ \omega_{3\text{-dB}}$, the magnitude response is down by at least 30 dB.
7.3. In the circuit of Fig. 7.4, $R = 3.3$ kΩ, $C = 0.047$ μF, $R_i = 27$ kΩ and $R_f = 20$ kΩ. Calculate the high frequency cut-off f_h and pass band gain A_0.
7.4. A low-pass Butterworth filter is to be designed to have a 3-dB bandwidth of 200 Hz and an attenuation of 50 dB at 400 Hz. Find the order of the filter.
7.5. Design a fourth order Butterworth low pass filter whose bandwidth is 1 kHz. Select all capacitors equal to 1000 nF.
7.6. Design a HPF at a cut-off frequency of 1 kHz and a pass band gain of 2.
7.7. Design a band pas filter so that $f_0 = 2$ kHz, $Q = 20$ and $A_0 = 10$. Choose $C = 1$ μF.
7.8. Design a notch filter for $f_0 = 8$ kHz and $Q = 10$. Choose $C = 500$ pF.
7.9. An ideal LPF having $f_h = 5$ kHz is cascaded with HPF having $f_\ell = 4.8$ kHz. Sketch the frequency response of the cascaded filter.
7.10. Find the transfer function of the circuits shown in Fig. P.7.10.

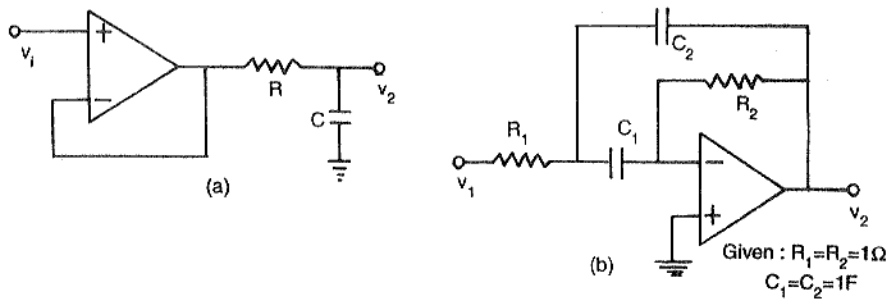

Fig. P. 7.10

7.11. Realize the circuit shown in Fig. P.7.10 using switched capacitors.
7.12. Find suitable component values of a lossy integrator of Fig. 7.25 (a), using switched capacitors. Given $f_h = 1$ kHz and low frequency gain of 10.

Experiment 7.1

To construct and plot the frequency response of a second order low pass, high pass filter. To measure the cut-off frequency in each case and verify with theoretical values.

Procedure

Low Pass Filter

1. Connect the circuit as shown in Fig. E.7.1 using discrete components. The values of the components have been taken from the Example 7.1. Please note that the Fig. E.7.1 has been numbered for the computer program 7.1.
2. Given an input signal v_i of 1 V peak to peak and measure the output voltage for different input frequencies (e.g. 100 Hz, 200 Hz, 500 Hz, 1 kHz, 1.5 kHz, 2.0 kHz, 5 kHz, 10 kHz).
3. Plot the frequency response 20 log (v_0/v_i) versus input signal frequency and find the 3 dB frequency from here.

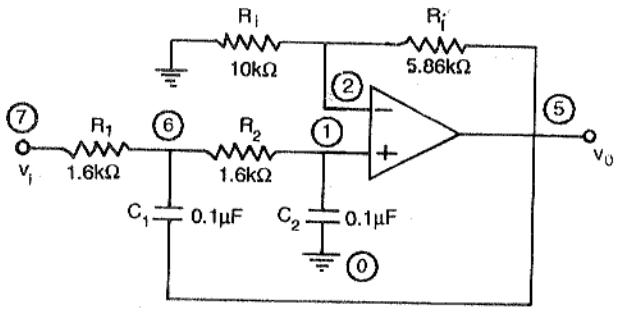

Fig. E.7.1 Second order low-pass filter

4. Calculate the theoretical value of upper cut-off frequency f_h and the pass band gain A_0:

$$f_h = \frac{1}{2\pi RC}; \quad \begin{bmatrix} R_1 = R_2 = R \\ C_1 = C_2 = C \end{bmatrix}$$

$$A_0 \text{ (dB)} = 20 \log \left(1 + \frac{R_f}{R_i}\right)$$

High Pass Filter

5. Interchange the resistor R with the capacitor C to make the high pass filter and repeat step 2 and 3.
6. Calculate the theoretical value of the lower cut-off frequency f_l and pass band gain A_0 using the formula of step 4.

Computer Program 7.1

Figure E.7.1 has been numbered for PSPICE simulation. The listing for this simulation is shown in Fig. C. 7.1(a) and the frequency response is shown in Fig. C. 7.1(b).

Fig. C. 7.1 (a) Program Listing

*2nd order low pass Butterworth filter (Sallen key filter)

```
* * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
    *LOWPASS BUTTERWORTH FILTER
    R1  7  6  1.6K
    R2  6  1  1.6K
    C1  6  5  0.1uF
    C2  1  0  0.1uF
    Ri  0  2  10K
    Rf  2  5  5.86k
*   Op-amp analysis
    X1  1  2  3  4  5  UA741
    .LIB  EVAL.LIB
*   Power supplies
    VCC  3  0  dc  12V
    VEE  0  4  dc  12V
    VIN  7  0  Ac  1V
    . AC DEC 20 1HZ 10 kHZ
    . PROBE
    □
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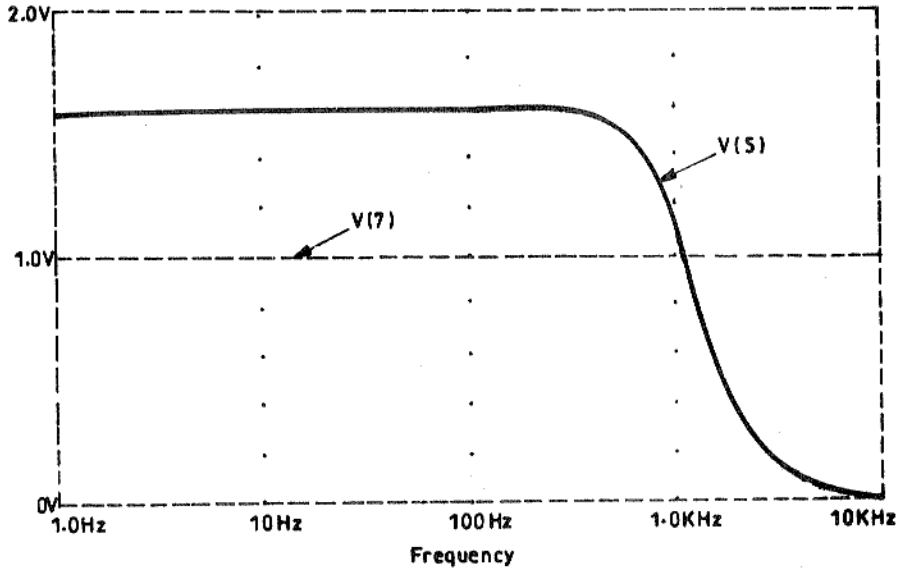


Fig. C. 7.1 (b) Frequency response of 2nd order low-pass filter

APPENDIX 7.1

Approximation Methods for Filter Design

We here consider techniques for approximating ideal filter transmission characteristics specifically for low pass filter.

Consider a realizable magnitude function that approximates the ideal low pass characteristics shown by dotted curve in Fig. 7.1 (a).

$$|H(j\omega)| = \frac{H(0)}{\sqrt{1+(\omega/\omega_0)^{2n}}}; n = 1, 2, 3 \ldots. \qquad \text{(A.7.1)}$$

This is known as the n-th order Butterworth or maximally flat response at $\omega = 0$. From the Binomial series expansion, $H(j\omega)$ can be written as †

$$|H(j\omega) = H(0)\left[1+\left(\frac{\omega}{\omega_0}\right)^{2n}\right]^{-1/2}$$

$$= H(0)\left[1-\frac{1}{2}\left(\frac{\omega}{\omega_0}\right)^{2n}+\frac{3}{8}\left(\frac{\omega}{\omega_0}\right)^{4n}-\frac{5}{16}\left(\frac{\omega}{\omega_0}\right)^{6n}+\ldots.\right] \qquad \text{(A.7.2)}$$

It can be seen that the first $(2n - 1)$ derivatives of $H(\omega)$ are zero at $\omega = 0$. Naturally approximation improves as n increases.

The pole locations corresponding to Eq. (A. 7.1) can be determined as,

$$|H(s)|^2 = H(s)\,H(-s) = \frac{H^2(0)}{1+(-s^2)^n} \qquad \text{(A. 7.3)}$$

The location of poles of $H(s)$ are found from,

$$1 + (-s^2)^n = 0 \qquad \text{(A. 7.4)}$$

The pole locations are:

$$s_k = \exp\left[j\left(\frac{2k-1}{n}\right)\frac{\pi}{2}\right]; n \text{ even} \qquad \text{(A. 7.5)}$$

$$s_k = \exp\left[j\,\frac{2k}{n}\cdot\frac{\pi}{2}\right]; n \text{ odd} \qquad \text{(A. 7.6)}$$

$$s_k = \exp\left[j\,\frac{2k+n-1}{2n}\cdot\frac{\pi}{2}\right]; k = 1, 2, \ldots.., 2n. \qquad \text{(A. 7.7)}$$

† $(1+x)^{-n} = 1+(-n)x+\frac{(-n)(-n-1)}{2!}x^2+\frac{(-n)(-n-1)(-n-2)}{3!}x^3+\ldots$

It may be noted that:

(i) Poles are located on a unit circle in the s-plane and have symmetry with respect to both real imaginary axis.
(ii) No poles lie on the imaginary axis.
(iii) Poles are separated by π/n radians.
(iv) A symmetric pair of poles is located on real axis for n odd.
(v) Poles are located at $\pi/2n$ radians from the real axis for n even.
(vi) Poles are located and $\pi/2n$ radians from the imaginary axis for n odd. Pole locations for $n = 4$ and $n = 5$ are shown in Fig. A. 7.1. Computation of poles upto $n = 6$ is given in Table A. 7.1.

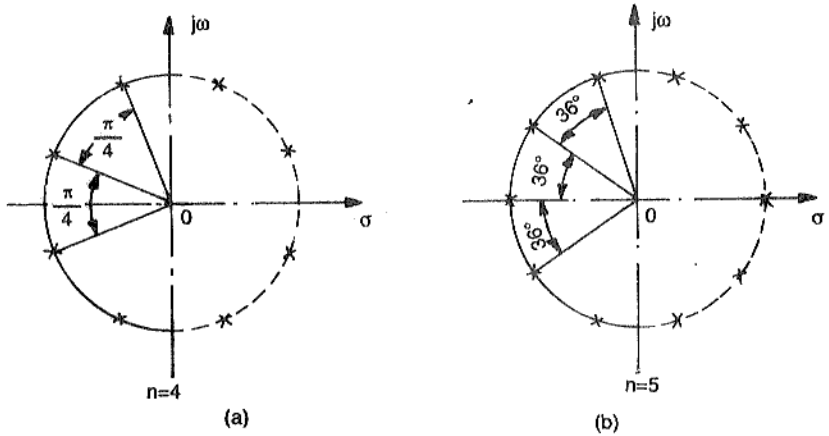


Fig. A. 7.1 Pole locations of Butterworth response function for $n = 4$ and $n = 5$ order

The transfer function $H(s)$ for an n-th order low pas filter is written as,

$$H(s) = \frac{H(0)}{s^n + b_{n-1}s^{n-1}+\ldots+b_1 s+1} \qquad \text{(A. 7.8)}$$

For stable operation, only the left half poles have been considered rejecting all right half plane poles.

The Butterworth polynomials which define the denominator of $H(s)$ in Eq. (A. 7.8) for even and odd are given by,

$$n \text{ even: } \prod_{k=1.}^{n/2}\left[s^2+(2\cos\theta_k)\,s+1\right]; \theta_k = \left(\frac{2k-1}{n}\right)\pi/2 \qquad \text{(A. 7.9)}$$

$$n \text{ odd: } (s+1)\prod_{l=1}^{(n-1)}\left[s^2+(2\cos\theta_\ell)\,s+1\right]; \theta_\ell = \frac{l\pi}{n} \qquad \text{(A. 7.10)}$$

The Butterworth polynomials upto $n = 6$ are also shown in the Table A. 7.1.

Table A. 7.1 Computation of Butterworth Polynomial

n	Angles from either real axis; in degrees	$\lvert\cos\theta\rvert$	$\alpha = 2\cos\theta$	Butterworth Polynomial
1.	0	1		$s + 1$
2.	± 45	0.70711	1.414	$s^2 + 1.414\,s + 1$
3.	0 ± 60	1 0.5	1	$(s + 1)(s^2 + s + 1)$ $= s^3 + 2s^2 + 2s + 1$
4.	± 22.5 ± 67.5	0.92388 0.38268	1.84776 0.76536	$(s^2 + 1.848\,s + 1)(s^2 + 0.765\,s + 1) = s^4 + 2.613\,s^3 + 3.414\,s^2 2.613\,s + 1$
5.	0 ± 36 ± 72	1 0.80902 0.30902	 1.61804 0.61804	$(s + 1)(s^2 + 1.618\,s + 1)(s^2 + 0.618s + 1)$ $= s^5 + 3.236s^4 + 5.236s^3 + 5.236s^2 + 3.236s + 1$
6.	± 15 ± 45 ± 75	0.96593 0.70711 0.25822	1.93186 1.41422 0.51644	$(s^2 + 1.932s + 1)(s^2 + 1.414s + 1)(s^2 + 0.518s + 1)$ $= s^6 + 3.863s^5 + 7.464s^4 + 9.141s^3 + 7.464s^2 + 3.863s + 1$

8

555 Timer

8.1 INTRODUCTION

The 555 timer is a highly stable device for generating accurate time delay or oscillation. Signetics Corporation first introduced this device as the SE555/NE555 and it is available in two package styles, 8–pin circular style, TO–99 can or 8–pin mini DIP or as 14–pin DIP. The 556 timer contains two 555 timers and is a 14-pin DIP. There is also available counter timer such as Exar's XR-2240 which contains a 555 timer plus a programmable binary counter in a single 16-pin package. A single 555 timer can provide time delay ranging from microseconds to hours whereas counter timer can have a maximum timing range of days.

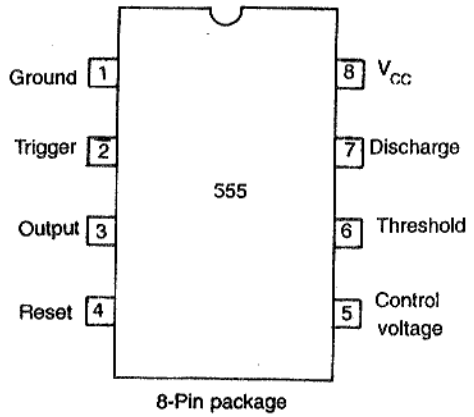


Fig. 8.1 Pin diagram

The 555 timer can be used with supply voltage in the range of + 5 V to + 18 V and can drive load upto 200 mA. It is compatible with both TTL and CMOS logic circuits. Because of the wide range of supply

voltage, the 555 timer is versatile and easy to use in various applications. Various applications include oscillator, pulse generator, ramp and square wave generator, mono-shot multivibrator, burglar alarm, traffic light control and voltage monitor etc.

8.2 DESCRIPTION OF FUNCTIONAL DIAGRAM

Figure 8.1 gives the pin diagram and Fig. 8.2 gives the functional diagram for 555 IC timer. Referring to Fig. 8.2, three 5 kΩ internal resistors act as voltage divider, providing bias voltage of (2/3) V_{cc} to the upper comparator (UC) and (1/3) V_{cc} to the lower comparator (LC), where V_{cc} is the supply voltage. Since these two voltages fix the necessary comparator threshold voltage, they also aid in determining the timing interval. It is possible to vary time electronically too, by applying a modulation voltage to the control voltage input terminal (pin 5). In applications, where no such modulation is intended, it is recommended by manufacturers that a capacitor (0.01 μF) be connected between control voltage terminal (pin 5) and ground to by-pass noise or ripple from the supply.

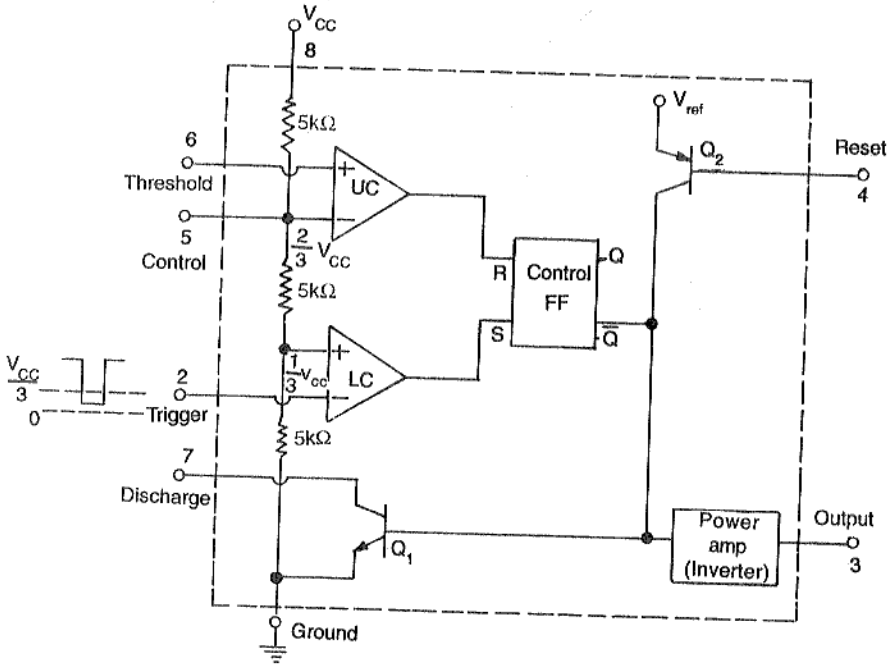


Fig. 8.2 Functional diagram of 555 timer

In the standby (stable) state, the output $\overline{Q}$ of the control flip-flop (FF) is HIGH. This makes the output LOW because of power amplifier which is basically an inverter. A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level

of the lower comparator (i.e. $V_{cc}/3$). At the negative going edge of the trigger, as the trigger passes through ($V_{cc}/3$), the output of the lower comparator goes HIGH and sets the FF ($Q = 1$, $\overline{Q} = 0$). During the positive excursion, when the threshold voltage at pin 6 passes through (2/3) V_{cc}, the output of the upper comparator goes HIGH and resets the FF ($Q = 0$, $\overline{Q} = 1$).

The reset input (pin 4) provides a mechanism to reset the FF in a manner which overrides the effect of any instruction coming to FF from lower comparator. This overriding reset is effective when the reset input is less than about 0.4 V. When this reset is not used, it is returned to V_{cc}. The transistor Q_2 serves as a buffer to isolate the reset input from the FF and transistor Q_1. The transistor Q_2 is driven by an internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

8.3 MONOSTABLE OPERATION

Figure 8.3 shows a 555 timer connected for monostable operation and its functional diagram is shown in Fig. 8.4. In the standby state, FF holds transistor Q_1 ***on***, thus clamping the external timing capacitor C to ground. The output remains at ground potential, i.e. LOW. As the trigger passes through $V_{cc}/3$, the FF is set, i.e. $\overline{Q} = 0$. This makes the transistor Q_1 ***off*** and the short circuit across the timing capacitor C is released. As $\overline{Q}$ is LOW, output goes HIGH (= V_{cc}). The timing cycle now begins. Since C is unclamped, voltage across it rises exponentially through R towards V_{cc} with a time constant RC

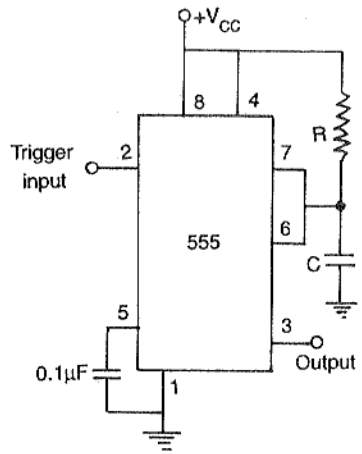


Fig. 8.3 Monostable multivibrator

as in Fig. 8.5(b). After a time period T (calculated later) the capacitor voltage is just greater than (2/3) V_{cc} and the upper comparator resets the FF, that is, $R = 1$, $S = 0$ (assuming very small trigger pulse width). This makes $\overline{Q} = 1$, transistor Q_1 goes ***on*** (i.e. saturates), thereby

discharging the capacitor C rapidly to ground potential. The output returns to the standby state or ground potential as shown in Fig. 8.5 (c).

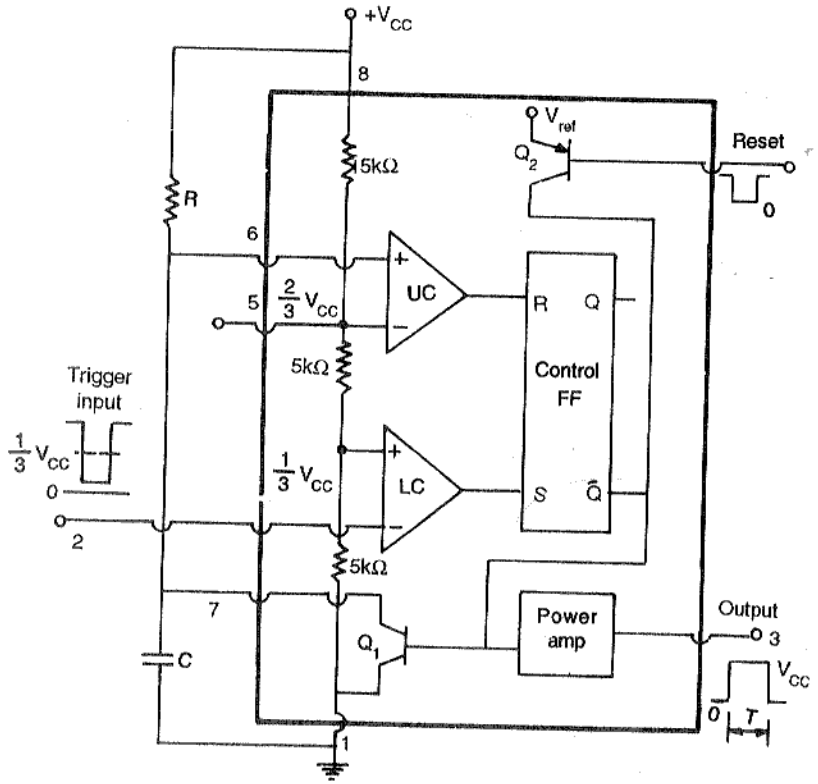


Fig. 8.4 Timer in monostable operation with functional diagram

The voltage across the capacitor as in Fig. 8.5(b) is given by

$$v_c = V_{cc}\,(1 - e^{-t/RC}) \qquad (8.1)$$

At $t = T$,

$$v_c = (2/3)\,V_{cc}$$

Therefore,

$$\frac{2}{3}V_{cc} = V_{cc}\,(1 - e^{-T/RC})$$

or,

$$T = RC \ln (1/3)$$

or,

$$T = 1.1\,RC \text{ (seconds)} \qquad (8.2)$$

It is evident from Eq. (8.2) that the timing interval is independent of the supply voltage. It may also be noted that once triggered, the output remains in the HIGH state until time T elapses, which depends only upon R and C. Any additional trigger pulse coming during this time will not change the output state. However, if a negative going reset pulse as in Fig. 8.5(d) is applied to the reset terminal (pin-4)

during the timing cycle, transistor Q_2 goes ***off***, Q_1 becomes ***on*** and the external timing capacitor C is immediately discharged. The output now will be as in Fig. 8.5 (e). It may be seen that the output of Q_2 is connected directly to the input of Q_1 so as to turn ***on*** Q_1 immediately and thereby avoid the propagation delay through the FF. Now, even

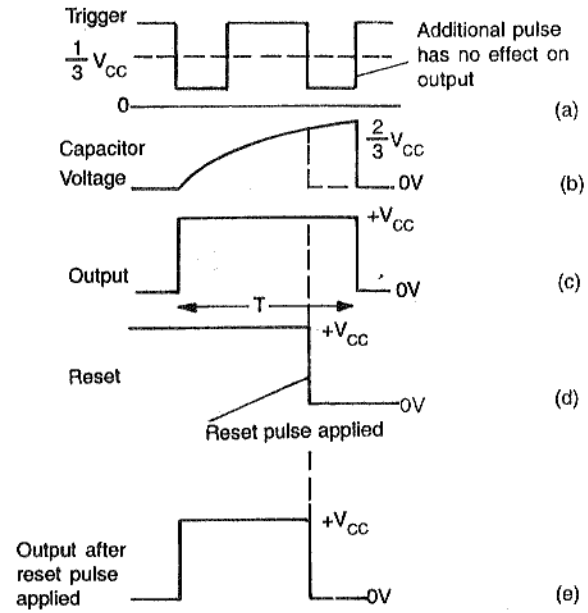


Fig. 8.5 Timing pulses

if the reset is released, the output will still remain LOW until a negative going trigger pulse is again applied at pin 2. Figure 8.6 shows a graph of the various combinations of R and C necessary to produce a given time delay.

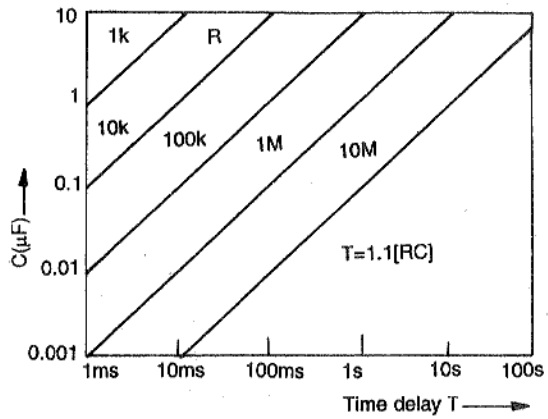


Fig. 8.6 Graph of *RC* combinations for different time delays

Sometimes the monostable circuit of Fig. 8.3 mistriggers on positive pulse edges, even with the control pin bypass capacitor. To prevent this, a modified circuit as shown in Fig. 8.7 is used. Here the resistor and capacitor combination of 10 kΩ and 0.001 μF at the input forms a differentiator. During the positive going edge of the trigger, diode D becomes forward biased, thereby limiting the amplitude of the positive spike to 0.7V.

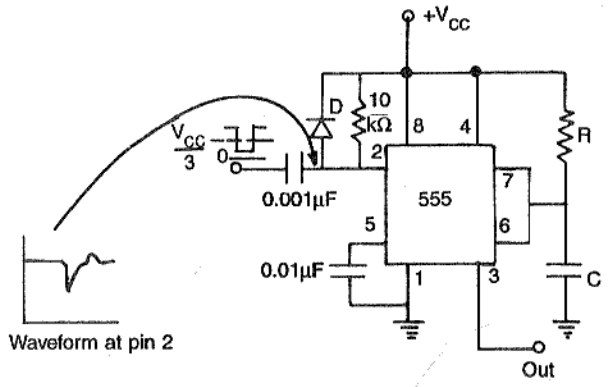


Fig. 8.7 Modified monostable circuit

Example 8.1

In the monostable multivibrator of Fig. 8.3, R = 100 kΩ and the time delay T = 100 mS. Calculate the value of C. Verify the value of C obtained from the graphs of Fig. 8.6.

Solution

From Eq. (8.2)., we get

$$C = T/1.1\ R = 100 \times 10^{-3}/1.1 \times 100 \times 10^{3} = 0.9\ \mu F$$

From the graph of Fig. 8.6, the value of C is found to be 0.9 μF also.

8.3.1 Applications in Monostable Mode

Missing Pulse Detector

Missing pulse detector circuit using 555 timer is shown in Fig. 8.8. Whenever, input trigger is low, the emitter diode of the transistor Q is forward biased. The capacitor C gets clamped to few tenths of a volt (~ 0.7V). The output of the timer goes HIGH. The circuit is designed so that the time period of the monostable circuit is slightly greater (1/3 longer) than that of the triggering pulses. So long the trigger pulse train keeps coming at pin 2, the output remains HIGH. However, if a pulse misses, the trigger input is high and transistor Q is cut off. The 555 timer enters into normal state of monostable operation. The output goes LOW after time T of the mono-shot. Thus this type of circuit can be used to detect missing heartbeat. It can also be used for

speed control and measurement. If input trigger pulses are generated from a rotating wheel, the circuit tells when the wheel speed drops below a predetermined value.

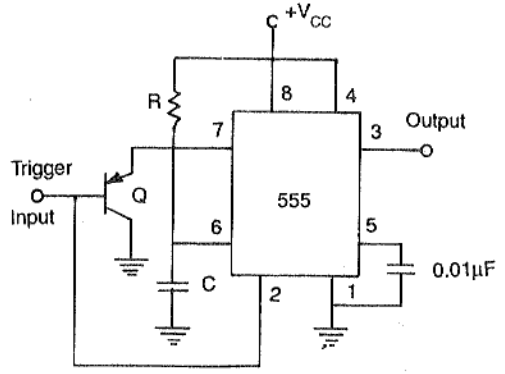


Fig. 8.8 A missing pulse detector monostable circuit

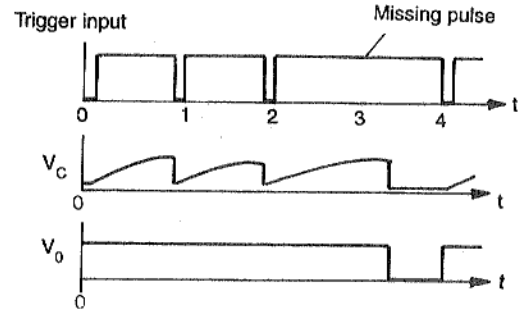


Fig. 8.9 Output of missing pulse detector

Linear Ramp Generator

Linear ramp can be generated by the circuit shown in Fig. 8.10. The resistor R of the monostable circuit is replaced by a constant current source. The capacitor is charged linearly by the constant current source formed by the transistor Q_3. The capacitor voltage v_c can be written as

$$v_c = \frac{1}{C}\int_0^t i\,dt \tag{8.3}$$

where i is the current supplied by the constant current source. Further, the KVL equation can be written as

$$\frac{R_1}{R_1 + R_2}\ V_{cc} - V_{BE} = (\beta + 1) I_B R_E \approx \beta I_B R_E = I_C R_E = i R_E \tag{8.4}$$

where I_B, I_C are the base current and collector current respectively, β is the current amplification factor in CE-mode and is very high. Therefore,

$$i = \frac{R_1 V_{cc} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2)} \tag{8.5}$$

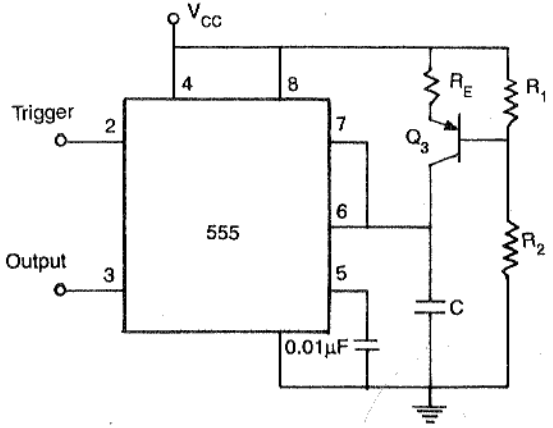


Fig. 8.10 Linear ramp generator

Now putting the value of the current i in Eq. (8.3), we get

$$v_c = \frac{R_1 V_{cc} - V_{BE}(R_1 + R_2)}{C\, R_E (R_1 + R_2)} \times t \tag{8.6}$$

At time $t = T$, the capacitor voltage v_c becomes (2/3) V_{cc}. Then we get

$$\frac{2}{3} V_{cc} = \frac{R_1 V_{cc} - V_{BE}(R_1 + R_2)}{R_E (R_1 + R_2) C} \times T \tag{8.7}$$

which gives the time period of the linear ramp generator as

$$T = \frac{(2/3)\, V_{cc} R_E (R_1 + R_2) C}{R_1 V_{cc} - V_{BE}(R_1 + R_2)} \tag{8.8}$$

The capacitor discharges as soon as its voltage reaches (2/3) V_{cc} which is the threshold of the upper comparator in the monostable circuit functional diagram. The capacitor voltage remains zero till another trigger is applied. The various waveforms are shown in Fig. 8.11.

The practical values can be noted as
R_1 = 47 kΩ; R_2 = 100 kΩ; R_E = 2.7 kΩ; C = 0.1 μF.
V_{cc} = 5 V (any value between 5 to 18V can be chosen)

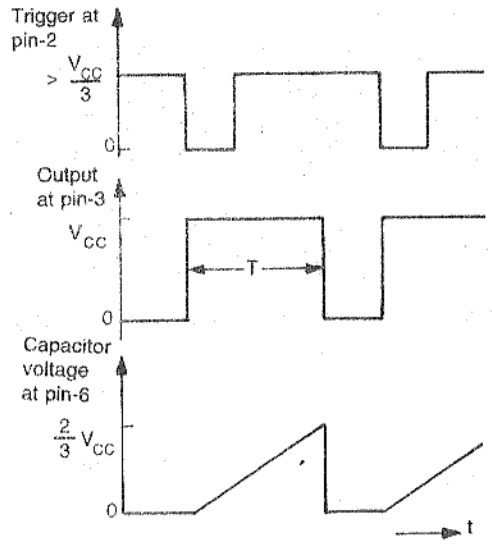


Fig. 8.11 Linear ramp generator output

Frequency Divider

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal. The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH (because of greater timing interval) for next negative going edge of the input square wave as shown in Fig. 8.12. The mono-shot will however be triggered on the third negative going input, depending on the choice of the time delay. In this way, the output can be made integral fractions of the frequency of the input triggering square wave.

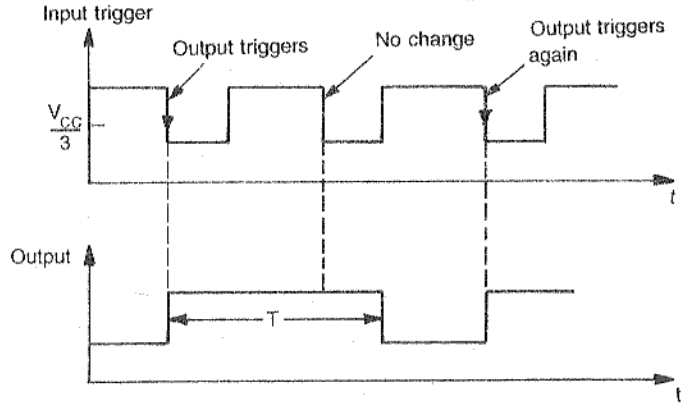


Fig. 8.12 Frequency divider circuit

Pulse Width Modulation

The circuit is shown in Fig. 8.13. This is basically a monostable multivibrator with a modulating input signal applied at pin-5. By the application of continuous trigger at pin-2, a series of output pulses are obtained, the duration of which depends on the modulating input at pin-5. The modulating signal applied at pin-5 gets superimposed upon the already existing voltage (2/3) V_{cc} at the inverting input terminal of UC. This in turn changes the threshold level of UC and the output pulse width modulation takes place. The modulating signal and the output waveform are shown in Fig. 8.14. It may be noted from the output waveform that the pulse duration, that is, the duty cycle only varies, keeping the frequency same as that of the continuous input pulse train trigger.

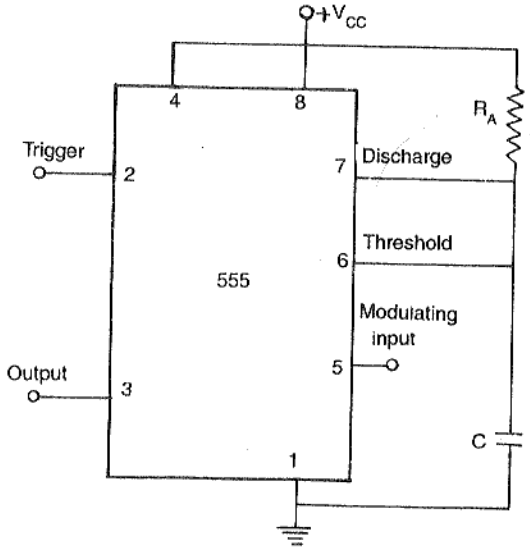
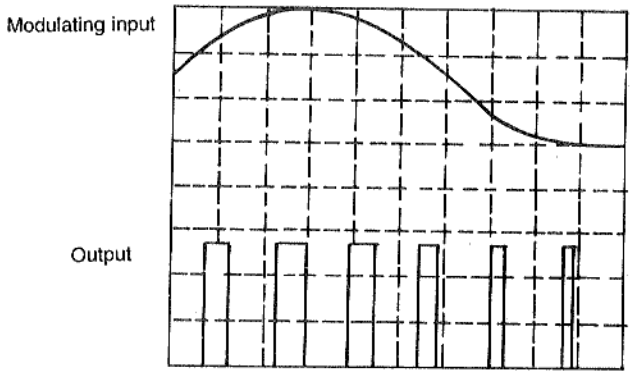


Fig. 8.13 Pulse width modulator



8.4 ASTABLE OPERATION

The device is connected for astable operation as shown in Fig. 8.15. For better understanding, the complete diagram of astable multivibrator with detailed internal diagram of 555 is shown in Fig. 8.16. Comparing with monostable operation, the timing resistor is now split into two sections R_A and R_B. Pin 7 of discharging transistor Q_1 is connected to the junction of R_A and R_B. When the power supply V_{cc} is connected, the external timing capacitor C charges towards V_{cc} with a time constant

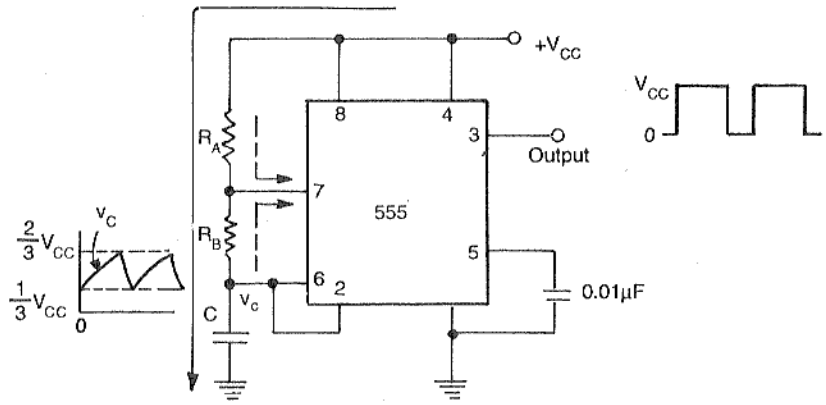


Fig. 8.15 Astable multivibrator using 555 timer

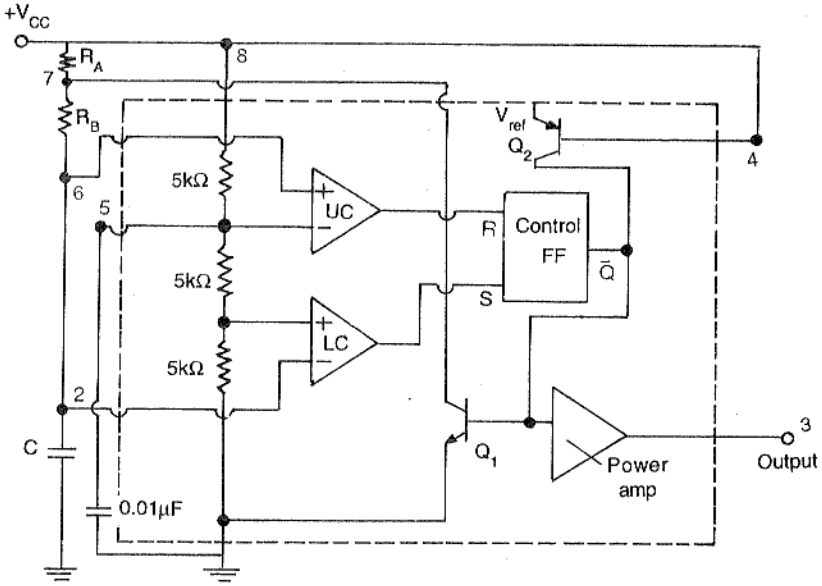


Fig. 8.16 Functional diagram of astable multivibrator using 555 timer

$(R_A + R_B)C$. During this time, output (pin 3) is high (equals V_{cc}) as Reset $R = 0$, Set $S = 1$ and this combination makes $\overline{Q} = 0$ which has unclamped the timing capacitor C.

When the capacitor voltage equals (to be precise is just greater than), (2/3) V_{cc} the upper comparator triggers the control flip-flop so that $\overline{Q} = 1$. This, in turn, makes transistor Q_1 ***on*** and capacitor C starts discharging towards ground through R_B and transistor Q_1 with a time constant R_BC (neglecting the forward resistance of Q_1). Current also flows into transistor Q_1 through R_A. Resistors R_A and R_B must be large enough to limit this current and prevent damage to the discharge transistor Q_1. The minimum value of R_A is approximately equal to $V_{cc}/0.2$ where 0.2 A is the maximum current through the ***on*** transistor Q_1.

During the discharge of the timing capacitor C, as it reaches (to be precise, is just less than) $V_{cc}/3$, the lower comparator is triggered and at this stage $S = 1$, $R = 0$, which turns $\overline{Q} = 0$. Now $\overline{Q} = 0$ unclamps the external timing capacitor C. The capacitor C is thus periodically charged and discharged between (2/3) V_{cc} and (1/3) V_{cc} respectively. Figure 8.17 shows the timing sequence and capacitor voltage wave form. The length of time that the output remains HIGH is the time for the capacitor to charge from (1/3) V_{cc} to (2/3) V_{cc}. It may be calculated as follows:

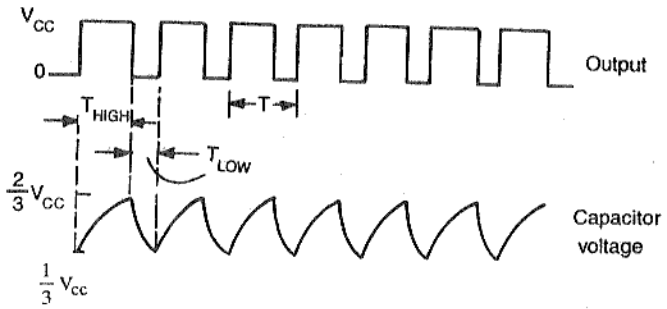


Fig. 8.17 Timing sequence of astable multivibrator

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by

$$v_c = V_{cc}(1 - e^{-t/RC})$$

The time t_1 taken by the circuit to charge from 0 to (2/3) V_{cc} is,

$$(2/3)\ V_{cc} = V_{cc}(1 - e^{-t_1/RC}) \qquad (8.9)$$

or, $$t_1 = 1.09\ RC$$

and the time t_2 to charge from 0 to (1/3) V_{cc} is,

$$(1/3)\ V_{cc} = V_{cc}(1 - e^{-t_2/RC}) \qquad (8.10)$$

or, $$t_2 = 0.405\ RC$$

So the time to charge from (1/3) V_{cc} to (2/3) V_{cc} is

$$t_{HIGH} = t_1 - t_2$$

$$t_{HIGH} = 1.09\ RC - 0.405\ RC = 0.69\ RC$$

So, for the given circuit,

$$t_{HIGH} = 0.69\ (R_A + R_B)C \qquad (8.11)$$

The output is low while the capacitor discharges from (2/3) V_{cc} to (1/3) V_{cc} and the voltage across the capacitor is given by

$$(1/3)\ V_{cc} = (2/3)V_{cc}\ e^{-t/RC}$$

solving, we get $t = 0.69\ RC$

So, for the given circuit, $t_{LOW} = 0.69\ R_BC$ (8.12)

Notice that both R_A and R_B are in the charge path, but only R_B is in the discharge path. Therefore, total time,

$$T = t_{HIGH} + t_{LOW}$$

or, $$T = 0.69\ (R_A + 2R_B)\ C$$

So, $$f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} \qquad (8.13)$$

Figure 8.18 shows a graph of the various combinations of $(R_A + 2R_B)$ and C necessary to produce a given stable output frequency. The duty cycle D of a circuit is defined as the ratio of ON time to the total time period $T = (t_{ON} + t_{OFF})$. In this circuit, when the transistor Q_1 is ***on***, the output goes low. Hence,

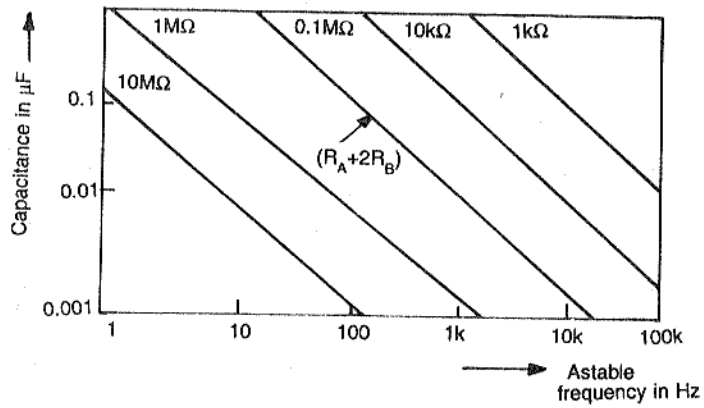


Fig. 8.18 Frequency dependence of R_A, R_B and C

$$D\% = \frac{t_{LOW}}{T} \times 100$$

$$= \frac{R_B}{R_A + 2R_B} \times 100 \qquad (8.14)$$

With the circuit configuration of Fig. 8.15 it is not possible to have a duty cycle more than 50% since $t_{HIGH} = 0.69\ (R_A + R_B)\ C$ will always be greater than $t_{LOW} = 0.69\ R_B C$. In order to obtain a symmetrical square wave i.e. $D = 50\%$, the resistance R_A must be reduced to zero. However, now pin 7 is connected directly to V_{cc} and extra current will flow through Q_1 when it is ***on***. This may damage Q_1 and hence the timer.

An alternative circuit which will allow duty cycle to be set at practically any level is shown in Fig. 8.19. During the charging portion of the cycle, diode D_1 is forward biased effectively short circuiting R_B so that

$$t_{HIGH} = 0.69\ R_A C$$

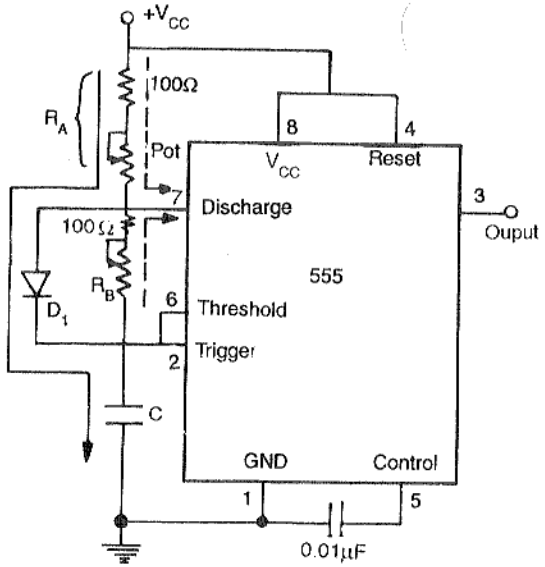


Fig. 8.19 Adjustable duty cycle rectangular wave generator

However, during the discharging portion of the cycle, transistor Q_1 becomes ON, thereby grounding pin 7 and hence the diode D_1 is reverse biased.

So $$t_{LOW} = 0.69\ R_B C \qquad (8.15)$$

$$T = t_{HIGH} + t_{LOW} = 0.69\ (R_A + R_B)\ C \qquad (8.16)$$

or, $$f = \frac{1.45}{(R_A + R_B)C} \qquad (8.17)$$

and duty cycle $$D = \frac{R_B}{R_A + R_B}$$

Resistors R_A and R_B could be made variable to allow adjustment of frequency and pulse width. However, a series resistor of atleast 100 Ω (fixed) should be added to each R_A and R_B. This will limit peak current to the discharge transistor Q_1 when the variable resistors are at minimum value. And, if R_A is made equal to R_B, then 50% duty cycle is achieved.

Symmetrical square wave generator by adding a clocked JK flip-flop to the output of the nonsymmetrical square wave generator is shown in Fig. 8.20. The clocked flip-flop acts as binary divider to the timer output. The output frequency in this case will be one half that of the timer. The advantage of this circuit is of having output of 50% duty cycle without any restriction on the choice of R_A and R_B.

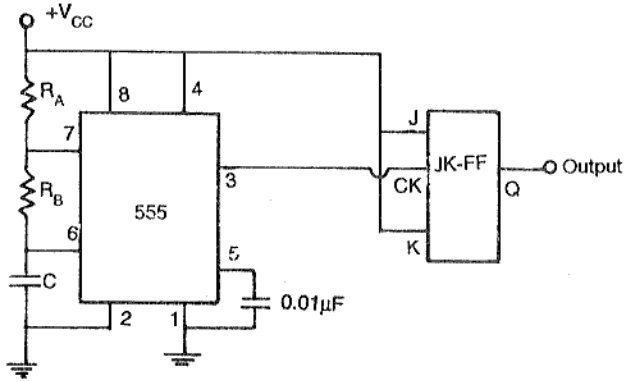


Fig. 8.20 Symmetrical waveform generator

Example 8.2

Refer Fig. 8.15. For $R_A = 6.8$ kΩ, $R_B = 3.3$ kΩ and $C = 0.1$ μF, calculate (a) t_{HIGH} (b) t_{LOW} (c) free running frequency (d) duty cycle, D.

Solution

(a) By Eq. (8.11)
$t_{HIGH} = 0.69\ (6.8\ k\Omega + 3.3\ k\Omega)\ (0.1\ \mu F) = 0.7$ ms

(b) By Eq. (8.12)
$t_{LOW} = 0.69\ (3.3\ k\Omega)\ (0.1\ \mu F) = 0.23$ ms

(c) $$f = \frac{1.45}{[(6.8\ k\Omega) + (2)\ (3.3\ k\Omega)]\ (0.1\ \mu F)} = 1.07\ kHz$$

(d) $$D = \frac{t_{LOW}}{T} = \frac{R_B}{R_A + 2R_B}$$

$$= \frac{3.3\ \text{k}\Omega}{6.8\ \text{k}\Omega + 2(3.3\ \text{k}\Omega)} = 0.25 \text{ or, } 25\%$$

8.4.1 Applications in Astable Mode

FSK Generator

In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called frequency shift keying (FSK) technique. A 555 timer in astable mode can be used to generate FSK signal. The circuit is as shown in Fig. 8.21. The standard digital data input frequency is 150 Hz. When input is HIGH, transistor Q is ***off*** and 555 timer works in the normal astable mode of operation. The frequency of the output waveform given by Eq. (8.1) can be rewritten as

$$f_o = \frac{1.45}{(R_A + 2R_B)C} \tag{8.18}$$

In a tele-typewriter using a modulator-demodulator (MODEM), a frequency between 1070 Hz to 1270 Hz is used as one of the standard FSK signals. The components R_A and R_B and the capacitor C can be selected so that f_o is 1070 Hz.

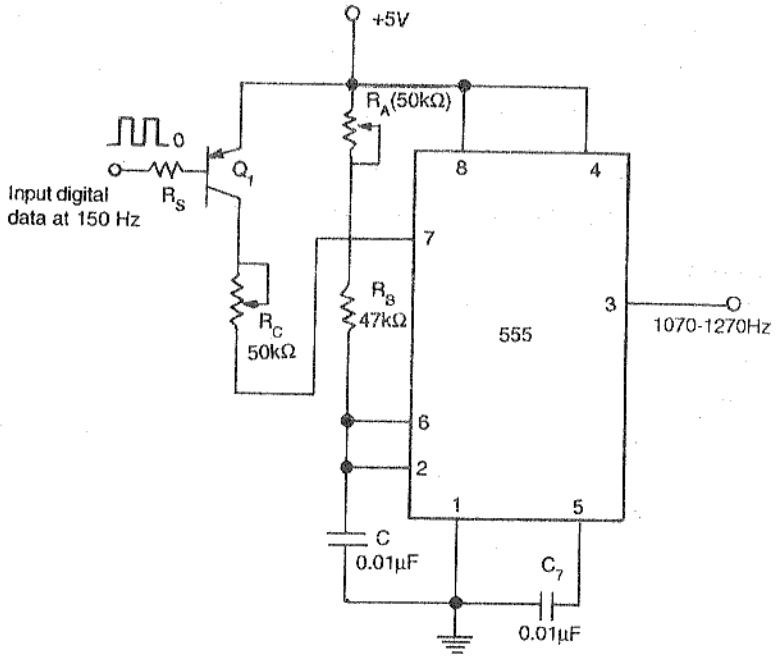


Fig. 8.21 FSK generator

When the input is LOW, Q goes ***on*** and connects the resistance R_c across R_A. The output frequency is now given by

$$\frac{1.45}{(R_A \parallel R_c) + 2R_B} \tag{8.19}$$

The resistance R_c can be adjusted to get an output frequency 1270 Hz.

Pulse-Position Modulator

The pulse-position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation

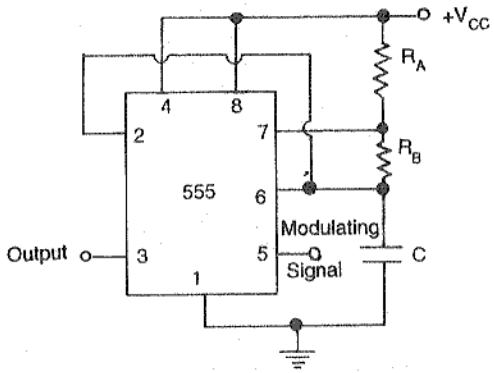


Fig. 8.22 Pulse position modulator

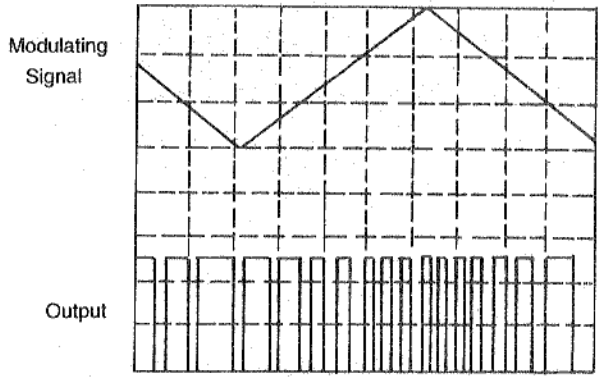


Fig. 8.23 Pulse position modulator output

as shown in Fig. 8.22. The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. Figure 8.23 shows the output waveform generated for a triangle wave modulation signal. It may be noted from the output waveform that the frequency is varying leading to pulse position modulation. The typical practical component values may be noted as

R_A = 3.9 kΩ, R_B = 3 kΩ, C = 0.01 μF

V_{cc} = 5V (any value between 5V to 18V may be chosen)

8.5 SCHMITT TRIGGER

The use of 555 timer as a Schmitt Trigger is shown in Fig. 8.24. Here the two internal comparators are tied together and externally biased at $V_{cc}/2$ through R_1 and R_2. Since the upper comparator will trip at (2/3) V_{cc} and lower comparator at (1/3) V_{cc}, the bias provided by R_1 and R_2 is centered within these two thresholds.

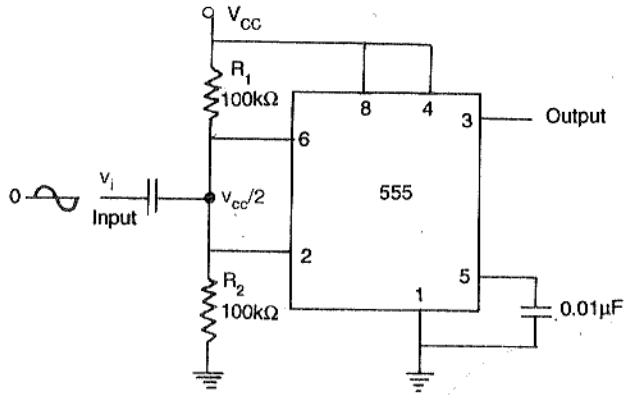


Fig. 8.24 Timer in Schmitt Trigger Operation

Thus, a sine wave of sufficient amplitude (> $V_{cc}/6$ = 2/3 V_{cc} – $V_{cc}/2$) to exceed the reference levels causes the internal flip-flop to alternately set and reset, providing a square wave output as shown in Fig. 8.25.

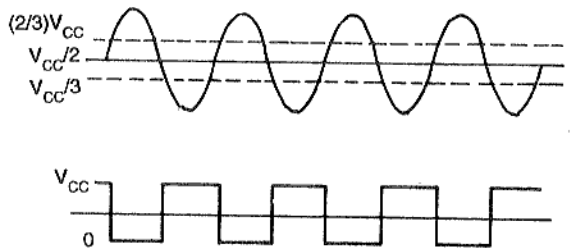


Fig. 8.25 Input output waveforms of Schmitt Trigger

It may be noted that unlike conventional multivibrator, no frequency division is taking place and frequency of square wave remains the same as that of input signal.

Summary

1. 555 IC Timer can produce very accurate and stable time delays, from microseconds to hours.
2. Timer is available in two packages, circular can and DIP.
3. It can be used with supply voltage varying from 5 to 18V and thus is compatible with TTL and CMOS circuits.

4. Timer can be used in monostable or astable mode of operation. Its various applications include waveform generator, missing pulse detector, frequency divider, pulse width modulator, burglar alarm, FSK generator, ramp generator, pulse position modulator etc.

Review Questions

8.1. Draw and explain the functional diagram of a 555 Timer.
8.2. Explain the function of reset.
8.3. What are the modes of operation of a timer?
8.4. Derive the expression of time delay of a monostable multivibrator.
8.5. Discuss some applications of timer in monostable mode.
8.6. Define duty cycle D.
8.7. Give methods for obtaining symmetrical square wave.
8.8. Discuss the operation of a FSK generator using 555 timer.
8.9. How is an astable multivibrator connected into a pulse position modulator?
8.10. Draw the circuit of a Schmitt trigger using 555 timer and explain its operation.

PROBLEMS

8.1. Design a monostable multivibrator using 555 timer to produce a pulse width of 100 ms. Verify the values of R and C obtained from the graph of Fig. 8.6.
8.2. The monostable multivibrator of Fig. 8.3 is used as a divide-by-3 network. The frequency of the input trigger is 15 kHz. If the value of C = 0.01 μF, calculate, the value of resistance R.
8.3. In the astable multivibrator of Fig. 8.15, R_A = 2.2 kΩ, R_B = 6.8 kΩ and C = .01 μF. Calculate (i) t_{HIGH} (ii) t_{LOW}, (iii) free running frequency, and (iv) duty cycle D.
8.4. Design a square waveform generator of frequency 100 Hz and duty cycle of 75%.
8.5. Design a symmetrical square waveform generator of 10 kHz.

Experiment

To construct and observe the waveforms of a 1 kHz square waveform generator using 555 timer for duty cycle, (a) D = 0.25; (b) D = 0.50.

Design aspects:

(a) Unsymmetrical square waveform generator

f = 1 kHz and D = 0.25

In Fig. 8.15, $$f = \frac{1.45}{(R_A + 2R_B)C}$$

and $$D = \frac{R_B}{R_A + 2R_B}$$

Select $C = 0.1\ \mu F$

Solving for R_A and R_B, we get

$$R_A = 3.6\ k\Omega;\ R_B = 5.5\ k\Omega$$

(b) Symmetrical square waveform generator

$$f = 1\ kHz \text{ and } D = 0.50$$

In the circuit of Fig. 8.19

$$f = \frac{1.45}{(R_A + R_B)C}$$

and $$D = \frac{R_B}{R_A + R_B}$$

Select $C = 0.1\ \mu F$

Use a diode 0A79

Solve for R_A and R_B. We get,

$$R_A = R_B = 7.25\ k\Omega$$

Procedure

1. Connect the circuit of Fig. 8.15 using component values as obtained in design part (a).
2. Observe and sketch the capacitor voltage waveform (pin-6) and output waveform (pin-3). Measure the frequency and duty cycle of the output waveform.
3. Next make the circuit of Fig. 8.19 using component values as obtained from design part (b).
4. Repeat step 2.

9

Phase-Locked Loops

9.1 INTRODUCTION

The phase-locked loop (PLL) is an important building block of linear systems. Electronic phase-locked loop (PLL) came into vogue in the 1930s when it was used for radar synchronisation and communication applications. The high cost of realizing PLL in discrete form limited its use earlier. Now with the advanced IC technology, PLLs are available as inexpensive monolithic ICs. This technique for electronic frequency control is used today in satellite communication systems, air borne navigational systems, FM communication systems, computers etc. The basic principle of PLL, different ICs and important applications are discussed.

9.2 BASIC PRINCIPLES

The basic block schematic of the PLL is shown in Fig. 9.1. This feedback system consists of:

1. Phase detector/comparator
2. A low pass filter
3. An error amplifier
4. A Voltage Controlled Oscillator (VCO)

The VCO is a free running multivibrator and operates at a set frequency f_o called free running frequency. This frequency is determined by an external timing capacitor and an external resistor. It can also be shifted to either side by applying a dc control voltage v_c to an appropriate terminal of the IC. The frequency deviation is directly proportional to the dc control voltage and hence it is called a "Voltage Controlled Oscillator" or, in short, VCO.

If an input signal v_s of frequency f_s is applied to the PLL, the phase detector compares the phase and frequency of the incoming signal to that of the output v_o of the VCO. If the two signals differ in frequency

and/or phase, an error voltage v_e is generated. The phase detector is basically a multiplier and produces the sum $(f_s + f_0)$ and difference $(f_s - f_0)$ components at its output. The high frequency component $(f_s + f_0)$ is removed by the low pass filter and the difference frequency

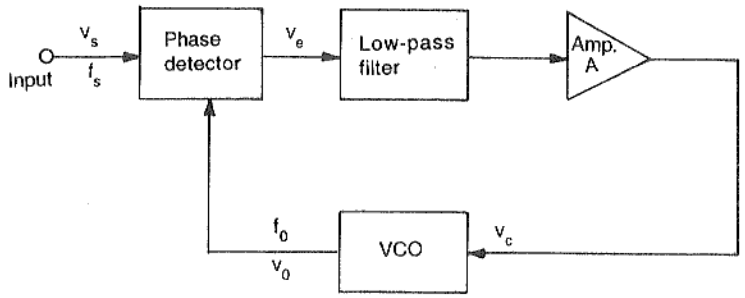


Fig. 9.1 Block schematic of the PLL

component is amplified and then applied as control voltage v_c to VCO. The signal v_c shifts the VCO frequency in a direction to reduce the frequency difference between f_s and f_0. Once this action starts, we say that the signal is in the capture range. The VCO continues to change frequency till its output frequency is exactly the same as the input signal frequency. The circuit is then said to be locked. Once locked, the output frequency f_0 of VCO is identical to f_s except for a finite phase difference ϕ. This phase difference ϕ generates a corrective control voltage v_c to shift the VCO frequency from f_0 to f_s and thereby maintain the lock. Once locked, PLL tracks the frequency changes of the input signal. Thus, a PLL goes through three stages (i) free running, (ii) capture and (iii) locked or tracking.

Figure 9.2 shows the capture transient. As capture starts, a small sine wave appears. This is due to the difference frequency between the VCO and the input signal. The dc component of the beat drives the VCO towards the lock. Each successive cycle causes the VCO frequency to move closer to the input signal frequency. The difference in frequency becomes smaller and a large dc component is passed by the filter, shifting the VCO frequency further. The process continues until the VCO locks on to the signal and the difference frequency is dc.

The low pass filter controls the capture range. If VCO frequency is far away, the beat frequency will be too high to pass through the filter and the PLL will not respond. We say that the signal is out of the capture band. However, once locked, the filter no longer restricts the PLL. The VCO can track the signal well beyond the capture band. Thus tracking range is always larger than the capture range.

Some of the important definitions in relation to PLL are:

Lock-in Range: Once the PLL is locked, it can track frequency changes in the incoming signals. The range of frequencies over which

the PLL can maintain lock with the incoming signal is called the lock-in range or tracking range. The lock range is usually expressed as a percentage of f_0, the VCO frequency.

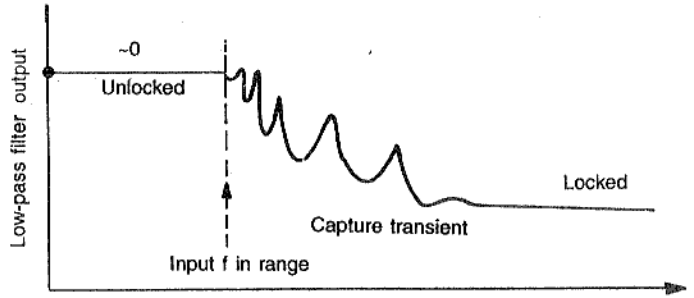


Fig. 9.2 The capture transient

Capture Range: The range of frequencies over which the PLL can acquire lock with an input signal is called the capture range. This parameter is also expressed as percentage of f_0.

Pull-in time: The total time taken by the PLL to establish lock is called pull-in time. This depends on the initial phase and frequency difference between the two signals as well as on the overall loop gain and loop filter characteristics.

9.3 PHASE DETECTOR/COMPARATOR

The phase detection is the most important part of the PLL system. There are two types of phase detectors used, analog and digital.

9.3.1 Analog Phase Detector

The principle of analog phase detection using switch type phase detector is shown in Fig. 9.3(a). An electronic switch S is opened and closed by signal coming from VCO (normally a square wave) as shown in Fig. 9.3(b). The input signal is, therefore, chopped at a repetition rate determined by VCO frequency. Figure 9.3(c) shows the input signal v_s assumed to be in phase ($\phi = 0°$) with VCO output v_0. Since the switch S is closed only when VCO output is positive, the output waveform v_e will be half sinusoids (shown hatched). Similarly, the output waveform for $\phi = 90°$ and $\phi = 180°$ is shown in Fig. 9.3(d, e). This type of phase detector is called a half wave detector, since the phase information for only one-half of the input waveform is detected and averaged. The output of the phase comparator when filtered through a low pass filter gives an error signal which is the average value of the output waveform shown by dotted line in Fig. 9.3(c, d, e).

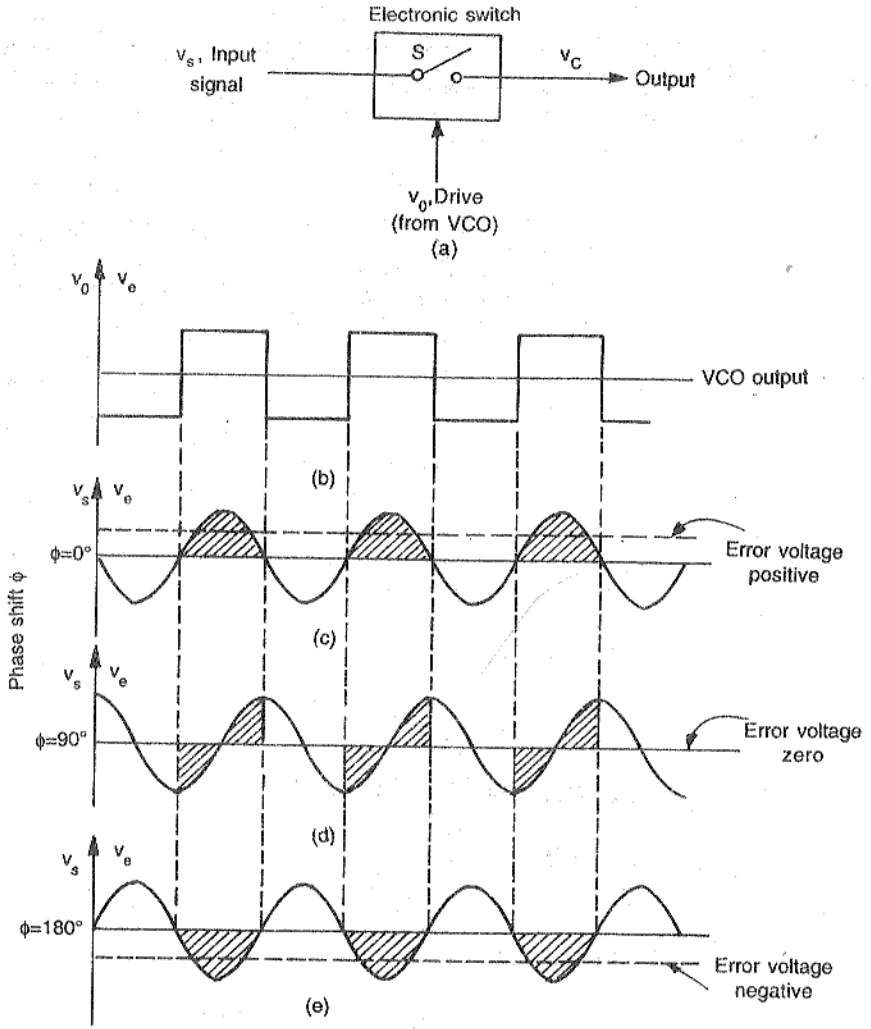


Fig. 9.3 Phase detector for PLL (a) Basic scheme (b) VCO output waveform. Input and output waveform (hatched) of phase detector for (c) $\phi = 0$ (d) $\phi = 90°$ (e) $\phi = 180°$

It may be seen that the error voltage is zero when the phase shift between the two inputs is 90°. So, for perfect lock, the VCO output should be 90° out of phase with respect to the input signal.

Analysis

A phase comparator is basically a multiplier which multiplies the input signal ($v_s = V_s \sin 2\pi f_s t$) by the VCO signal ($v_o = V_o \sin (2\pi f_o t + \phi)$). Thus the phase comparator output is,

$$v_e = KV_sV_o \sin (2\pi f_s t) \sin (2\pi f_o t + \phi) \qquad (9.1)$$

where K is the phase comparator gain (or attenuation constant) and ϕ is the phase shift between the input signal and the VCO output. Equation (9.1) can be simplified as,

$$v_e = \frac{KV_sV_o}{2}\left[\cos(2\pi f_s t - 2\pi f_o t - \phi) - \cos(2\pi f_s t + 2\pi f_o t + \phi)\right] \qquad (9.2)$$

when at lock, that is, $f_s = f_o$,

$$\text{Then } v_e = \frac{KV_sV_o}{2}\left[\cos(-\phi) - \cos(2\pi \times 2f_o t + \phi)\right]$$

This shows that the phase comparator output contains a double frequency term and a dc term $(KV_sV_o/2) \cos \phi$ which varies as a function of phase ϕ, that is, $\cos \phi$ between the two signals. The double frequency term is eliminated by the low pass filter and the dc signal is applied to the modulating input terminal of a VCO. It can be seen that in the perfect locked state ($f_s = f_o$), the phase shift should be 90° ($\cos 90° = 0$), in order to get zero error signal, that is, $v_e = 0$.

There are two problems associated with the switch type phase detector:

1. The output voltage v_e is proportional to the input signal amplitude V_s. This is undesirable since it makes phase detector gain and the loop gain dependent on the input signal amplitude.
2. The output is proportional to $\cos \phi$ and not proportional to ϕ making it non-linear.

Both these problems can be eliminated by limiting the amplitude of the input signal, that is, converting the input to a constant amplitude square wave. A circuit which performs phase comparison with square wave input is shown in Fig. 9.4(a). This is a balanced modulator used as full-wave switching phase detector. Here the input signal is applied to the differential pair Q_1Q_2. Transistors Q_3–Q_4 and Q_5–Q_6 are two sets of SPDT switches activated by the VCO output. The input signal v_s and the VCO output v_o are assumed to be high enough to switch the transistors in Fig. 9.4 (a) fully ***on*** or ***off***. In Fig. 9.4(b) when v_s and v_o both are high during the time 0 to $(\pi-\phi)$, transistors Q_1 and Q_3 are driven ***on*** and current I_E flows through Q_1 and Q_3. This gives an output voltage

$$v_e = -I_E R_L \qquad (9.4)$$

Next for the period $(\pi - \theta)$ for π, when v_s is high and v_o is low, transistors Q_1 and Q_4 are driven ***on*** resulting in an output voltage

$$v_e = I_E R_L \qquad (9.5)$$

In this way, the output voltage waveform v_e in Fig. 9.4(b) is obtained.

The average value of the phase detector output v_e can be calculated as,

$$(v_e)_{av} = \frac{1}{\pi}\left[(\text{area } A_1) + (\text{area } A_2)\right]$$

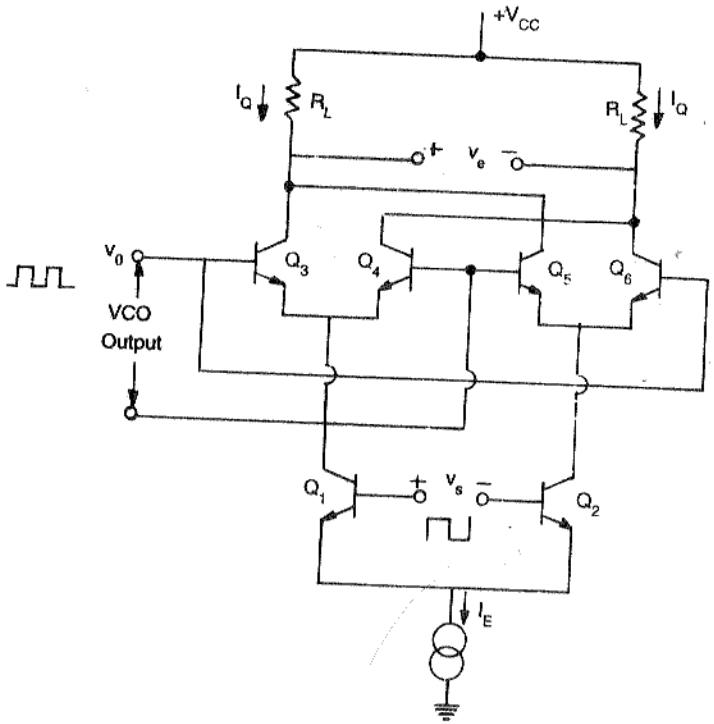


Fig. 9.4 (a) Phase detector for IC PLL

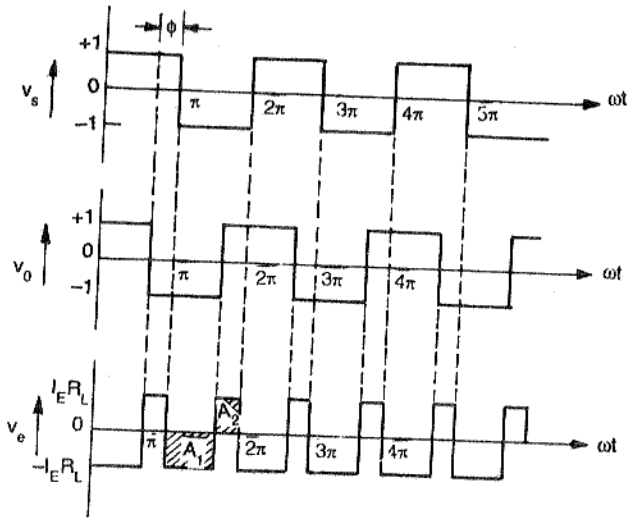


Fig. 9.4 (b) Timing diagram of input and output waveforms for balanced modulator circuit of Fig. 9.4 (a)

$$= \frac{1}{\pi}\left[I_E R_L \phi + (-I_E R_L) \times (\pi - \phi)\right]$$

$$= I_E R_L \left(\frac{2\phi}{\pi} - 1\right)$$

$$= 4\frac{I_Q R_L}{\pi}\left(\phi - \frac{\pi}{2}\right) \qquad [\text{Since } I_E = 2I_Q]$$

$$= K_\phi(\phi - \pi/2) \qquad (9.6)$$

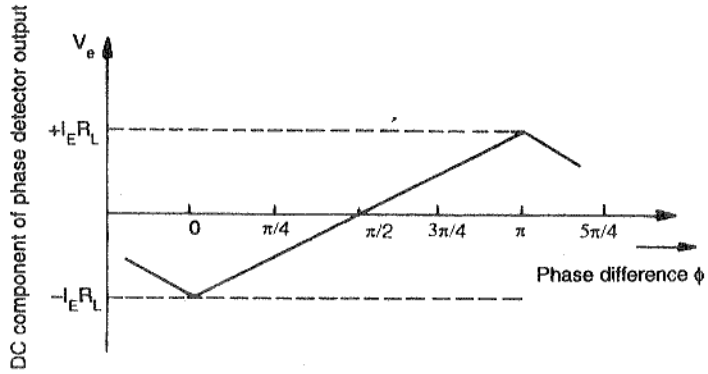


Fig. 9.4 (c) Output dc voltage versus input phase difference of balanced modulator full wave switching phase detector

where K_ϕ is the phase angle-to-voltage transfer coefficient or, the conversion ratio of the phase detector. This linear relationship between v_e and ϕ is depicted in Fig. 9.4 (c).

9.3.2 Digital Phase Detector

Figure 9.5(a) shows the digital type XOR (Exclusive–OR) phase detector. It uses CMOS type 4070 Quad 2-input XOR gate. The output of the XOR gate is high when only one of the inputs signals f_s or f_o is high. This type of detector is used when both the input signals are square waves. The input and output waveforms for $f_s = f_o$ are shown in Fig. 9.5(b). In this figure, f_s is leading f_o by ϕ degrees. The variation of dc output voltage with phase difference ϕ is shown in Fig. 9.5(c). It can be seen that the maximum dc output voltage occurs when the phase difference is π because the output of the gate remains high throughout. The slope of the curve gives the conversion ratio k_ϕ of the phase detector. So, the conversion ration K_ϕ for a supply voltage $V_{cc} = 5$V is,

$$K_\phi = \frac{5}{\pi} = 1.59 \text{ V/rad} \qquad (9.7)$$

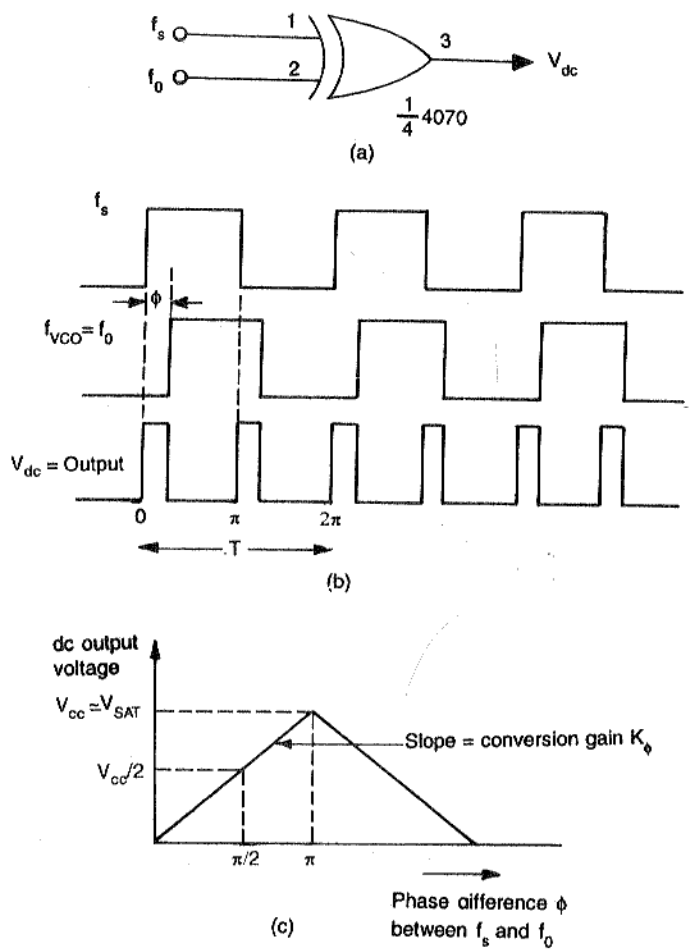


Fig. 9.5 (a) Exclusive-OR phase detector (b) Input and output waveforms (c) DC output voltage versus phase difference ϕ curve

Another type of digital phase detector is an edge-triggered phase detector as shown in Fig. 9.6(a). The circuit is an R-S flip-flop made by NOR gates, such as CD 4001. This circuit is useful when f_s (incoming signal) and f_0 (VCO output) are both pulse waveforms with duty cycle less than 50 percent. The output of the R-S flip-flop changes its state on the leading edge of f_s and f_0 as shown in Fig. 9.6(b). The variation of dc output voltage vs phase difference between f_s and f_0 is shown in Fig. 9.6(c). This type of detector has better capture tracking and locking characteristics as the dc output voltage is linear upto 360° compared to 180° in the case of Exclusive-OR detector.

Digital phase detector is also available in independent monolithic IC form. A typical example is MC4344/4044. This IC gives input/output transfer characteristics which is linear upto 4π radians or 720°.

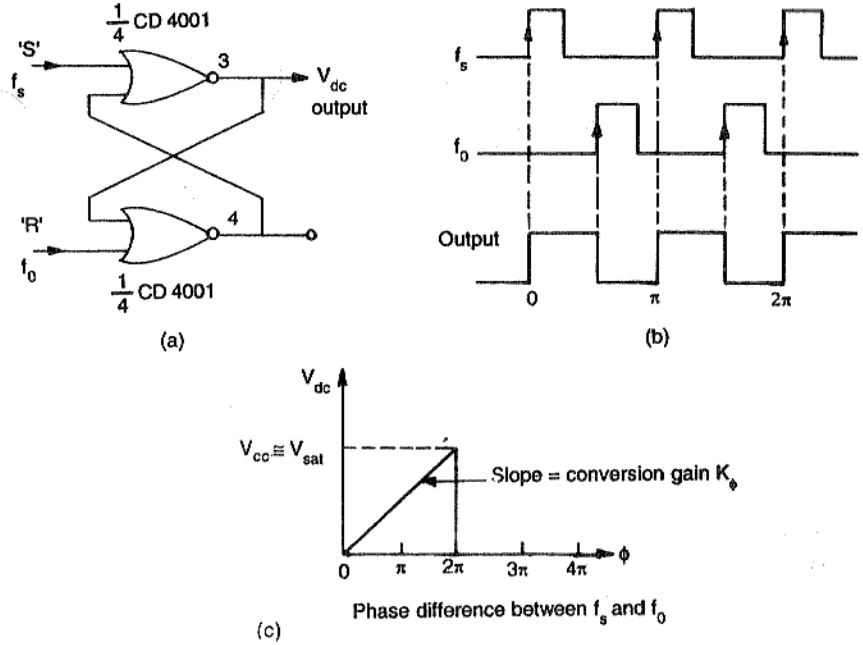
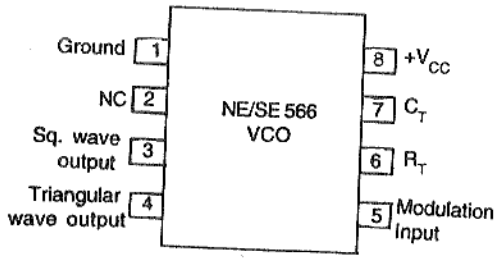


Fig. 9.6 (a) Edge-triggered phase detector using CD4001, Quad 2-input NOR gate (b) Input and output waveforms (c) dc output voltage vs phase difference ϕ

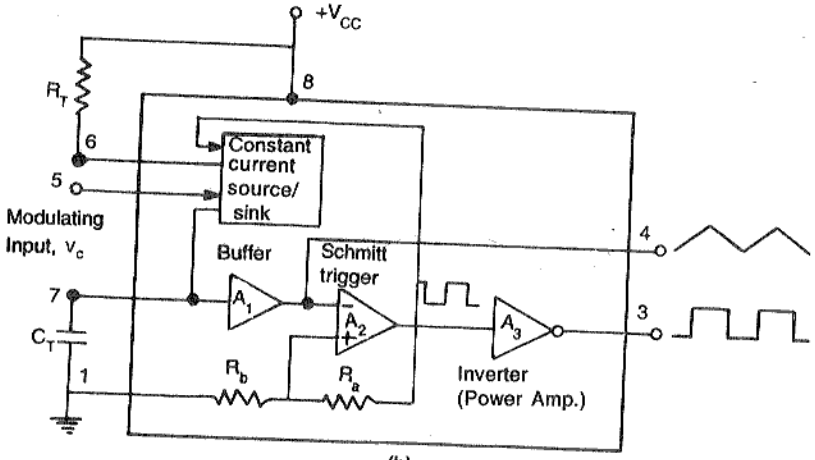
9.4 VOLTAGE CONTROLLED OSCILLATOR (VCO)

A common type of VCO available in IC form is Signetics NE/SE566. The pin configuration and basic block diagram of 566 VCO are shown in Fig. 9.7(a, b). Referring to Fig. 9.7(b), a timing capacitor C_T is linearly charged or discharged by a constant current source/sink. The amount of current can be controlled by changing the voltage v_c applied at the modulating input (pin 5) or by changing the timing resistor R_T external to IC chip. The voltage at pin 6 is held at the same voltage as pin 5. Thus, if the modulating voltage at pin 5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt trigger A_2 via buffer amplifier A_1. The output voltage swing of the Schmitt trigger is designed to V_{cc} and 0.5 V_{cc}. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from 0.5 V_{cc} to 0.25 V_{cc}. In Fig. 9.7(c), when the voltage on the capacitor C_T exceeds 0.5 V_{cc} during charging, the output of the Schmitt trigger goes LOW (0.5 V_{cc}). The capacitor now discharges and when it is at 0.25 V_{cc}, the output of Schmitt



(a)



(b)

Fig. 9.7 Voltage controlled oscillator (a) Pin configuration (b) Block diagram

trigger goes HIGH (V_{cc}). Since the source and sink currents are equal, capacitor charges and discharges for the same amount of time. This gives a triangular voltage waveform across C_T which is also available at pin 4. The square wave output of the Schmitt trigger is inverted* by inverter A_3 and is available at pin 3. The output waveforms are shown in Fig. 9.7(c).

The output frequency of the VCO can be calculated as follows:

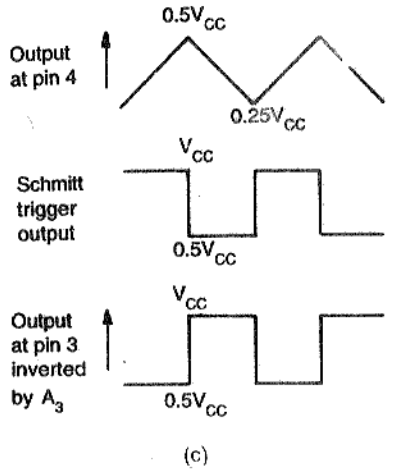
The total voltage on the capacitor changes from 0.25 V_{cc} to 0.5 V_{cc}. Thus $\Delta v = 0.25\ V_{cc}$. The capacitor chargers with a constant current source.

So
$$\frac{\Delta v}{\Delta t} = \frac{i}{C_T}$$

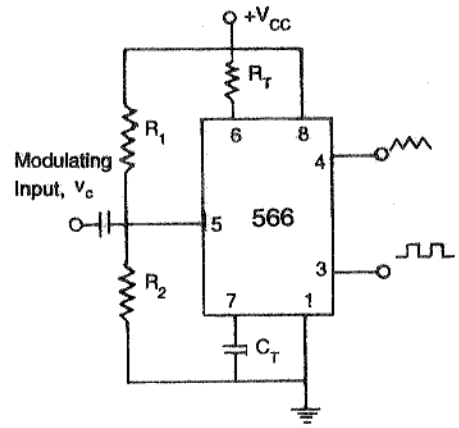
or,
$$\frac{0.25\ V_{cc}}{\Delta t} = \frac{i}{C_T}$$

or,
$$\Delta t = \frac{0.25\ V_{cc} C_T}{i} \qquad (9.8)$$

* An inverter is basically a current amplifier to drive the load.



(c)



(d)

Fig. 9.7 (c) Output waveform (d) Typical connection diagram

The time period T of the triangular waveform = $2\Delta t$. The frequency of oscillator f_o is,

$$f_o = \frac{1}{T} = \frac{1}{2\ \Delta t}$$

$$= \frac{i}{0.5\ V_{cc} C_T}$$

But,
$$i = \frac{V_{cc} - v_c}{R_T} \qquad (9.9)$$

where, v_c is the voltage at pin 5. Therefore,

$$f_o = \frac{2(V_{cc} - v_c)}{C_T R_T V_{cc}} \qquad (9.10)$$

The output frequency of the VCO can be changed either by (i) R_T, (ii) C_T or (iii) the voltage v_c at the modulating input terminal pin 5. The voltage v_c can be varied by connecting a R_1R_2 circuit as shown in Fig. 9.7(d). The components R_T and C_T are first selected so that VCO output frequency lies in the centre of the operating frequency range. Now the modulating input voltage is usually varied from 0.75 V_{cc} to V_{cc} which can produce a frequency variation of about 10 to 1. With no modulating input signal, if the voltage at pin 5 is biased† at (7/8) V_{cc}, Eq. (9.10) gives the VCO output frequency as,

† The expression of f_o depends upon the initial choice of the voltage v_c. If the value of v_c is taken as 0.85 V_{cc} then f_o comes out to be $0.3/R_TC_T$.

$$f_o = \frac{2(V_{cc} - (7/8)\,V_{cc})}{C_T R_T V_{cc}} = \frac{1}{4 R_T C_T} = \frac{0.25}{R_T C_T} \qquad (9.11)$$

Voltage to Frequency Conversion Factor

A parameter of importance for VCO is voltage to frequency conversion factor K_v and is defined as

$$K_v = \frac{\Delta f_0}{\Delta v_c}$$

Here Δv_c is the modulation voltage required to produce the frequency shift Δf_o for a VCO. If we assume that the original frequency is f_o and the new frequency is f_1, then

$$\Delta f_o = f_1 - f_o$$

$$= \frac{2(V_{cc} - v_c + \Delta v_c)}{C_T R_T V_{cc}} - \frac{2(V_{cc} - v_c)}{C_T R_T V_{cc}}$$

$$= \frac{2\,\Delta v_c}{C_T R_T V_{cc}} \qquad (9.12)$$

or, $$\Delta v_c = \frac{\Delta f_o\, C_T R_T V_{cc}}{2} \qquad (9.13)$$

Putting the value of $C_T R_T$ from Eq. (9.11)

$$\Delta v_c = \Delta f_o\, V_{cc}/8 f_o \qquad (9.14)$$

or, $$K_v = \frac{\Delta f_o}{\Delta v_c} = \frac{8 f_o}{V_{cc}} \qquad (9.15)$$

9.5 LOW PASS FILTER

The filter used in a PLL may be either passive type as shown in Fig. 9.8(a, b) or active type as in Fig. 9.8(c).

The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of the PLL. These characteristics include capture and lock range, band-width and transient response. If filter band-width is reduced, the response time increases. However, reducing the band-width of the filter also reduces the capture range of the PLL. The filter serves one more important purpose. The charge on the filter capacitor gives a short time 'memory' to the PLL. Thus, even if the signal becomes less than the noise for a few cycles, the dc voltage on the capacitor continues to shift the frequency of the VCO till it picks up signal again. This produces a high noise immunity and locking stability.

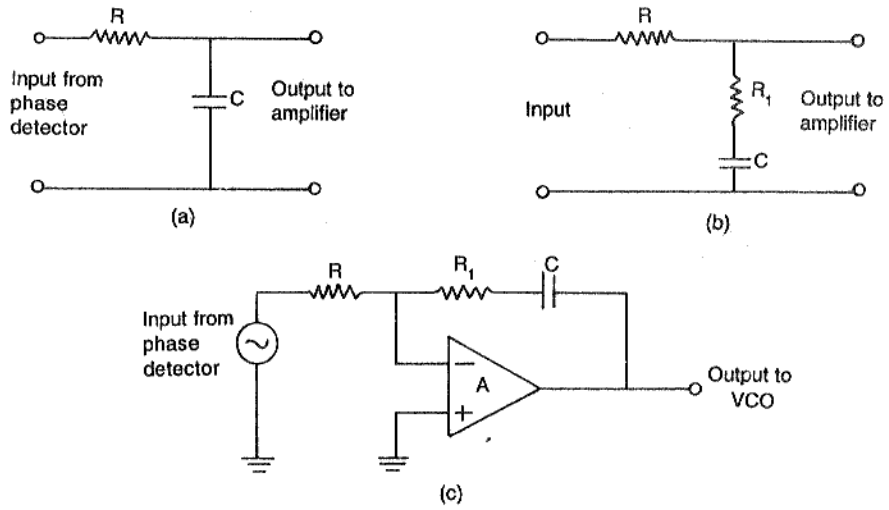


Fig. 9.8 Low pass filter (a, b) Passive filter (c) Active filter

9.6 MONOLITHIC PHASE-LOCKED LOOP

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However, a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE560 series introduced by Signetics and LM560 series by National Semiconductor. The SE/NE 560, 561, 562, 564, 565 and 567 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL, we will discuss some of the important features of this IC chip.

IC PLL 565

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in Fig. 9.9(a, b). The output frequency of the VCO (both inputs 2, 3 grounded) as given by Eq. (9.11) can be rewritten as,

$$f_o = \frac{0.25}{R_T C_T}\ \text{Hz} \qquad (9.16)$$

where R_T and C_T are the external resistor and capacitor connected to pin 8 and pin 9. A value between 2 kΩ and 20 kΩ is recommended for R_T. The VCO free running frequency is adjusted with R_T and C_T to be at the centre of the input frequency range. It may be seen that phase locked loop is internally broken between the VCO output and the

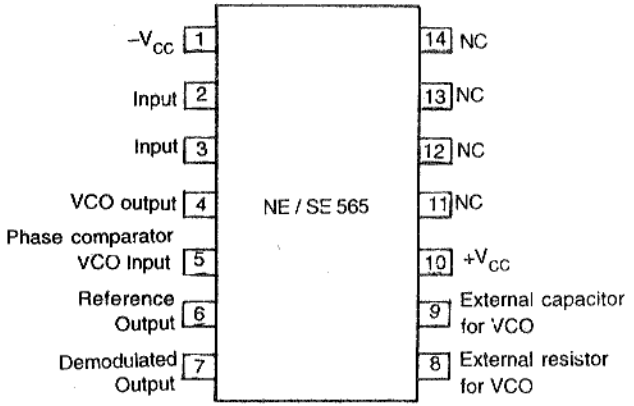


Fig. 9.9 (a) Pin diagram

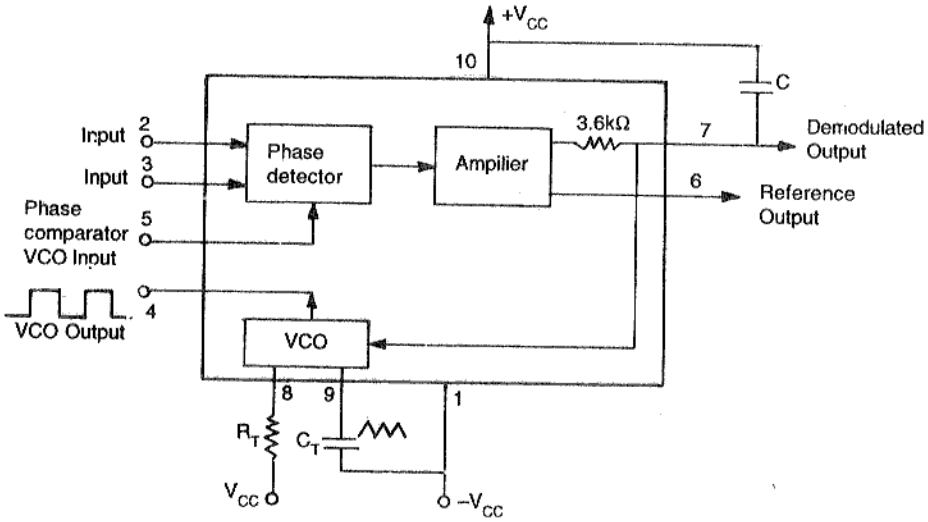


Fig. 9.9 (b) NE/SE565 PLL block diagram

phase comparator input. A short circuit between pins 4 and 5 connects the VCO output to the phase comparator so as to compare f_o with input signal f_s. A capacitor C is connected between pin 7 and pin 10 (supply terminal) to make a low pass filter with the internal resistance of 3.6 kΩ.

In Fig. 9.10, a complete diagram of LM565 (National Semiconductor) IC PLL is presented. The analog phase detector is comprised of the Q_1–Q_2, Q_3–Q_4 and Q_5–Q_6 differential amplifier pairs with Q_{37} together with R_3 (200 Ω) serving as a current sink bias source. Resistors R_1 and R_2 (each 7.2 kΩ) serve as the load for the phase detector. The output voltage of the phase detector is limited by the diode-connected transistors Q_7 and Q_8 to a maximum of ± 0.7 V which minimizes the

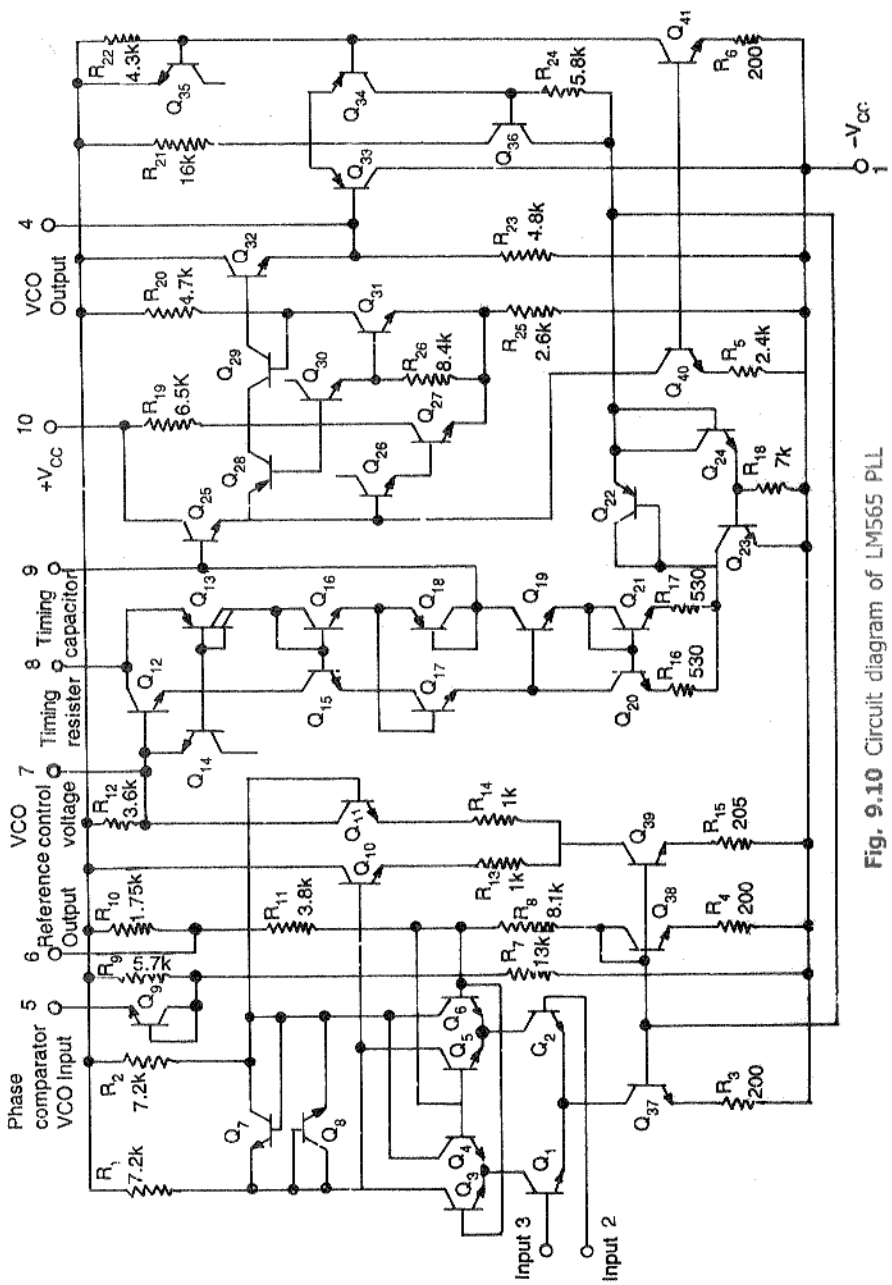


Fig. 9.10 Circuit diagram of LM565 PLL

effect of high amplitude noise pulses and other transient effect on the operation of the PLL. This makes the conversion ratio of the phase detector of 565 PLL as,

$$K_\phi = \frac{0.7 - (-0.7)}{\pi} = \frac{1.4}{\pi} \tag{9.17}$$

A balanced output is taken from the phase detector and supplied to the Q_{10}–Q_{11} differential pair which is biased by the Q_{39} current sink. Q_{10}–Q_{11} serves as the amplifier stage (which is designed for a gain of 1.4) after phase detector. A single ended output is taken from this stage across the resistors R_{12} (3.6 kΩ). Resistor R_{12} also serves as part of the LPF when an external capacitor between pin 7 and ground of is connected.

The VCO consists of a voltage controlled current source (Q_{12} through Q_{23}). Equal charging and discharging currents are supplied to external capacitor C_T connected at pin 9. Resistor R_T is connected between pin 8 and positive supply $+V_{cc}$. The Schmitt trigger (Q_{25} through Q_{36}) with the differential amplifier output circuit (Q_{33} and Q_{34}) is part of VCO. This controls the turn-on and turn-off of Q_{23} and Q_{24} for the switching action of the current source for the charging and discharging cycles. Transistor Q_{14}, Q_{26}, Q_{30}, Q_{35} are used as diodes to obtain the desired level shift.

The important electrical parameters of 565 PLL are:

Operating frequency range	:	0.001 Hz to 500 kHz
Operating voltage range	:	± 6V to ± 12V
Input level	:	10 mV rms min. to 3V pp max
Input impedance	:	10 kΩ typical
Output sink current	:	1 mA typical
Drift in VCO centre frequency with temperature	:	300 ppm/°C. (parts per million per degree centigrade)
Drift in VCO centre frequency with supply voltage	:	1.5 percent/V max
Triangle wave amplitude	:	2.4 V_{pp} at ± 6 V supply voltage
Square wave amplitude	:	5.4 V_{pp} at ± 6 V supply voltage
Bandwidth adjustment range	:	< ± 1 to ± 60%

Derivation of Lock-in Range

If ϕ radians is the phase difference between the signal and the VCO voltage, then the output voltage of the analog phase detector is given by,

$$v_e = K_\phi(\phi - \pi/2) \tag{9.18}$$

where K_ϕ is the phase angle-to-voltage transfer coefficient of the phase detector. The control voltage to VCO is,

$$v_c = AK_\phi(\phi - \pi/2) \tag{9.19}$$

where A is the voltage gain of the amplifier. This v_c shifts VCO frequency from its free running frequency f_o to a frequency f given by,

$$f = f_o + K_v v_c \tag{9.20}$$

where K_v is the voltage to frequency transfer coefficient of the VCO. When PLL is locked-in to signal frequency f_s, then we have

$$f = f_s = f_o + K_v v_c \tag{9.21}$$

since, $$v_c = (f_s - f_o)/K_v = A K_\phi (\phi - \pi/2) \tag{9.22}$$

Thus, $$\phi = \pi/2 + (f_s - f_o)/K_v K_\phi A \tag{9.23}$$

The maximum output voltage magnitude available from the phase detector occurs for $\phi = \pi$ and 0 radian (see in Fig. 9.4(c) and v_e (max) $= \pm K_\phi \pi/2$ from Eq. (9.6). The corresponding value of the maximum control voltage available to drive the VCO will be,

$$v_{c(max)} = \pm (\pi/2)\ K_\phi A \tag{9.24}$$

The maximum VCO frequency swing that can be obtained is given by,

$$(f - f_o)_{max} = K_v v_{c(max)} = K_v K_\phi A\ (\pi/2) \tag{9.25}$$

Therefore, the maximum range of signal frequencies over which the PLL can remain locked will be,

$$f_s = f_o \pm (f - f_o)_{max}$$
$$= f_o \pm K_v K_\phi\ (\pi/2) A = f_o \pm \Delta f_L \tag{9.26}$$

where $2\ \Delta f_L$ will be the lock-in frequency range and is given by,

lock-in range = $$2\,\Delta f_L = K_v K_\phi A\,\pi \tag{9.27}$$

or, $$\Delta f_L = \pm K_v K_\phi A\ (\pi/2) \tag{9.28}$$

The lock-in range is symmetrically located with respect to VCO free running frequency f_o. For IC PLL 565,

$$K_v = \frac{8 f_o}{V} \quad \text{(from Eq. (9.15))}$$

where $$V = +V_{cc} - (-V_{cc})$$

Again, $$K_\phi = \frac{1.4}{\pi} \quad \text{(from Eq. (9.17))}$$

and $$A = 1.4$$

Hence the lock-in range from Eq. (9.28) becomes,

$$\Delta f_L = \pm 7.8\ f_o/V \tag{9.29}$$

Derivation of Capture Range

When PLL is not initially locked to the signal, the frequency of the VCO will be free running frequency f_o. The phase angle difference between the signal and the VCO output voltage will be,

$$\phi = (\omega_s t + \theta_s) - (\omega_o t + \theta_o) = (\omega_s - \omega_o)t + \Delta\theta \tag{9.30}$$

thus the phase angle difference does not remain constant but will change with time at a rate given by

$$\frac{d\phi}{dt} = \omega_s - \omega_o \tag{9.31}$$

The phase detector output voltage will therefore not have a dc component but will produce an ac voltage with a triangular waveform of peak amplitude $K_\phi(\pi/2)$ and a fundamental frequency $(f_s - f_o) = \Delta_f$.

The low pass filter (LPF) is a simple RC network having transfer function

$$T(jf) = \frac{1}{1 + j(f/f_1)} \tag{9.32}$$

where $f_1 = 1/2\,\pi\,RC$ is the 3-dB point of LPF. In the slope portion of LPF where $(f/f_1)^2 >> 1$, then

$$T(f) \simeq \frac{f_1}{jf} \tag{9.33}$$

The fundamental frequency term supplied to the LPF by the phase detector will be the difference frequency $\Delta f = f_s - f_o$. If $\Delta f > 3f_1$, the LPF transfer function will be approximately,

$$T(\Delta f) \simeq f_1/\Delta f = f_1/(f_s - f_o) \tag{9.34}$$

The voltage v_c to drive the VCO is,

$$v_c = v_e \times T(f) \times A \tag{9.35}$$

or,
$$v_{c(max)} = v_{e(max)} \times T(f) \times A$$
$$= \pm K_\phi(\pi/2)A\ (f_1/\Delta f).\ \text{(from Eq. (9.24))} \tag{9.36}$$

Then the corresponding value of the maximum VCO frequency shift is,

$$(f - f_o)_{max} = K_v\, v_{c(max)} = \pm K_v K_\phi(\pi/2)A\ (f_1/\Delta f) \tag{9.37}$$

For the acquisition of signal frequency, we should put $f = f_s$ so that the maximum signal frequency range that can be acquired by PLL is,

$$(f_s - f_o)_{max} = \pm K_v K_\phi(\pi/2)A\ (f_1/\Delta f_c) \tag{9.38}$$

Now
$$\Delta f_c = (f_s - f_o)_{max}$$

so,
$$(\Delta f_c)^2 = K_v K_\phi(\pi/2)A f_1 \text{ (from Eq. (9.38))}$$

since,
$$\Delta f_L = \pm K_v K_\phi(\pi/2)A$$

we get,
$$(\Delta f_c) \simeq \pm\sqrt{f_1\,\Delta f_L} \tag{9.39}$$

Therefore, the total capture range is,

$$2\,\Delta f_c \simeq 2\sqrt{f_1\,\Delta f_L} \tag{9.40}$$

where the lock-in range $= 2\,\Delta f_L = K_v K_\phi A\,\pi$. In case of IC PLL 565, $R = 3.6$ kΩ, so the capture range is

$$\pm\left[\frac{\Delta f_L}{2\pi(3.6\times10^3)C}\right]^{\frac{1}{2}} \tag{9.41}$$

where C is in farads.

The capture range is symmetrically located with respect to VCO free running frequency f_o as is shown in Fig. 9.11. The PLL cannot acquire a signal outside the capture range, but once captured, it will hold on till the signal frequency goes beyond the lock-in range. In order to increase the ability of lock-in range, large capture range is required. However, a large capture range will make the PLL more susceptible to noise and undesirable signal. Hence a suitable compromise is often reached between these two opposing requirements of the

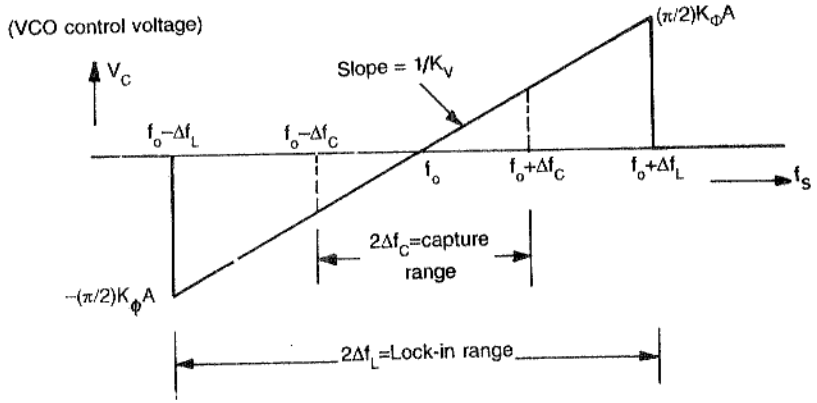


Fig. 9.11 PLL lock-in range and capture range

capture range. Many a times the LPF band-width is first set for a large value for initial acquisition of signal, then once the signal is captured, the band-width of LPF is reduced substantially. This will minimize the interference of undesirable signals and noise.

9.7 PLL APPLICATIONS

The output from a PLL system can be obtained either as the voltage signal $v_c(t)$ corresponding to the error voltage in the feedback loop, or

as a frequency signal at VCO output terminal. The voltage output is used in frequency discriminator application whereas the frequency output is used in signal conditioning, frequency synthesis or clock recovery applications.

Consider the case of voltage output. When PLL is locked to an input frequency, the error voltage $v_c(t)$ is proportional to $(f_s - f_0)$. If the input frequency is varied as in the case of FM signal, v_c will also vary in order to maintain the lock. Thus the voltage output serves as a frequency discriminator which converts the input frequency changes to voltage changes.

In the case of frequency output, if the input signal is comprised of many frequency components corrupted with noise and other disturbances, the PLL can be made to lock, selectively on one particular frequency component at the input. The output of VCO would then regenerate that particular frequency (because of LPF which gives output for beat frequency) and attenuate heavily other frequencies. VCO output thus can be used for regenerating or reconditioning a desired frequency signal (which is weak and buried in noise) out of many undesirable frequency signals.

Some of the typical applications of PLL are discussed now.

9.7.1 Frequency Multiplication/Division

Figure 9.12 gives the block diagram of a frequency multiplier using PLL. A divide by N network is inserted between the VCO output and the phase comparator input. In the locked state, the VCO output frequency f_0 is given by,

$$f_0 = N f_s \tag{9.42}$$

The multiplication factor can be obtained by selecting a proper scaling factor N of the counter.

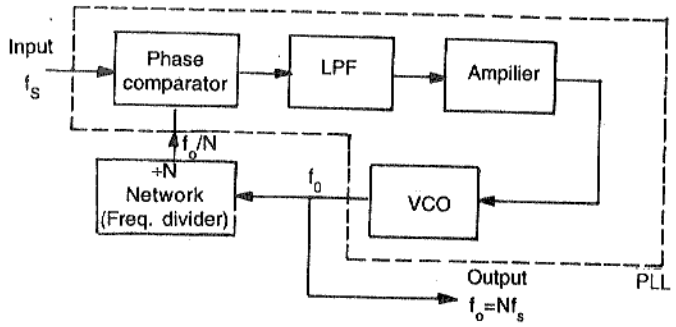


Fig. 9.12 Frequency multiplier using IC PLL

Frequency multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics e.g. square wave, pulse train etc., then VCO can be directly locked to the

n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of Fig. 9.12 can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_0 of VCO is now given by

$$f_0 = \frac{f_s}{m} \tag{9.43}$$

9.7.2 Frequency Translation

A schematic for shifting the frequency of an oscillator by a small factor is shown in Fig. 9.13. It can be seen that a mixer (or multiplier) and a low-pass filter are connected externally to the PLL. The signal f_s which has to be shifted and the output frequency f_0 of the VCO are applied as inputs to the mixer. The output of the mixer contains the sum and difference of f_s and f_0. However, the output of LPF contains only the difference signal $(f_0 - f_s)$. The translation or offset frequency $f_1 (f_1 << f_s)$ is applied to the phase comparator. When PLL is in locked state,

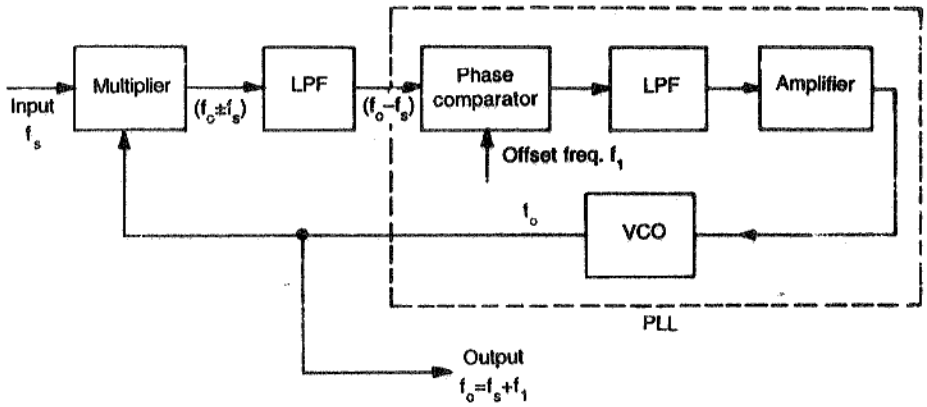


Fig. 9.13 PLL used as a frequency translator

$$f_0 - f_s = f_1$$

or

$$f_0 = f_s + f_1 \tag{9.44}$$

Thus, it is possible to shift the incoming frequency f_s by f_1.

9.7.3 AM Detection

A PLL may be used to demodulate AM signals as shown in Fig. 9.14. The PLL is locked to the carrier frequency of the incoming AM signal.

The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

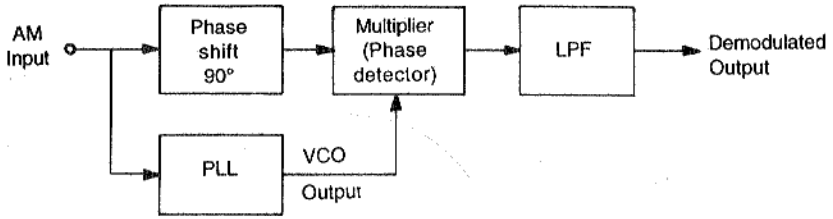


Fig. 9.14 PLL used as AM demodulator

9.7.4 FM Demodulation

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

9.7.5 Frequency Shift Keying (FSK) Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 9.15 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

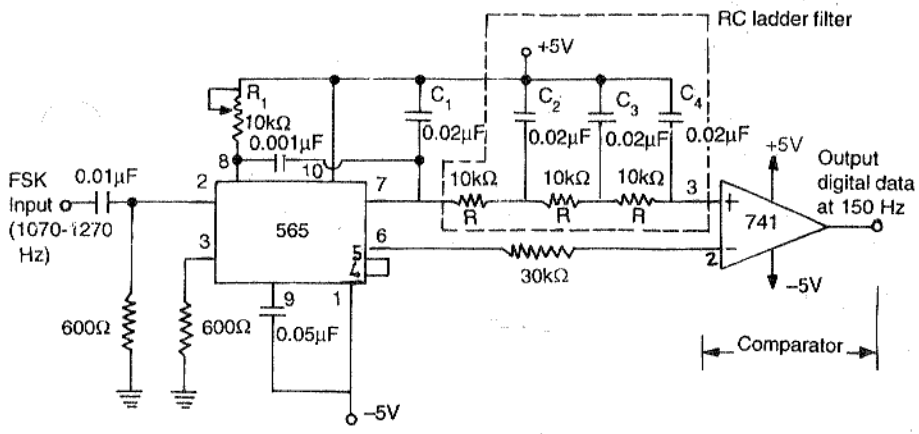


Fig. 9.15 FSK demodulator

Summary

1. A phase locked loop consists of a phase detector, low pass filter, amplifier and a VCO in feedback loop.
2. The important characteristics of a PLL are: lock-in range, capture range and pull-in-time.
3. The lock range is usually greater than the capture range. The capture range depends upon the LPF characteristics.
4. The phase detectors are of two types: analog and digital. The phase detector is basically a multiplier.
5. The frequency of VCO can be set by an external capacitor and resistor. The output frequency f_0 of VCO is compared with the incoming signal f_s. When $f_0 = f_s$ the PLL is said to be locked.
6. The low pass filter may be passive or active type. The LPF controls the capture range and lock range of PLL.
7. Signetics SE/NE 560 series – 560, 561, 562, 564, 565 and 567 are monolithic PLLs. All the blocks of a PLL are also available as independent ICs and can be interconnected to make a PLL.
8. The PLLs are used as frequency multiplier, divider, AM and FM demodulator, FSK demodulator etc.

Review Questions

9.1. List the basic building blocks of a PLL.
9.2. Define capture range, lock range and pull-in-time.
9.3. Which is greater 'Capture range' or 'Lock range'?
9.4. What is the major difference between digital and analog PLLs?
9.5. Give the block diagram of IC 566 VCO and explain its operation.
9.6. What is the range of modulating input voltage applied to a VCO?
9.7. List the applications of PLL.
9.8. Draw the circuit of a PLL AM detector and explain its operation.

PROBLEMS

9.1. In the VCO of Fig. 9.7 calculate the change in output frequency if the supply voltage is varied between 9V and 11V. Assume V_{cc} = 12V, R_T = 6.8 kΩ, C_T = 75 pF, R_1 = 15 kΩ and R_2 = 100 kΩ.

9.2. Determine the dc control voltage v_c at lock if signal frequency f_s = 10 kHz, VCO free running frequency is 10.66 kHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/V.

9.3. If f_s = 100 kHz, the voltage to frequency transfer coefficient of VCO, K_v = 2 MHz/V, f_0 the VCO frequency is 5 MHz and N = 100 in the frequency multiplier of Fig. 9.12, what is the dc control voltage at lock?

9.4. Calculate output frequency f_0, lock range Δf_L and capture range Δf_c of a 565 PLL if R_T = 10 kΩ, C_T = 0.01 μF and C = 10 μF.

9.5. Repeat Problems 9.4 for C_T = 470 pF.

Experiment

(a) To study the operation of NE 565 PLL.
(b) To use NE 565 as a multiplier.

Procedure

1. Make connections of the PLL as shown in Fig. E. 9.1 (a).
2. Measure the free running frequency of VCO at pin 4, with the input signal V_{in} set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$.
3. Now apply the input signal of 1 V_{pp} square wave at a 1 kHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.

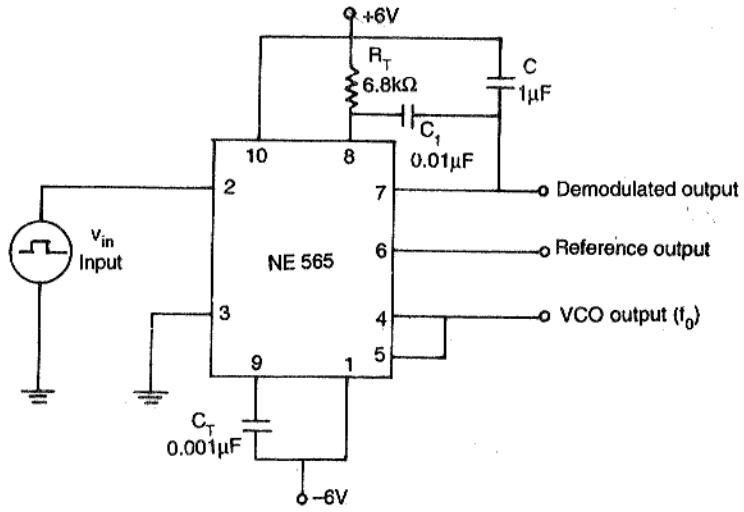


Fig. E. 9.1 (a) NE565 PLL connection diagram

4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f_2. This frequency f_2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range.
6. The lock range $\Delta f_L = (f_2 - f_4)$. Compare it with the calculated value of $\frac{\pm 7.8\, f_0}{12}$. Also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value of capture range.

$$\Delta f_c = \pm\left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3) \times C}\right]^{\frac{1}{2}}$$

7. To use PLL as a multiplier, make connections as shown in Fig. E. 9.1(b). The circuit uses a 4-bit binary counter 7490 used as a divide-by-5 circuit

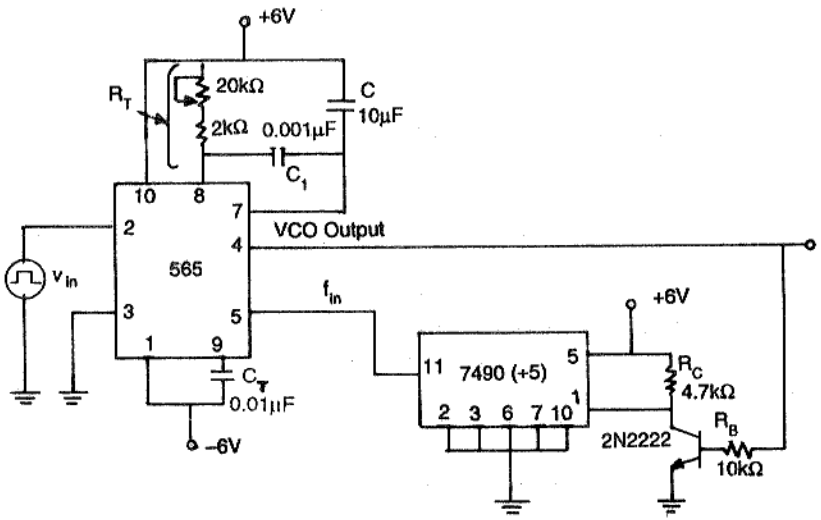


Fig. E. 9.1 (b) NE 565 as a frequency multiplier

8. Set the input signal at 1 V_{pp} square wave at 500 Hz.
9. Vary the VCO frequency by adjusting the 20 kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
10. Repeat steps 8, 9 for input frequency of 1 kHz and 1.5 kHz.

10

D-A And A-D Converters

10.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superimposition of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variable in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 10.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

The scheme given in Fig. 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data

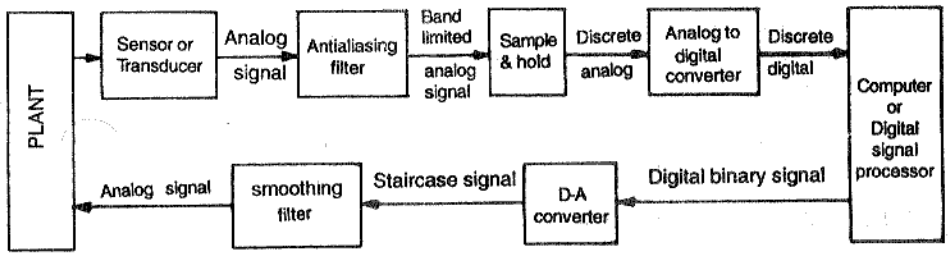


Fig. 10.1 Circuit showing application of A/D and D/A converter

acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

10.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 10.2. The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K\ V_{FS}\ (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad (10.1)$$

where, V_o = output voltage
V_{FS} = full scale output voltage
K = scaling factor usually adjusted to unity
$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left
d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$
d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

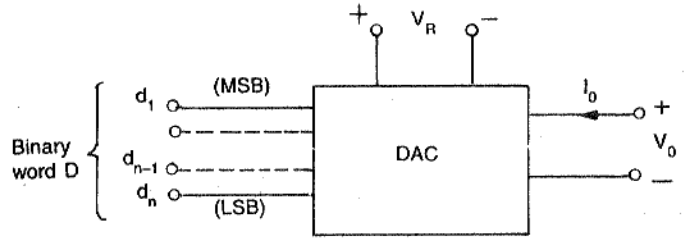


Fig. 10.2 Schematic of a DAC

There are various ways to implement Eq. (10.1) Here we shall discuss the following resistive techniques only:

Weighted resistor DAC
R-2R ladder
Inverted R-2R ladder

10.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 10.3(a) uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 10.3(a), the output current I_0 for an ideal op-amp can be written as

$$I_0 = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_0 = I_0 R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad (10.2)$$

Comparing Eq. (10.1) with Eq. (10.2) it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 10.3(a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 10.3(b) for a 3-bit weighted resistor DAC. It may be noted that

(i) Although the op-amp in Fig. 10.3(a) is connected in inverting mode, it can also be connected in non-inverting mode.
(ii) The op-amp is simply working as a current to voltage converter.
(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be + 5 V and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as

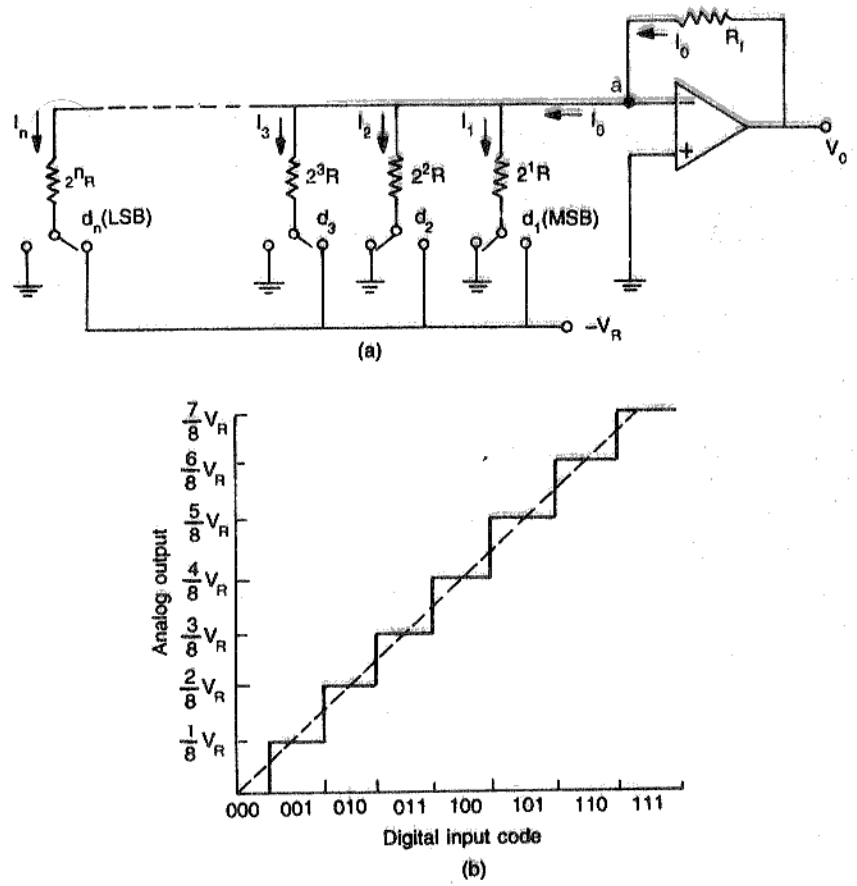


Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are 2^0R, 2^1R, 2^2R, ..., 2^7R. The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5 kΩ. The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as 2.5 kΩ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 10.3 (a) are in series with resistors and therefore, their ***on*** resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

Different types of digitally controlled SPDT electronic switches are available of which two are shown in Fig. 10.4. A totem-pole MOSFET driver in Fig. 10.4(a) feeds each resistor connected to the inverting input terminal 'a' of Fig. 10.3(a). The two complementary gate inputs Q and $\overline{Q}$ come from MOSFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i.e. logic '1' corresponds to -10 V and logic '0' corresponds to zero volt. If there is '1' in the bit line, $S = 1$ and $R = 0$ so that $Q = 1$ and $\overline{Q} = 0$. This drives the transistor Q_1 ***on***, thus connecting the resistor R_1 to the reference voltage $-V_R$ whereas the transistor Q_2 remains ***off***. Similarly a '0' at the bit line connects the resistor R_1 to the ground terminal.

Another SPDT switch of Fig. 10.4(b) consists of CMOS inverter feeding an op-amp voltage follower which drives R_1 from a very low output resistance. The circuit is using a positive logic with $V(1) = V_R = +5$ V and $V(0) = 0$ V. The complement $\overline{Q}$ of the bit under consideration is applied at the input. Thus $\overline{Q} = 0$ makes transistor Q_1 ***off*** and Q_2 ***on***. The output of the CMOS inverter is at logic 1, that is, 5 V is applied to resistor R_1 through the voltage follower. And if $\overline{Q} = 1$ the output of the CMOS inverter is 0V connecting the resistance R_1 to ground.

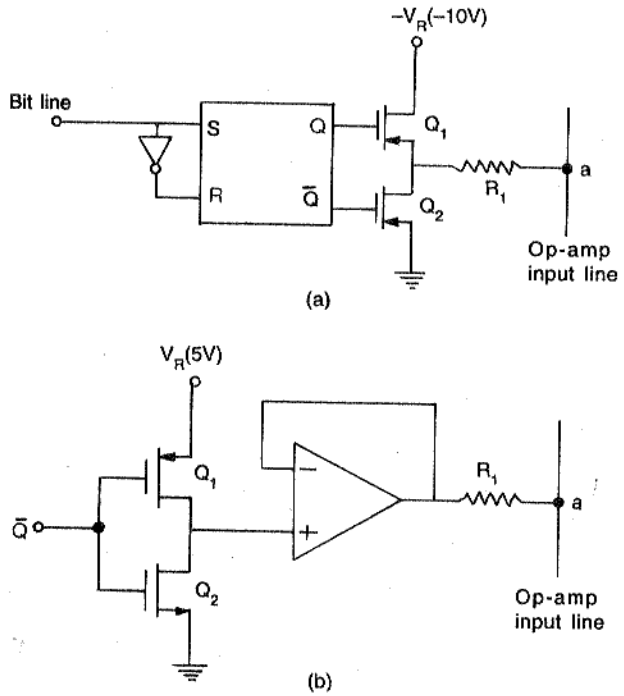


Fig. 10.4 (a) A totem pole MOSFET switch (b) CMOS inverter as switch

10.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 10.5 (a), where the switch position $d_1\, d_2\, d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 10.5 (b) and finally to Fig. 10.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}$$

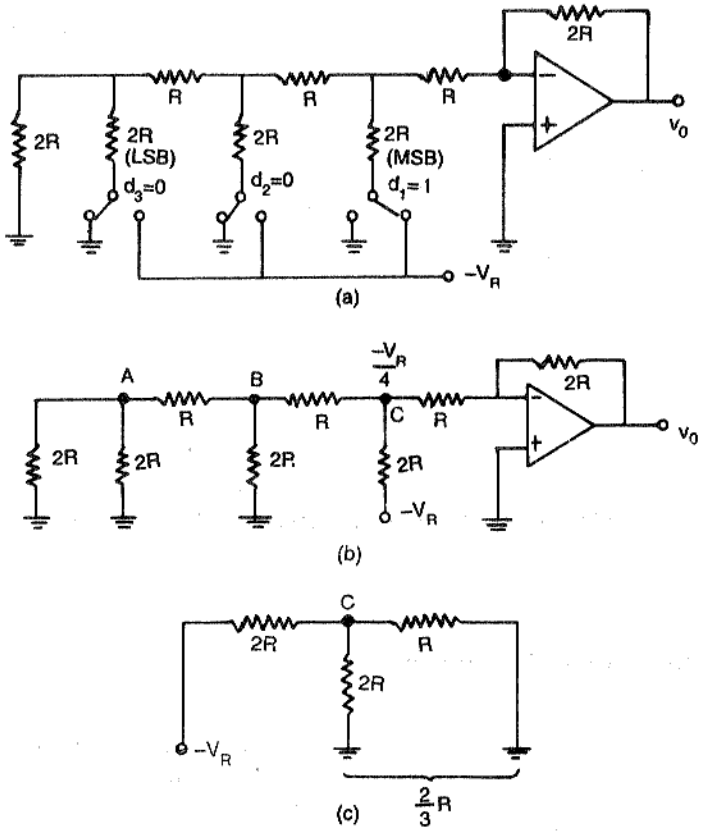


Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The output voltage

$$V_0 = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 10.6 (a). The circuit can be simplified to the equivalent form of Fig. 10.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_0 = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

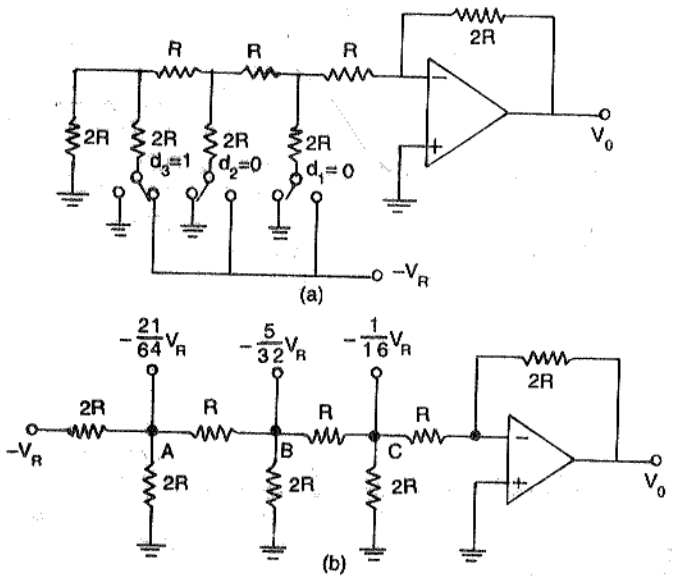


Fig. 10.6 (a) R-2R ladder DAC for switch positions 001 (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

10.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 10.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of

switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 10.7 (a), when switch d_i is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch d_i is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the currents divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig. 10.7 (b). Consider a reference current of 2 mA. Just to the right of node *A*, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node *A*. Similarly to the right of node *B*, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node *B*. Similarly, current divides equally at node *C* to 0.25 mA. The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 10.7(a) are the SPDT switches discussed earlier. According to bit d_i, the corresponding switch gets connected either to ground for $d_i = 0$ or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for $d_i = 1$ and from ground to $-V_R$ for $d_i = 0$. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 10.7(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 10.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

10.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage V_R is called a multiplying D/A converter (MDAC). Thus if in the Eq. (10.1), the reference voltage v_R is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

Then, $$v_0(t) = V_{om} \cos (2\pi f t + 180°)$$

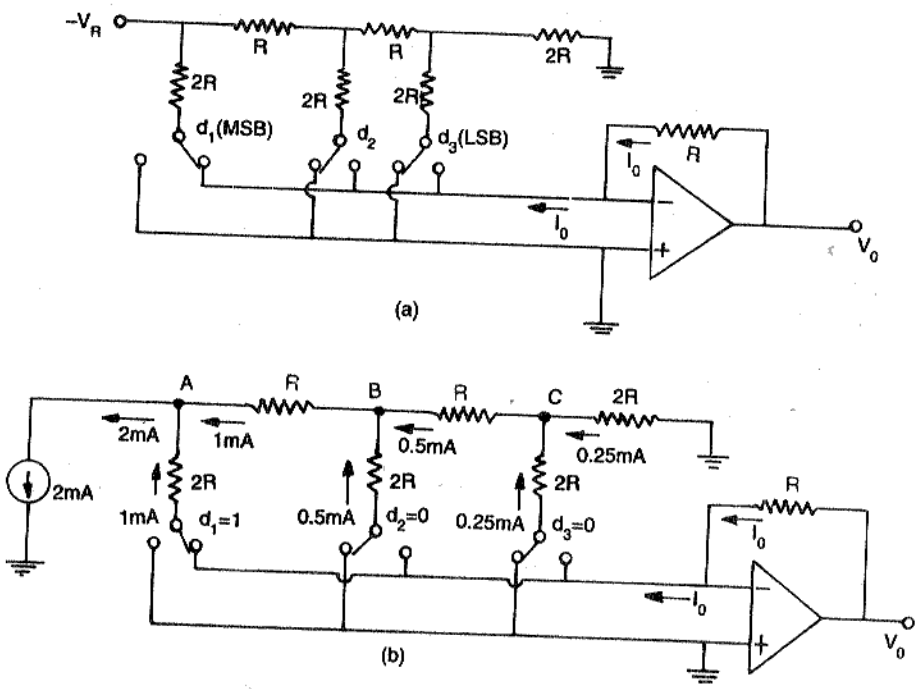


Fig. 10.7 (a) Inverted R-2R ladder DAC (b) Inverted R-2R ladder DAC showing division of current for digital input word 001

where V_{om} will vary from 0V to $(1-2^{-n})$ V_{im} depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output V_o is a fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

10.2.5 Monolithic DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 10.8 (a). It has eight input data lines d_1 (MSB) through d_8 (LSB). It requires 2 mA reference current for full scale input and two power supplies V_{cc} = + 5 V and V_{EE} – 5 V (V_{EE} can range from – 5 V to –15 V). The total reference current

source is determined by resistor R_{14} and voltage reference V_R and is equal to V_R/R_{14} = 5V/2.5 kΩ = 2 mA. The resistor $R_{15} = R_{14}$ match the input impedance of the reference source. The output current I_o is calculated as

$$I_o = \frac{V_R}{R_{14}}\left(\sum_{i=1}^{8} d_i\, 2^{-i}\right); d_i = 0 \text{ or } 1$$

For full scale input (i.e. d_8 through d_1 = 1)

$$I_o = \frac{5\text{ V}}{2.5\text{ k}\Omega}\left(\sum_{i=1}^{8} 1\times 2^{-i}\right) = 2\text{ mA } (255/256) = 1.992\text{ mA}$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage V_o for the full scale input is

$$V_o = 2\text{ mA } (255/256) \times 5\text{ k}\Omega = 9.961\text{ V}$$

In general the output voltage V_o is given by

$$V_o = \frac{V_R}{R_{14}} R_f\left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \ldots + \frac{d_8}{256}\right]$$

The 1408 DAC can be calibrated for bipolar range from – 5 V to + 5 V by adding resistor R_B (5 kΩ) between V_R and output pin 4 as shown in Fig. 10.8 (b). The resistor R_B supplies 1 mA (= V_R/R_B) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation I_o' is

$$I_o' = I_o - (V_R/R_B) = (V_R/R_{14})\left(\sum_{i=1}^{8} d_i 2^{-i}\right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

$$V_o = I_o' R_f = (I_o - V_R/R_B)R_f = (0 - 5\text{ V}/5\text{ k}\Omega) \times 5\text{ k}\Omega = -5\text{ V}$$

For binary input word = 10000000 output V_o becomes

$$\begin{aligned} V_o &= (I_o - V_R/R_B)R_f = [V_R/R_{14})\ (d_1/2) - (V_R/R_B)]R_f \\ &= [(5\text{ V}/2.5\text{ k}\Omega)\ (1/2) - (5\text{ V}/5\text{ k}\Omega)]\ 5\text{ k}\Omega \\ &= (1\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega = 0\text{V} \end{aligned}$$

For binary input word = 11111111 output V_o becomes

$$\begin{aligned} V_o &= [(V_R/R_{14})\ (255/256) - (V_R/R_B)]R_f = (1.992\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega \\ &= 0.992\text{ mA} \times 5\text{ k}\Omega = +4.960\text{ V} \end{aligned}$$

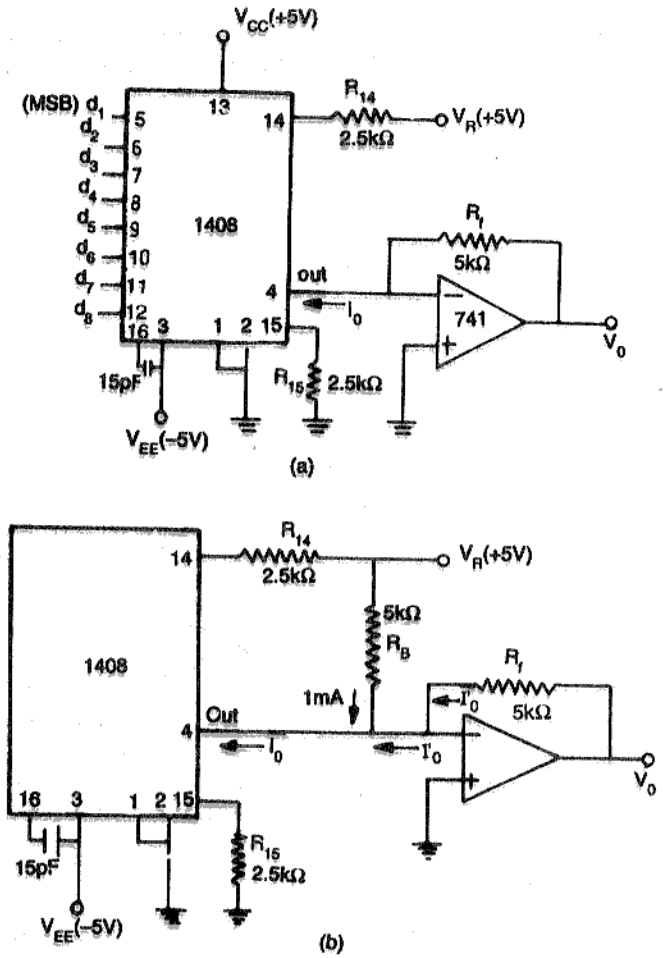


Fig. 10.8 1408 D/A converter (a) Voltage output in unipolar range (b) Modified circuit for bipolar output

Example 10.1

The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111?

Solution

The output voltage for input 101101111 is

$$= 10.3 \text{ mV } (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$$
$$= 10.3 \text{ mV } (367)$$
$$= 3.78 \text{ V}$$

n-th harmonic of the input signal without connecting any frequency divider in between. However, as the amplitude of the higher order harmonics becomes less, effective locking may not take place for high values of n. Typically n is kept less than 10.

The circuit of Fig. 9.12 can also be used for frequency division. Since the VCO output (a square wave) is rich in harmonics, it is possible to lock the m-th harmonic of the VCO output with the input signal f_s. The output f_o of VCO is now given by

$$f_o = \frac{f_s}{m} \tag{9.43}$$

9.7.2 Frequency Translation

A schematic for shifting the frequency of an oscillator by a small factor is shown in Fig. 9.13. It can be seen that a mixer (or multiplier) and a low-pass filter are connected externally to the PLL. The signal f_s which has to be shifted and the output frequency f_o of the VCO are applied as inputs to the mixer. The output of the mixer contains the sum and difference of f_s and f_o. However, the output of LPF contains only the difference signal $(f_o - f_s)$. The translation or offset frequency $f_1 (f_1 << f_s)$ is applied to the phase comparator. When PLL is in locked state,

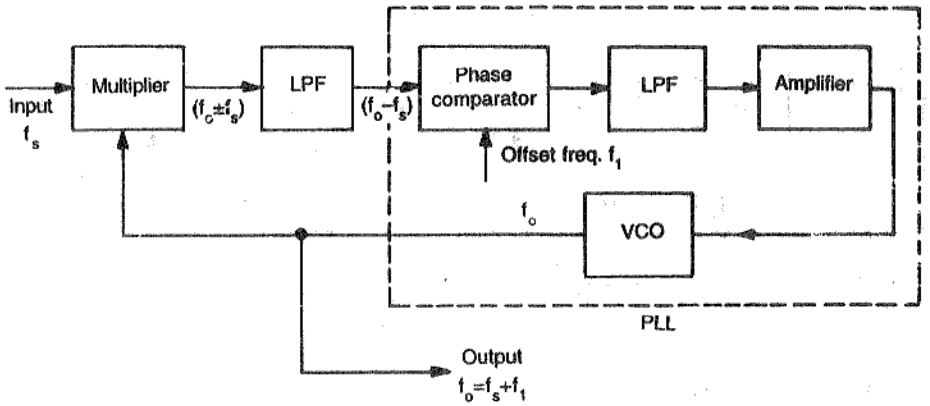


Fig. 9.13 PLL used as a frequency translator

$$f_o - f_s = f_1$$

or

$$f_o = f_s + f_1 \tag{9.44}$$

Thus, it is possible to shift the incoming frequency f_s by f_1.

9.7.3 AM Detection

A PLL may be used to demodulate AM signals as shown in Fig. 9.14. The PLL is locked to the carrier frequency of the incoming AM signal.

The output of VCO which has the same frequency as the carrier, but unmodulated is fed to the multiplier. Since VCO output is always 90° out of phase with the incoming AM signal under the locked condition, the AM input signal is also shifted in phase by 90° before being fed to the multiplier. This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and the difference signals, the demodulated output is obtained after filtering high frequency components by the LPF. Since the PLL responds only to the carrier frequencies which are very close to the VCO output, a PLL AM detector exhibits a high degree of selectivity and noise immunity which is not possible with conventional peak detector type AM modulators.

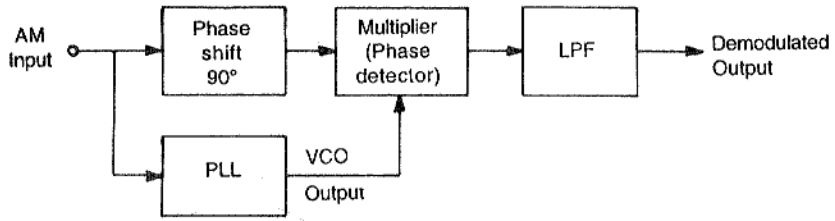


Fig. 9.14 PLL used as AM demodulator

9.7.4 FM Demodulation

If PLL is locked to a FM signal, the VCO tracks the instantaneous frequency of the input signal. The filtered error voltage which controls the VCO and maintains lock with the input signal is the demodulated FM output. The VCO transfer characteristics determine the linearity of the demodulated output. Since, VCO used in IC PLL is highly linear, it is possible to realize highly linear FM demodulators.

9.7.5 Frequency Shift Keying (FSK) Demodulator

In digital data communication and computer peripheral, binary data is transmitted by means of a carrier frequency which is shifted between two preset frequencies. This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using a FSK demodulator at the receiving end. The 565 PLL is very useful as a FSK demodulator. Figure 9.15 shows FSK demodulator using PLL for tele-typewriter signals of 1070 Hz and 1270 Hz. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output. A three stage filter removes the carrier component and the output signal is made logic compatible by a voltage comparator.

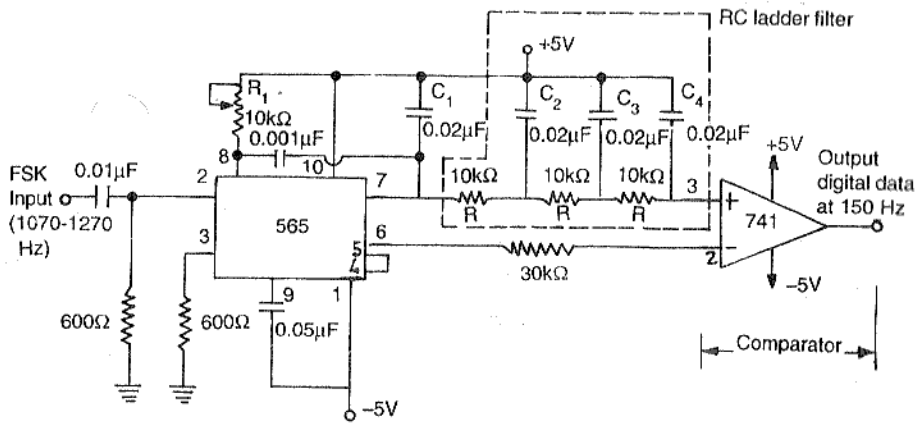


Fig. 9.15 FSK demodulator

Summary

1. A phase locked loop consists of a phase detector, low pass filter, amplifier and a VCO in feedback loop.
2. The important characteristics of a PLL are: lock-in range, capture range and pull-in-time.
3. The lock range is usually greater than the capture range. The capture range depends upon the LPF characteristics.
4. The phase detectors are of two types: analog and digital. The phase detector is basically a multiplier.
5. The frequency of VCO can be set by an external capacitor and resistor. The output frequency f_o of VCO is compared with the incoming signal f_s. When $f_o = f_s$ the PLL is said to be locked.
6. The low pass filter may be passive or active type. The LPF controls the capture range and lock range of PLL.
7. Signetics SE/NE 560 series – 560, 561, 562, 564, 565 and 567 are monolithic PLLs. All the blocks of a PLL are also available as independent ICs and can be interconnected to make a PLL.
8. The PLLs are used as frequency multiplier, divider, AM and FM demodulator, FSK demodulator etc.

Review Questions

9.1. List the basic building blocks of a PLL.
9.2. Define capture range, lock range and pull-in-time.
9.3. Which is greater 'Capture range' or 'Lock range'?
9.4. What is the major difference between digital and analog PLLs?
9.5. Give the block diagram of IC 566 VCO and explain its operation.
9.6. What is the range of modulating input voltage applied to a VCO?
9.7. List the applications of PLL.
9.8. Draw the circuit of a PLL AM detector and explain its operation.

PROBLEMS

9.1. In the VCO of Fig. 9.7 calculate the change in output frequency if the supply voltage is varied between 9V and 11V. Assume V_{cc} = 12V, R_T = 6.8 kΩ, C_T = 75 pF, R_1 = 15 kΩ and R_2 = 100 kΩ.

9.2. Determine the dc control voltage v_c at lock if signal frequency f_s = 10 kHz, VCO free running frequency is 10.66 kHz and the voltage to frequency transfer coefficient of VCO is 6600 Hz/V.

9.3. If f_s = 100 kHz, the voltage to frequency transfer coefficient of VCO, K_v = 2 MHz/V, f_o the VCO frequency is 5 MHz and N = 100 in the frequency multiplier of Fig. 9.12, what is the dc control voltage at lock?

9.4. Calculate output frequency f_o, lock range Δf_L and capture range Δf_c of a 565 PLL if R_T = 10 kΩ, C_T = 0.01 μF and C = 10 μF.

9.5. Repeat Problems 9.4 for C_T = 470 pF.

Experiment

(a) To study the operation of NE 565 PLL.
(b) To use NE 565 as a multiplier.

Procedure

1. Make connections of the PLL as shown in Fig. E. 9.1 (a).
2. Measure the free running frequency of VCO at pin 4, with the input signal V_{in} set equal to zero. Compare it with the calculated value = $0.25/R_TC_T$.
3. Now apply the input signal of 1 V_{pp} square wave at a 1 kHz to pin 2. Connect one channel of the scope to pin 2 and display this signal on the scope.

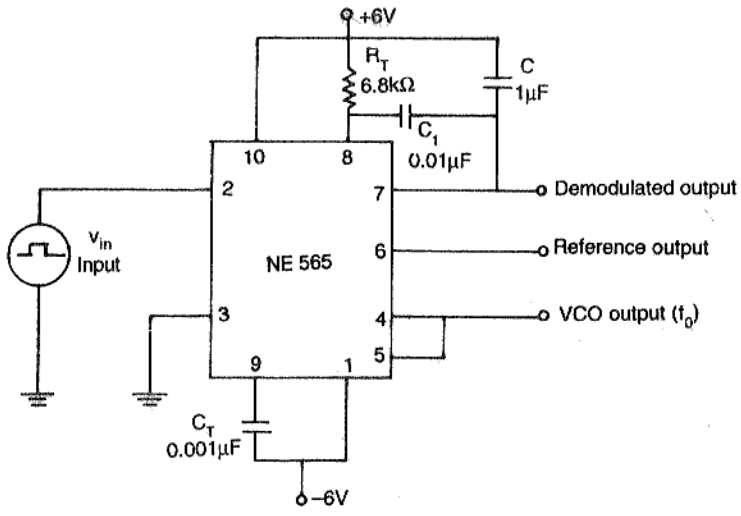


Fig. E. 9.1 (a) NE565 PLL connection diagram

4. Gradually increase the input frequency till the PLL is locked to the input frequency. This frequency f_1 gives the lower end of the capture range. Go on increasing the input frequency, till PLL tracks the input signal, say, to a frequency f_2. This frequency f_2 gives the upper end of the lock range. If input frequency is increased further, the loop will get unlocked.
5. Now gradually decrease the input frequency till the PLL is again locked. This is the frequency f_3, the upper end of the capture range. Keep on decreasing the input frequency until the loop is unlocked. This frequency f_4 gives the lower end of the lock range.
6. The lock range $\Delta f_L = (f_2 - f_4)$. Compare it with the calculated value of $\frac{\pm 7.8 f_0}{12}$. Also the capture range is $\Delta f_c = (f_3 - f_1)$. Compare it with the calculated value of capture range.

$$\Delta f_c = \pm \left[\frac{\Delta f_L}{(2\pi)(3.6)(10^3) \times C} \right]^{\frac{1}{2}}$$

7. To use PLL as a multiplier, make connections as shown in Fig. E. 9.1(b). The circuit uses a 4-bit binary counter 7490 used as a divide-by-5 circuit

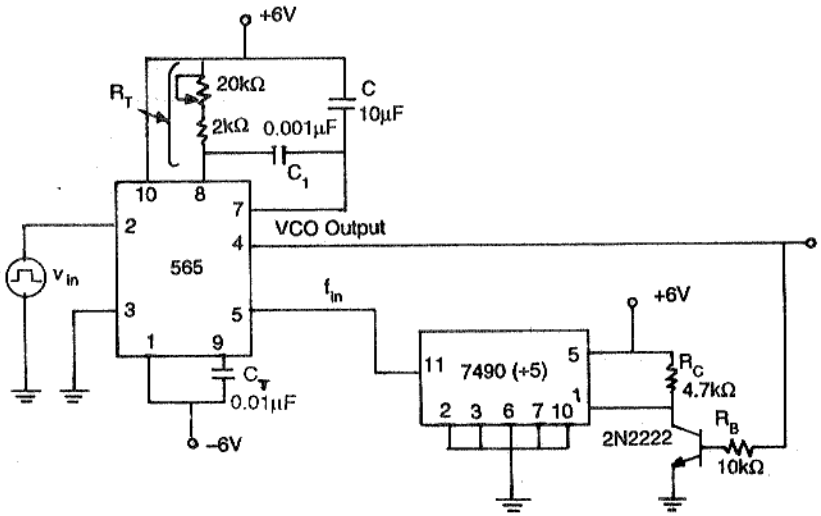


Fig. E. 9.1 (b) NE 565 as a frequency multiplier

8. Set the input signal at 1 V_{pp} square wave at 500 Hz.
9. Vary the VCO frequency by adjusting the 20 kΩ potentiometer till the PLL is locked. Measure the output frequency. It should be 5 times the input frequency.
10. Repeat steps 8, 9 for input frequency of 1 kHz and 1.5 kHz.

10

D-A And A-D Converters

10.1 INTRODUCTION

Most of the real-world physical quantities such as voltage, current, temperature, pressure and time etc. are available in analog form. Even though an analog signal represents a real physical parameter with accuracy, it is difficult to process, store or transmit the analog signal without introducing considerable error because of the superimposition of noise as in the case of amplitude modulation. Therefore, for processing, transmission and storage purposes, it is often convenient to express these variable in digital form. It gives better accuracy and reduces noise. The operation of any digital communication system is based upon analog to digital (A/D) and digital to analog (D/A) conversion.

Figure 10.1 highlights a typical application within which A/D and D/A conversion is used. The analog signal obtained from the transducer is band limited by antialiasing filter. The signal is then sampled at a frequency rate more than twice the maximum frequency of the band limited signal. The sampled signal has to be held constant while conversion is taking place in A/D converter. This requires that ADC should be preceded by a sample and hold (S/H) circuit. The ADC output is a sequence in binary digit. The micro-computer or digital signal processor performs the numerical calculations of the desired control algorithm. The D/A converter is to convert digital signal into analog and hence the function of DAC is exactly opposite to that of ADC. The D/A converter is usually operated at the same frequency as the ADC. The output of a D/A converter is commonly a staircase. This staircase-like digital output is passed through a smoothing filter to reduce the effect of quantization noise.

The scheme given in Fig. 10.1 is used either in full or in part in applications such as digital audio recording and playback, computer, music and video synthesis, pulse code modulation transmission, data

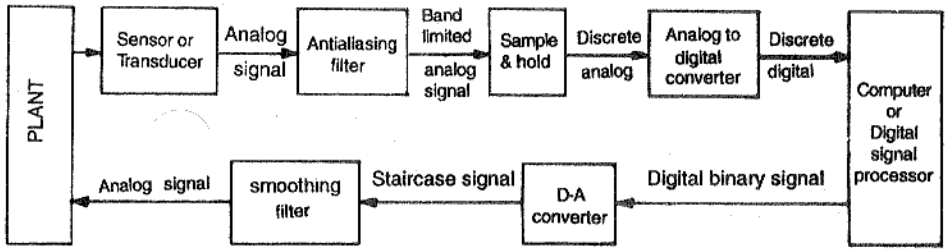


Fig. 10.1 Circuit showing application of A/D and D/A converter

acquisition, digital multimeter, direct digital control, digital signal processing, microprocessor based instrumentation.

Both ADC and DAC are also known as data converters and are available in IC form. It may be mentioned here that for slowly varying signal, sometimes sample and hold circuit may be avoided without considerable error. The A-D conversion usually makes use of a D-A converter so we shall first discuss DAC followed by ADC.

10.2 BASIC DAC TECHNIQUES

The schematic of a DAC is shown in Fig. 10.2. The input is an n-bit binary word D and is combined with a reference voltage V_R to give an analog output signal. The output of a DAC can be either a voltage or current. For a voltage output DAC, the D/A converter is mathematically described as

$$V_o = K\ V_{FS}\ (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad (10.1)$$

where, V_o = output voltage
V_{FS} = full scale output voltage
K = scaling factor usually adjusted to unity
$d_1 d_2 \ldots d_n$ = n-bit binary fractional word with the decimal point located at the left
d_1 = most significant bit (MSB) with a weight of $V_{FS}/2$
d_n = least significant bit (LSB) with a weight of $V_{FS}/2^n$

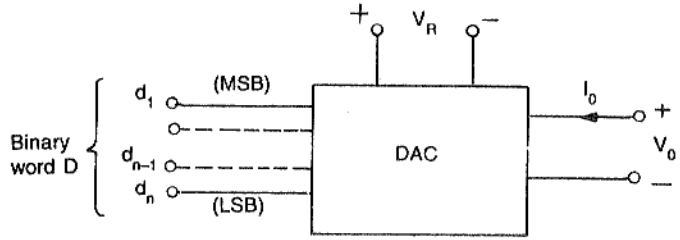


Fig. 10.2 Schematic of a DAC

There are various ways to implement Eq. (10.1) Here we shall discuss the following resistive techniques only:

Weighted resistor DAC
R-2R ladder
Inverted R-2R ladder

10.2.1 Weighted Resistor DAC

One of the simplest circuits shown in Fig. 10.3(a) uses a summing amplifier with a binary weighted resistor network. It has n-electronic switches $d_1, d_2, \ldots, d_n$ controlled by binary input word. These switches are single pole double throw (SPDT) type. If the binary input to a particular switch is 1, it connects the resistance to the reference voltage ($-V_R$). And if the input bit is 0, the switch connects the resistor to the ground. From Fig. 10.3(a), the output current I_0 for an ideal op-amp can be written as

$$I_0 = I_1 + I_2 + \ldots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \ldots + \frac{V_R}{2^n R} d_n$$

$$= \frac{V_R}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n})$$

The output voltage

$$V_0 = I_0 R_f = V_R \frac{R_f}{R} (d_1 2^{-1} + d_2 2^{-2} + \ldots + d_n 2^{-n}) \qquad (10.2)$$

Comparing Eq. (10.1) with Eq. (10.2) it can be seen that if $R_f = R$ then $K = 1$ and $V_{FS} = V_R$.

The circuit shown in Fig. 10.3(a) uses a negative reference voltage. The analog output voltage is therefore positive staircase as shown in Fig. 10.3(b) for a 3-bit weighted resistor DAC. It may be noted that

(i) Although the op-amp in Fig. 10.3(a) is connected in inverting mode, it can also be connected in non-inverting mode.
(ii) The op-amp is simply working as a current to voltage converter.
(iii) The polarity of the reference voltage is chosen in accordance with the type of the switch used. For example, for TTL compatible switches, the reference voltage should be + 5 V and the output will be negative.

The accuracy and stability of a DAC depends upon the accuracy of the resistors and the tracking of each other with temperature. There are however a number of problems associated with this type of DAC. One of the disadvantages of binary weighted type DAC is the wide range of resistor values required. It may be observed that for better resolution, the input binary word length has to be increased. Thus, as

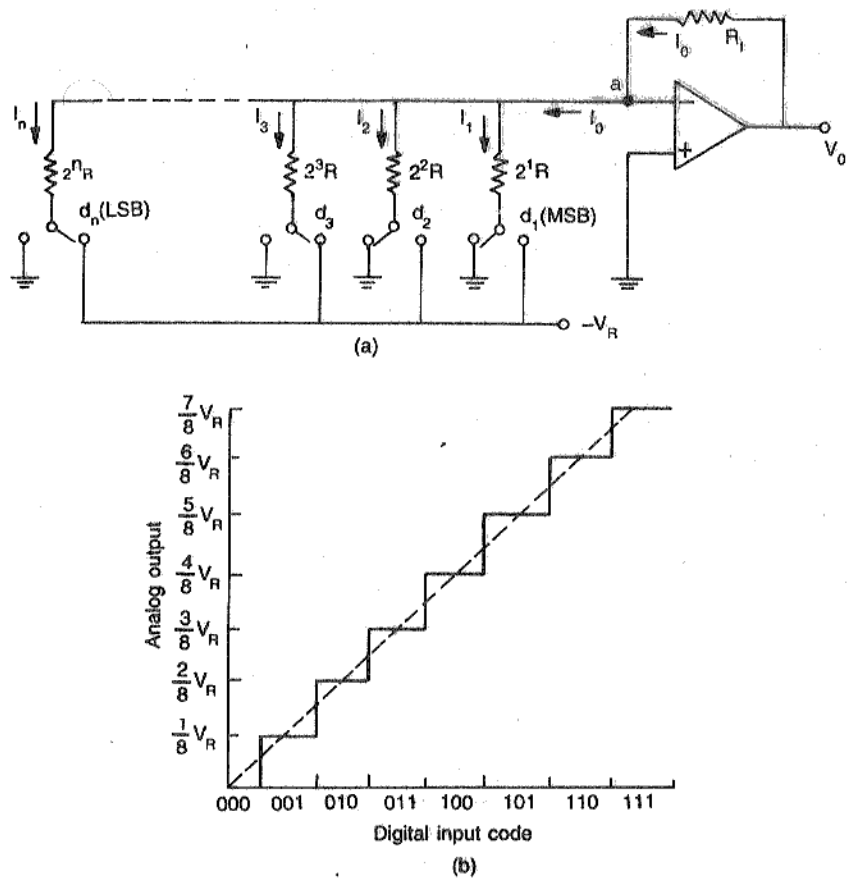


Fig. 10.3 (a) A simple weighted resistor DAC (b) Transfer characteristics of a 3-bit DAC

the number of bit increases, the range of resistance value increases. For 8-bit DAC, the resistors required are 2^0R, 2^1R, 2^2R, ..., 2^7R. The largest resistor is 128 times the smallest one for only 8-bit DAC. For a 12-bit DAC, the largest resistance required is 5.12 MΩ if the smallest is 2.5 kΩ. The fabrication of such a large resistance in IC is not practical. Also the voltage drop across such a large resistor due to the bias current would also affect the accuracy. The choice of smallest resistor value as 2.5 kΩ is reasonable; otherwise loading effect will be there. The difficulty of achieving and maintaining accurate ratios over such a wide range especially in monolithic form restricts the use of weighted resistor DACs to below 8-bits.

The switches in Fig. 10.3 (a) are in series with resistors and therefore, their ***on*** resistance must be very low and they should have zero offset voltage. Bipolar transistors do not perform well as voltage switches, due to the inherent offset voltage when in saturation. However, by using MOSFET, this can be achieved.

Different types of digitally controlled SPDT electronic switches are available of which two are shown in Fig. 10.4. A totem-pole MOSFET driver in Fig. 10.4(a) feeds each resistor connected to the inverting input terminal 'a' of Fig. 10.3(a). The two complementary gate inputs Q and $\overline{Q}$ come from MOSFET S-R flip-flop or a binary cell of a register which holds one bit of the digital information to be converted to an analog number. Assume a negative logic, i.e. logic '1' corresponds to -10 V and logic '0' corresponds to zero volt. If there is '1' in the bit line, $S = 1$ and $R = 0$ so that $Q = 1$ and $\overline{Q} = 0$. This drives the transistor Q_1 ***on***, thus connecting the resistor R_1 to the reference voltage $-V_R$ whereas the transistor Q_2 remains ***off***. Similarly a '0' at the bit line connects the resistor R_1 to the ground terminal.

Another SPDT switch of Fig. 10.4(b) consists of CMOS inverter feeding an op-amp voltage follower which drives R_1 from a very low output resistance. The circuit is using a positive logic with $V(1) = V_R = +5$ V and $V(0) = 0$ V. The complement $\overline{Q}$ of the bit under consideration is applied at the input. Thus $\overline{Q} = 0$ makes transistor Q_1 ***off*** and Q_2 ***on***. The output of the CMOS inverter is at logic 1, that is, 5 V is applied to resistor R_1 through the voltage follower. And if $\overline{Q} = 1$ the output of the CMOS inverter is 0V connecting the resistance R_1 to ground.

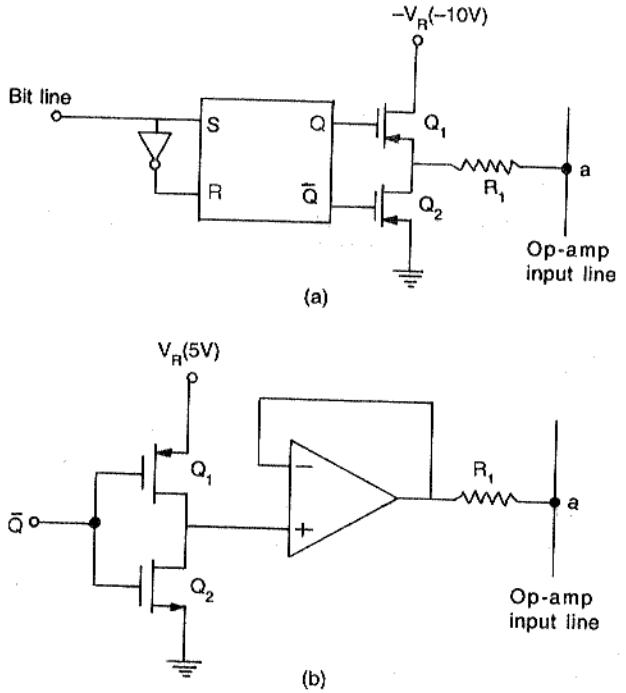


Fig. 10.4 (a) A totem pole MOSFET switch (b) CMOS inverter as switch

10.2.2 R-2R Ladder DAC

Wide range of resistors are required in binary weighted resistor type DAC. This can be avoided by using R-2R ladder type DAC where only two values of resistors are required. It is well suited for integrated circuit realization. The typical value of R ranges from 2.5 kΩ to 10 kΩ.

For simplicity, consider a 3-bit DAC as shown in Fig. 10.5 (a), where the switch position $d_1\ d_2\ d_3$ corresponds to the binary word 100. The circuit can be simplified to the equivalent form of Fig. 10.5 (b) and finally to Fig. 10.5 (c). Then, voltage at node C can be easily calculated by the set procedure of network analysis as

$$\frac{-V_R\left(\frac{2}{3}R\right)}{2R+\frac{2}{3}R} = -\frac{V_R}{4}.$$

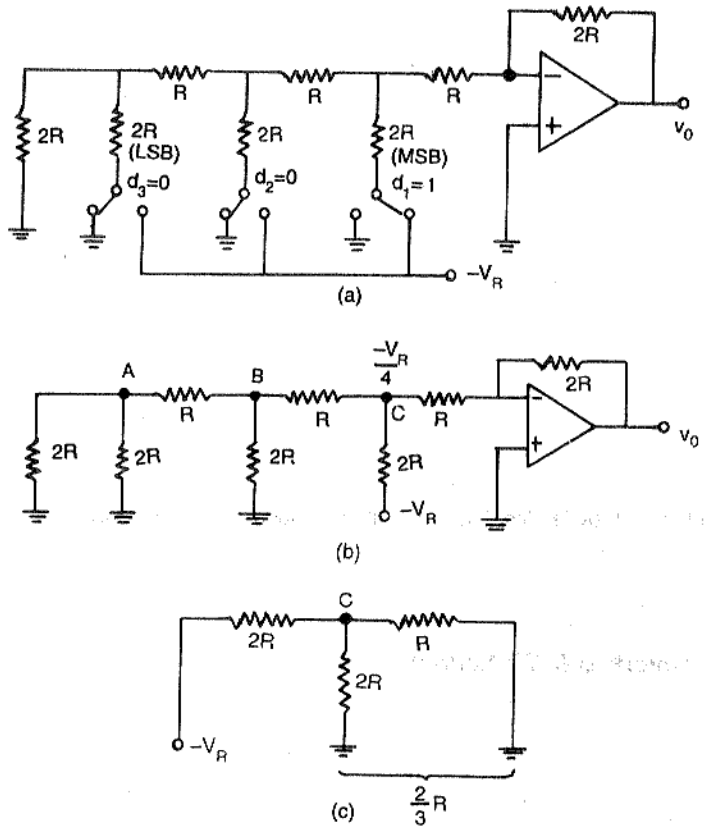


Fig. 10.5 (a) R-2R ladder DAC (b) Equivalent circuit of (a), (c) Equivalent circuit of (b)

The output voltage

$$V_0 = \frac{-2R}{R}\left(-\frac{V_R}{4}\right) = \frac{V_R}{2} = \frac{V_{FS}}{2}$$

The switch position corresponding to the binary word 001 in 3 bit DAC is shown in Fig. 10.6 (a). The circuit can be simplified to the equivalent form of Fig. 10.6 (b). The voltages at the nodes (A, B, C) formed by resistor branches are easily calculated in a similar fashion and the output voltage becomes

$$V_0 = \left(-\frac{2R}{R}\right)\left(-\frac{V_R}{16}\right) = \frac{V_R}{8} = \frac{V_{FS}}{8}$$

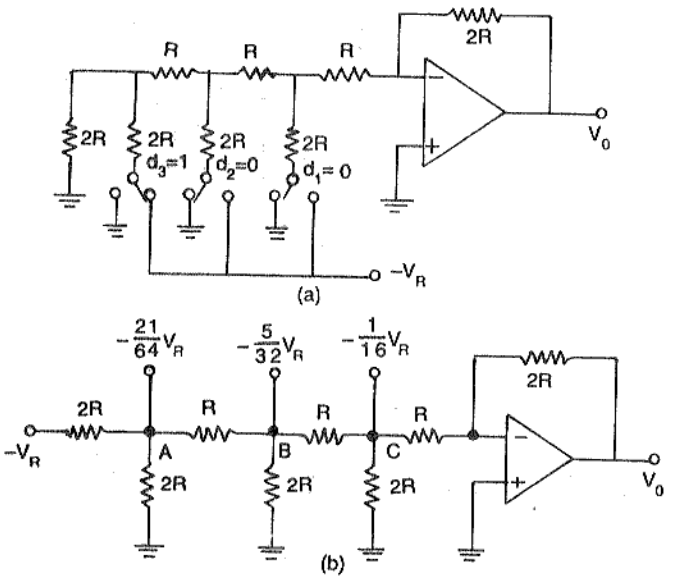


Fig. 10.6 (a) R-2R ladder DAC for switch positions 001 (b) Equivalent circuit

In a similar fashion, the output voltage for R-2R ladder type DAC corresponding to other 3-bit binary words can be calculated.

10.2.3 Inverted R-2R Ladder

In weighted resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as the input data changes. More power dissipation causes heating, which in turn, creates non-linearity in DAC. This is a serious problem and can be avoided completely in 'Inverted R-2R ladder type DAC'. A 3-bit Inverted R-2R ladder type DAC is shown in Fig. 10.7 (a) where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either to ground or to the inverting input terminal of the op-amp which is also at virtual ground. Since both the terminals of

switches d_i are at ground potential, current flowing in the resistances is constant and independent of switch position, i.e. independent of input binary word. In Fig. 10.7 (a), when switch d_i is at logical '0' i.e., to the left, the current through 2R resistor flows to the ground and when the switch d_i is at logical '1' i.e., to the right, the current through 2R sinks to the virtual ground. The circuit has the important property that the currents divides equally at each of the nodes. This is because the equivalent resistance to the right or to the left of any node is exactly 2 R. The division of the current is shown in Fig. 10.7 (b). Consider a reference current of 2 mA. Just to the right of node *A*, the equivalent resistor is 2 R. Thus 2 mA of reference input current divides equally to value 1 mA at node *A*. Similarly to the right of node *B*, the equivalent resistor is 2 R. Thus 1 mA of current further divides to value 0.5 mA at node *B*. Similarly, current divides equally at node *C* to 0.25 mA. The equal division of current in successive nodes remains the same in the 'inverted R-2R ladder' irrespective of the input binary word. Thus the currents remain constant in each branch of the ladder. Since constant current implies constant voltage, the ladder node voltages remain constant at $V_R/2^0$, $V_R/2^1$, $V_R/2^2$. The circuit works on the principle of summing currents and is also said to operate in the current mode. The most important advantage of the current mode or inverted ladder is that since the ladder node voltages remain constant even with changing input binary words (codes), the stray capacitances are not able to produce slow-down effects on the performance of the circuit.

It may be noted that the switches used in Fig. 10.7(a) are the SPDT switches discussed earlier. According to bit d_i, the corresponding switch gets connected either to ground for $d_i = 0$ or to $-V_R$ for $d_i = 1$. The current flows from inverting input terminal to $-V_R$ for $d_i = 1$ and from ground to $-V_R$ for $d_i = 0$. Regardless of the binary input word, the current in the resistive branches of the inverted ladder circuit remains always constant as explained in Fig. 10.7(b). However, the current through the feedback resistor R is the summing current depending upon the input binary word. It may further be mentioned that, Fig. 10.7 (b) shows only the current division for making the analysis simple, though it is a voltage driven DAC.

10.2.4 Multiplying DACs

A digital to analog converter which uses a varying reference voltage V_R is called a multiplying D/A converter (MDAC). Thus if in the Eq. (10.1), the reference voltage v_R is a sine wave given by

$$v_R(t) = V_{im} \cos 2\pi ft$$

Then,

$$v_0(t) = V_{om} \cos (2\pi f\, t + 180°)$$

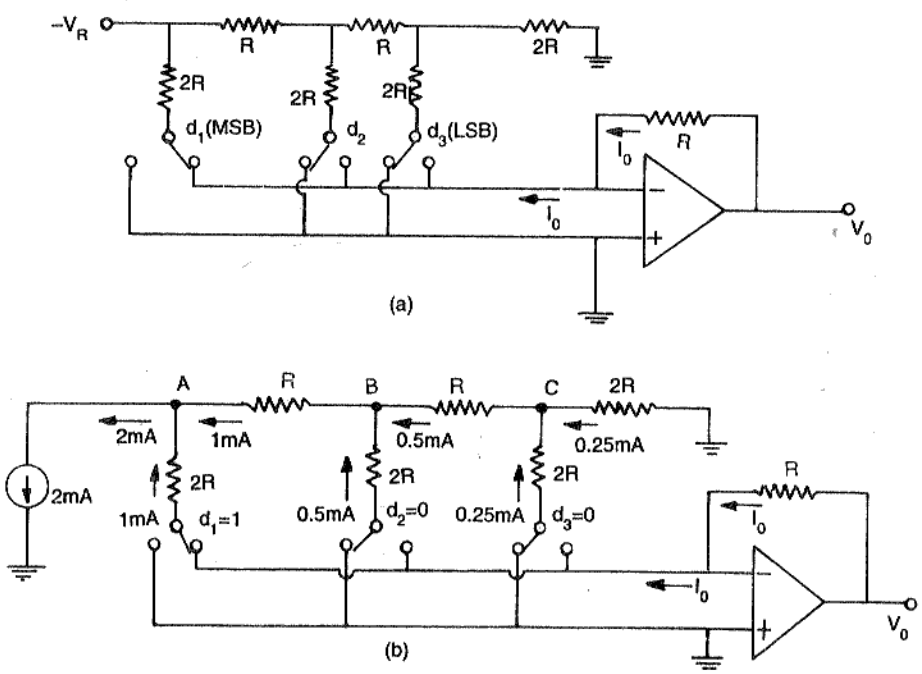


Fig. 10.7 (a) Inverted R-2R ladder DAC (b) Inverted R-2R ladder DAC showing division of current for digital input word 001

where V_{om} will vary from 0V to $(1-2^{-n})\ V_{im}$ depending upon the input code. When used like this, MDAC behaves as a digitally controlled audio attenuator because the output V_o is a fraction of the voltage representing the input digital code and the attenuator setting can be controlled by digital logic. If followed by an op-amp integrator, the MDAC provides digitally programmable integration which can be used in the design of digitally programmable oscillators, filters.

10.2.5 Monolithic DAC

Monolithic DACs consisting of R-2R ladder, switches and the feedback resistor are available for 8, 10, 12, 14 and 16 bit resolution from various manufacturers. The MC 1408L is a 8-bit DAC with a current output. The SE/NE 5018 is also a 8-bit DAC but with a voltage output. There are hybrid D/A converters available in DATEL DAC-HZ series for current as well as voltage output.

A typical 8-bit DAC 1408 compatible with TTL and CMOS logic with settling time around 300 ns is shown in Fig. 10.8 (a). It has eight input data lines d_1 (MSB) through d_8 (LSB). It requires 2 mA reference current for full scale input and two power supplies V_{cc} = + 5 V and V_{EE} – 5 V (V_{EE} can range from – 5 V to –15 V). The total reference current

source is determined by resistor R_{14} and voltage reference V_R and is equal to V_R/R_{14} = 5V/2.5 kΩ = 2 mA. The resistor $R_{15} = R_{14}$ match the input impedance of the reference source. The output current I_o is calculated as

$$I_o = \frac{V_R}{R_{14}}\left(\sum_{i=1}^{8} d_i\, 2^{-i}\right);\ d_i = 0 \text{ or } 1$$

For full scale input (i.e. d_8 through d_1 = 1)

$$I_o = \frac{5\text{ V}}{2.5\text{ k}\Omega}\left(\sum_{i=1}^{8} 1\times 2^{-i}\right) = 2\text{ mA } (255/256) = 1.992\text{ mA}$$

The output is 1 LSB less than the full scale reference current of 2 mA. So, the output voltage V_o for the full scale input is

$$V_o = 2\text{ mA } (255/256) \times 5\text{ k}\Omega = 9.961\text{ V}$$

In general the output voltage V_o is given by

$$V_o = \frac{V_R}{R_{14}} R_f\left[\frac{d_1}{2} + \frac{d_2}{4} + \frac{d_3}{8} + \ldots + \frac{d_8}{256}\right]$$

The 1408 DAC can be calibrated for bipolar range from – 5 V to + 5 V by adding resistor R_B (5 kΩ) between V_R and output pin 4 as shown in Fig. 10.8 (b). The resistor R_B supplies 1 mA (= V_R/R_B) current to the output in the opposite direction of the current generated by the input signal. Therefore the output current for the bipolar operation I_o' is

$$I_o' = I_o - (V_R/R_B) = (V_R/R_{14})\left(\sum_{i=1}^{8} d_i 2^{-i}\right) - (V_R/R_B)$$

For binary input word = 00000000, i.e. zero input, the output becomes,

$$V_o = I_o' R_f = (I_o - V_R/R_B)R_f = (0 - 5\text{ V}/5\text{ k}\Omega) \times 5\text{ k}\Omega = -5\text{ V}$$

For binary input word = 10000000 output V_o becomes

$$\begin{aligned} V_o &= (I_o - V_R/R_B)R_f = [V_R/R_{14})\ (d_1/2) - (V_R/R_B)]R_f \\ &= [(5\text{ V}/2.5\text{ k}\Omega)\ (1/2) - (5\text{ V}/5\text{ k}\Omega)]\ 5\text{ k}\Omega \\ &= (1\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega = 0\text{V} \end{aligned}$$

For binary input word = 11111111 output V_o becomes

$$\begin{aligned} V_o &= [(V_R/R_{14})\ (255/256) - (V_R/R_B)]R_f = (1.992\text{ mA} - 1\text{ mA}) \times 5\text{ k}\Omega \\ &= 0.992\text{ mA} \times 5\text{ k}\Omega = +4.960\text{ V} \end{aligned}$$

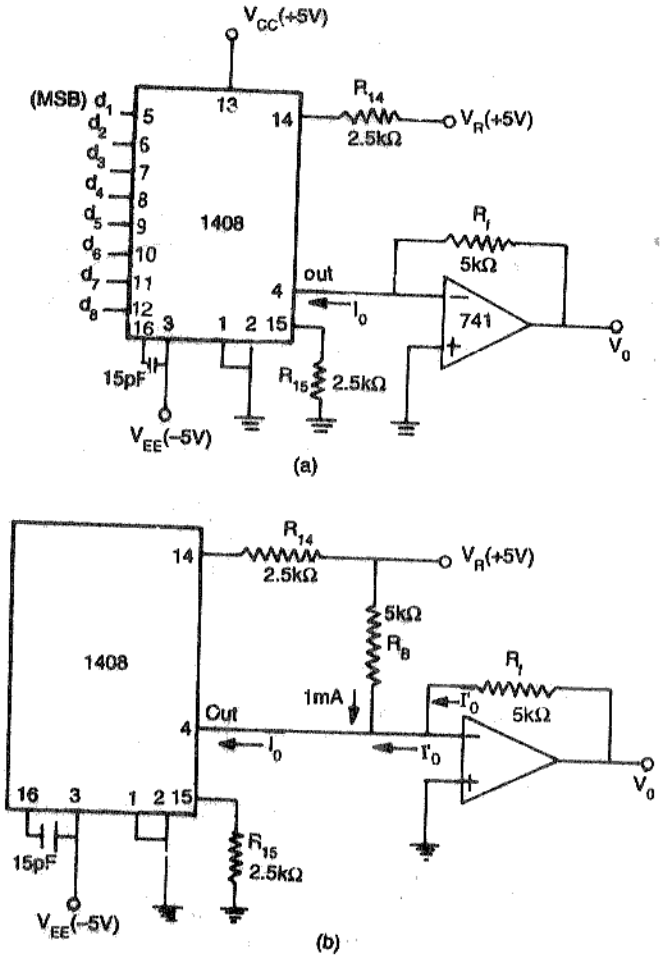


Fig. 10.8 1408 D/A converter (a) Voltage output in unipolar range (b) Modified circuit for bipolar output

Example 10.1

The basic step of a 9-bit DAC is 10.3 mV. If 000000000 represents 0 V, what output is produced if the input is 101101111?

Solution

The output voltage for input 101101111 is

$$= 10.3 \text{ mV } (1 \times 2^8 + 0 \times 2^7 + 1 \times 2^6 + 1 \times 2^5 + 0 \times 2^4 + 1 \times 2^3 + 1 \times 2^2 + 1 \times 2^1 + 1 \times 2^0)$$

$$= 10.3 \text{ mV } (367)$$

$$= 3.78 \text{ V}$$

10.3. If a 10-bit D/A converter spans a range of 0 to 10 V and is always within 1 mV of its ideal output. What is its linearity as a percent of full-scale range?

10.4. Find the voltage at all nodes 0, 1, 2, ... and at the output of a 5-bit R-2R ladder DAC. The least significant bit is 1 and all other bits are equal to 0. Assume $V_R = -10$ V and $R = 10$ kΩ.

10.5. The Fig. P. 10.5 shows a binary weighted resistor D/A converter.

(i) Show that the output resistance is independent of the digital word and that

$$R_o = \frac{2^{N-1}}{2^N - 1} R$$

(ii) Show that the analog output voltage for the MSB is

$$V_o = \frac{2^{N-1}}{2^N - 1} V_R$$

(iii) Show that the analog output voltage for the LSB is

$$V_o = \frac{1}{2^N - 1} V_R$$

10.6. (a) Draw the circuit diagram of a 6-bit inverted R-2R ladder DAC.

(b) For $V(1) = 5$ V, what is the maximum output voltage?

(c) What is the minimum voltage that can be resolved?

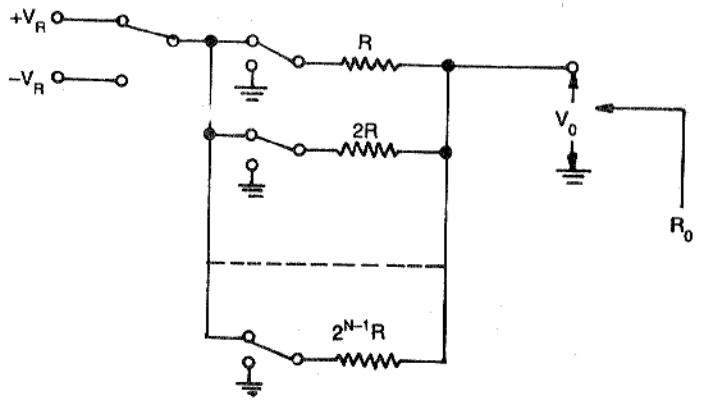


Fig. P. 10.5

10.7. The analog input signal ranges for −5 to +8 V in a nine bit A/D converter.

(i) How many quantization levels are available with this A/D converter?

(ii) What is the resolution in volt per increment?

(iii) What binary number will be produced when the analog input is zero volt?

10.8. A counting A/D converter uses a 7-bit DAC. The MSB of DAC output voltage is + 5V.
(i) If the analog input voltage is + 6.85 V, what will be the R-2R ladder output voltage when the clock stops?
(ii) What is the number of clock pulses that occur between the release of reset and stopping of the clock?

10.9. The ADC in problem 10.8 uses a 100 kHz clock. How long did it take to digitize 6.85V?

10.10. What is the conversion time of a 10-bit successive approximation A/D converter if its input clock is 5 MHz.

10.11. A dual slope ADC uses a 18-bit counter with a 5 MHz clock. The maximum input voltage is +12 V and the maximum integrator output voltage at 2^N count is – 10 V. If R = 100 kΩ, find the size of the capacitor to be used for integrator.

10.12. The dual slope ADC of problem 10.11 has an input voltage of + 5.237V. Determine the digital number in binary which represents the count in the register.

Experiment 10.1

To construct a 4-bit R-2R ladder type D/A converter. Plot the transfer characteristics, that is, binary input vs output voltage. Calculate the resolution and linearity of the converter from the graph.

(i) Choose R = 10 kΩ, 2R = 20 kΩ of tolerance ± 1% or less.
(ii) For logic '0' short to ground and logic '1' connect to a + 5V supply.

Procedure

1. Set up the circuit shown in Fig. E. 10.1.
2. With all inputs (d_0 to d_3) shorted to ground, adjust the 20 kΩ-pot until the output is 0V. This will nullify any offset voltage at the input of the op-amp.

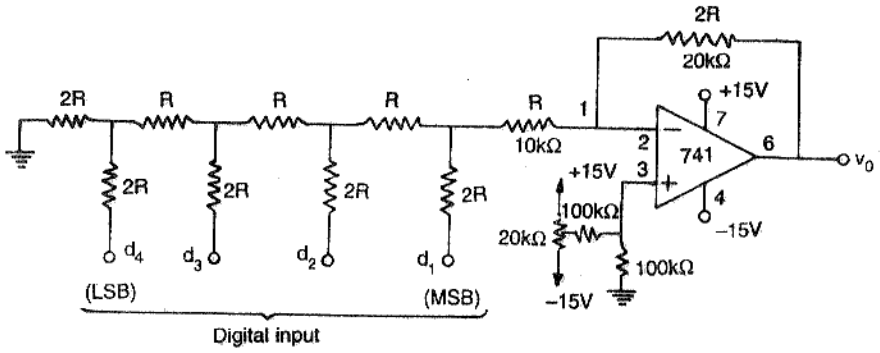


Fig. E. 10.1 A 4-bit R-2R ladder D/A converter

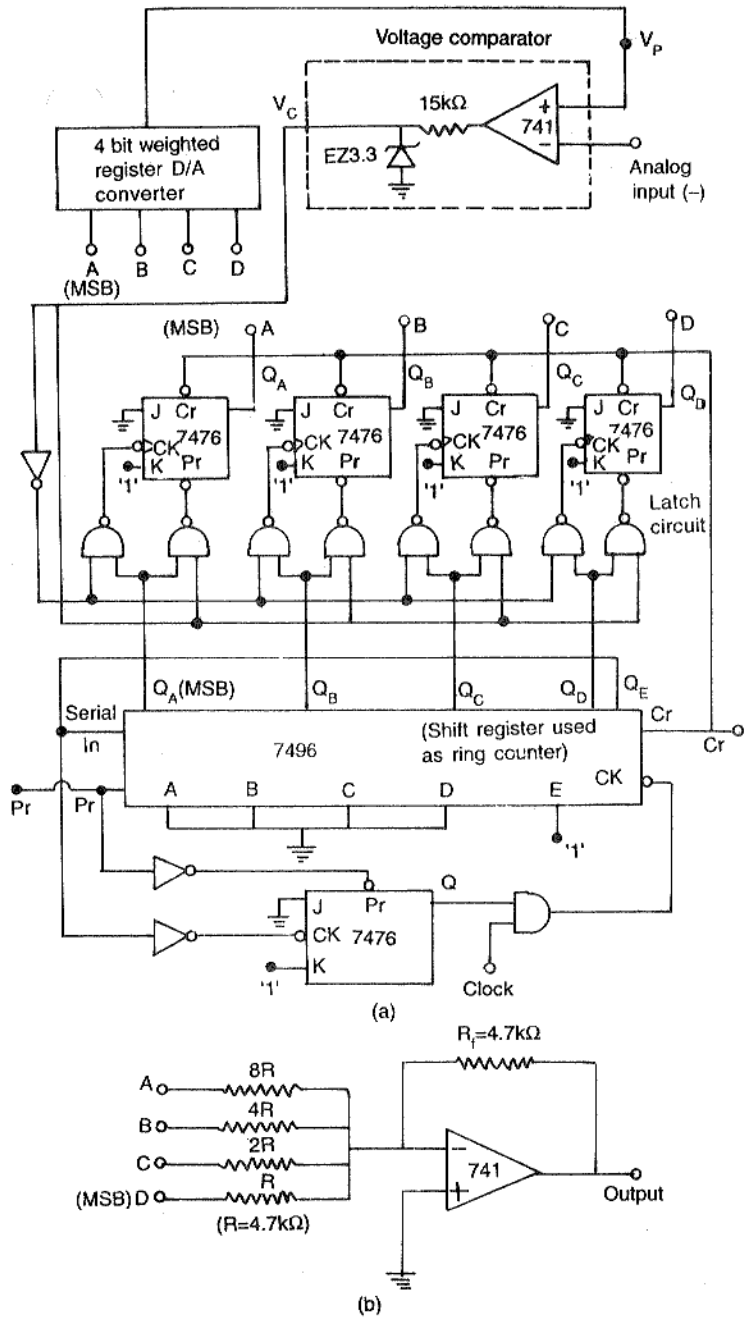


Fig. E. 10.2 (a) Successive approximation A/D converter (b) 4-bit weighted resistor D/A converter

3. Measure the output voltage for all binary inputs (0000 to 1111) states and plot a graph of binary inputs vs output voltage.
4. Measure the size of each step and hence calculate resolution.
5. Calculate linearity using the definition given in Sec. 10.4.

Experiment 10.2

To set up a 4-bit successive approximation type A/D converter and study its performance.

Procedure

(i) Set up the circuit as shown in Fig. E. 10.2(a). Use the circuit of Fig. E. 10.2(b) for 4-bit weighted resistor D/A converter.
(ii) Connect the Cr terminal to ground momentarily to clear all the flip-flops and the shift resistor IC 7496.
(iii) Connect the Pr terminal momentarily to logic '1' to set the shift register (being used as ring counter) output as $Q_E = 1$, $Q_A = Q_B = Q_C = Q_D = 0$, this will also enable the AND gate for the clock to be transmitted.
(iv) Apply an analog voltage of – 10V. Apply clock pulses, and observe the stable digital output available at the outputs Q_D, Q_C, Q_B, Q_A of the J-K flip-flops.
(v) Vary the input voltage for 0 to –10V and repeat steps (ii), (iii) and (iv).

Appendix-I

PSPICE TUTORIAL

SPICE is a general-purpose circuit program that simulates electronic circuits. SPICE contains models for various circuit elements, active as well as passive and is capable of simulating most of the electronic circuits. SPICE is acronym for *Simulation Program with Integrated Circuit Emphasis* and is used as a popular electrical circuit analysis program. SPICE was originally developed at the University of California, Berkley in the mid-1970s. SPICE has undergone a number of modifications over the years. PSPICE is a very popular version developed by MicroSim Corporation to run on DOS and MacIntosh personal computers.

This appendix includes a summary of the most common default representations for PSPICE circuit models.

PSPICE can be used to simulate and analyze circuits containing resistors, capacitors, inductors, independent and dependent voltage and current sources, and basic semiconductor devices. Separate SPICE models are used for diodes, BJT, JFET, MOSFET, MESFET and Op-Amps.

As a first step, the user must identify each node in the circuit. The location of an element in the circuit is specified by listing the two nodes to which it is connected. Each node is identified by an integer, however, the 0 is reserved for the ground or reference node. The orders in which the two nodes at the terminals of an element are listed are important. The first node is that one at which the +reference for the voltage across the circuit element is located. Thus an element connected between nodes 1 (first named) and 2 (last named) has the voltage V_{12} with the reference at node 1. The element current I_{12} flows from node 1 (first named) through the element to node 2 (last named).

A resistor is identified by a capital letter R followed by no more than seven additional letters or integers such as RI, ROUTPUT, RINPUT are okay but R1-2, R1/0 are not okay. The value of the resistor can be given in ohms or by use of scale factors as given in Table A-1.

Abbreviation	Meaning	Multiplier
P	pico	10^{-12}
N	nano	10^{-9}
U	micro	10^{-6}
M	milli	10^{-3}
K	kilo	10^{3}
MEG	mega	10^{6}
G	giga	10^{9}
T	tera	10^{12}

A statement given by

R1 1 2 10K

states that a resistance R1 is connected between nodes 1 and 2 with a value of 10 kΩ.

The independent voltage source is identified by a name beginning with *V* and followed by any combination of not more than seven additional letters or integers. Independent current sources have names beginning with *I*. Thus all the following statements represent dc voltage sources:

VIN 6 0 DC 1.5 → a voltage source VIN is connected between nodes 6 and ground of dc value 1.5 volt.

V2 1 2 DC 10M → a voltage source V2 is connected between nodes 1 and 2 of dc value 10 millivolt.

VCC 4 3 DC 9 → a voltage source VCC is connected between nodes 4 and 3 of dc value 9 volts.

A general sinusoidal input source shown in Fig. 1 has the syntax:

Sin (offset amp freq. delay)

e.g. V1 1 0 sin(0 1V 5 KHz)

means that a sinusoidal input source, V1 of peak amplitude of 1V and frequency 5 KHz is connected between nodes 1 and 0.

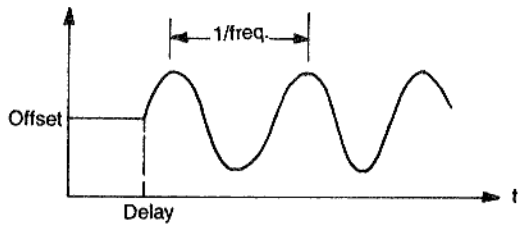


Fig. 1. A general sinusoidal input source

A pulse input source shown in the Fig. 2. has the syntax:

Pulse (V_1 V_2 DELAY T_{RISE} T_{FALL} DUR PERIOD)

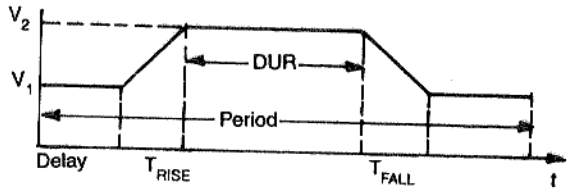


Fig. 2. A pulse input source

If a square wave input has to be applied to the nodes 1 and 0, then the statement will be given as

V1 1 0 pulse(–1V 1V 0MS 0MS 0MS .1MS .2MS)

So the input will be as shown in Fig. 3.

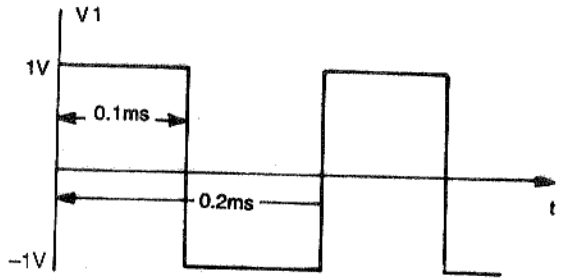


Fig. 3. Square wave input

A step input is given by

V1 1 0 pulse(0V 1V 0MS 0MS 0MS 1MS 1MS)

and is shown in Fig. 4.

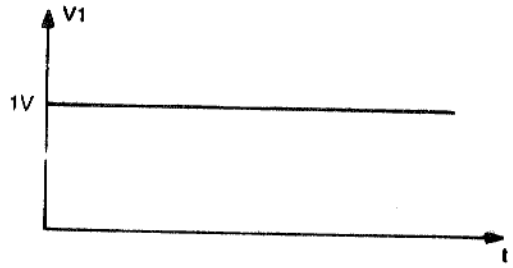


Fig. 4. Step input

Control Commands for Analysis

Note that the SPICE program always interprets the first line of program as title of the analysis. Hence always put the title of the circuit for which the analysis is being done. Each program begins with a TITLE statement and ends with an .END statement. For comments, any line beginning with (*) will be printed or displayed but not counted for analysis purpose by the computer.
The control statement

.OP

instructs the computer to calculate the dc voltage between each node and the reference node. The voltages at specific nodes can be obtained from the .PRINT statement. Note that the .PRINT command does not print anything on the paper. The control statement

.PRINT DC V(3) V(1, 3) 1(VX)

instructs the computer to calculate DC value of the node voltage V(3), node-to-node voltage named V (1, 3) between nodes 1 and 3, and the current named I(VX).
Every SPICE program must be ended with the last line as the control statement .END.

Capabilities of PSPICE

Using PSPICE, one can perform the following analysis:

1. DC analysis (large-signal transfer characteristics),
2. AC (small signal) analysis
3. Transient analysis

PSPICE simulation can be performed at different operating temperatures and thermal component noise can also be added. Output can be provided in the tabular form, two dimensional plots, graphs and Bode plots. A special feature of PSPICE is that it includes a graphical output interface called PROBE and a library of devices with pre determined characteristics called parts.

Each analysis is invoked by giving a command statement. The command statements for each of the above analysis are discussed as follows:

DC Analysis

The dc analysis is performed by the statement .DC
The syntax is as follows;

.DC	SOURCE	START	STOP	INCR
.DC	Vin	–5	5	0.1

This means that Vin in the circuit is varied from –5 to +5V in equal steps of 0.1 Volt. All the capacitors in the circuit are treated as open circuit and inductors as short circuit during this analysis.

AC Analysis (Sinusoidal steady state frequency response)

The syntax for performing the ac analysis is given as:

.AC SCALE TYPE NPOINTS FSTART FSTOP

The parameter SCALETYPE must be set to LIN, DEC or OCT, that is frequency scale can be selected with linear increments, logarithmic increments or octaves of frequency. Thus the statement

.AC DEC 50 1K 1MEG

will calculate response at 50 points per decade starting at 1 KHz and up to 1 Mega Hz. If analysis is desired at a single frequency, then NPOINTS, FSTART and FSTOP should be set to 1.

Transient Analysis

.TRAN

.TRAN computes the output of the circuit as a function of time in response to input signal sources designated as SIN, PULSE or PWL (piecewise linear). The .TRAN statement is written as:

.TRAN TSTEP TSTOP TSTART TINCR UIC

The last three entries are optional. The analysis always begins at t = 0 and ends at t = TSTOP. The output is printed or plotted after every time increment TSTEP. TSTART specifies the time at which output begins. If TSTART is nonzero, analysis begins at t = 0 but the output is printed or plotted at time TSTART. If TSTART is omitted, its value by default is zero. Computations are performed using a time increment specified by TINCR. If TINCR is omitted, its value is set to (TSTART-TSTOP)/50. The UIC gives the user initial condition.

Generating Output

In the older versions of SPICE, output was generated by using .PRINT and .PLOT control statements. In PSPICE, however, output is generated in graphical form by including the command line .PROBE in the input file. The graphical interface screen displayed by Probe is user friendly. Some typical functions possible in Probe include plotting graphs of voltages or currents w.r.t. to other voltages, currents or time, adding comments, text to graphs, analyzing plots using cursors, and generating hard copy output.

Only limited features of PSPICE have been discussed in this Appendix. Further details can be found in the following references.

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Appendix-II

ANSWER TO SELECTED PROBLEMS

Chapter-2

1. 100 μV
3. 10 kΩ, 90 kΩ
5. − 10
9. 100 μV, 0 V, 0.01 V
11. –2.585 V
12. 0.1V, 4.9 V
15. 137.5 kΩ
18. 7.5 mA, 2.5 mA

Chapter-3

1. 606 mV
2. 0.48 V
3. 0.606 V, 5 V

Chapter 4

1. $-5V_1 + 2V_2$
2. 3 V
3. 0.979 V, 2.22 kΩ
9. $-1.64\,(t) + 3.24(t - 250) - 1.64\,(t - 500)$
10. $-2 \sin 10^4 t - 5\times 10^3 t$
11. 20 dB, 16.989 dB
15. $\dfrac{0.33\times 10^7}{s + 1.67\times 10^6}$

Chapter 5

4. 3.836 V, − 3.836 V
5. ± 6.9 V
7. 5V, ± 5V, 99 kΩ
9. 15, 3.73 V, –2.66 V, 0 V
12. 11.6 kΩ, 10 kΩ, 5 kΩ, 0.01 μF

Chapter 6

1. 25 Ω
3. $R_1 = 3R_2$
4. R_{sc} = 8.3 Ω
6. R_1 = 200 Ω
   R_2 = 100 Ω for I_L = 50 mA

Chapter 7

2. 5
3. 1 kHz, 1.74
4. 9
6. 1.6 kΩ, for $R_f = R_i$ = 10 kΩ; C = 0.1 μF
7. 2050 Hz, 1950 Hz
10. (a) $\dfrac{1}{RCs + 1}$; (b) $\dfrac{-s}{s^2 + 2s + 1}$

Chapter 8

2. 6.06 kΩ
3. 62.1 μs, 46.92 μs, 9.18 kHz, 43%
4. 0.1 μF, 108.75 kΩ, 72.5 kΩ
5. 0.1 μF, $R_A = R_B$ = 725 Ω

Chapter 9

1. 653.6 kHz
2. − 0.1 V
3. 2.5 V
4. 2500 Hz, ± 812.5 Hz, ± 59.95 Hz
5. ± 275.6 Hz.

Chapter 10

1. 4, 33.33% of full scale
2. 6.9 V
3. 0.102
4. − 3.33 V, − 1.66 V, − 0.82 V, − 0.39 V, − 0.156 V
7. 512, 0.0254 V
10. 2 μs
11. 0.629 μF
12. 101000100001100001

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