their linear region by supplying currents into the bases by the external circuit. In an ideal op-amp, we assumed that no current is drawn from the input terminals. However, practically, input terminals do conduct a small value of dc current to bias the input transistors. The base currents entering into the inverting and non-inverting terminals are shown as I_B^- and I_B^+ respectively in Fig. 3.1 (a). Even though both the transistors are identical, I_B^- and I_B^+ are not exactly equal due to internal imbalances between the two inputs. Manufacturers specify input bias current I_B as the average value of the base currents entering into the terminals of an op-amp.

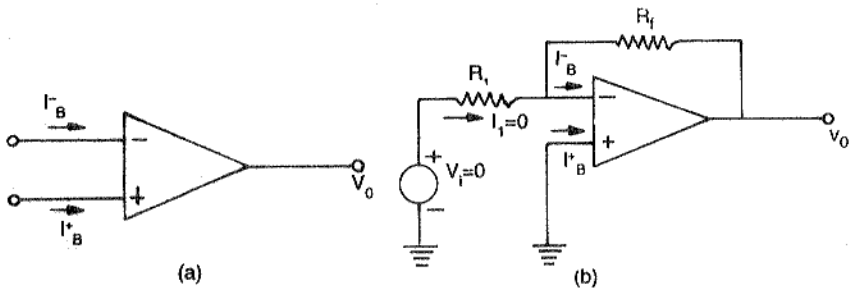


Fig. 3.1 (a) Input bias currents (b) inverting amplifier with bias currents

So, $$I_B = \frac{I_B^+ + I_B^-}{2} \tag{3.1}$$

For 741, a bipolar op-amp, the bias current is 500 nA or less. The FET input op-amp will have bias currents as low as 50 pA at room temperature.

Consider the basic inverting amplifier of Fig. 3.1 (b). If input voltage V_i is set to zero volt, the output voltage V_o should also be zero volt. Instead, we find that the output voltage is offset by,

$$V_o = (I_B^-)R_f \tag{3.2}$$

For a 741 op-amp, with a 1 MΩ feedback resistor,

$$V_o = 500 \text{ nA} \times \text{I MΩ} = 500 \text{ mV}$$

The output is driven to 500 mV with zero input because of the bias currents. In applications where signal levels are measured in millivolts, this is totally unacceptable. This effect can be compensated for as shown in Fig. 3.1 (c) where a compensation resistor R_{comp} has been added between the noninverting input terminal and ground. Current I_B^+ flowing through the compensating resistor R_{comp} develops a voltage V_1 across it. Then, by KVL, we get,

$$-V_1 + 0 + V_2 - V_o = 0$$

or $$V_o = V_2 - V_1 \tag{3.3}$$

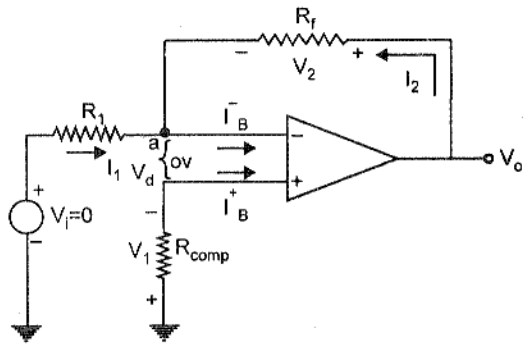


Fig. 3.1 (c) Bias current compensation

By selecting proper value of R_{comp}, V_2 can be cancelled with V_1 and the output V_o will be zero. The value of R_{comp} is derived as

$$V_1 = I_B^+ R_{comp}$$

or $$I_B^+ = \frac{V_1}{R_{comp}} \tag{3.4}$$

The node 'a' is at voltage $(-V_1)$, because the voltage at the non-inverting input terminal is $(-V_1)$. So, with $V_i = 0$, we get,

$$I_1 = \frac{V_1}{R_1} \tag{3.5}$$

Also, $$I_2 = \frac{V_2}{R_f} \tag{3.6}$$

For compensation, V_o should be zero for $V_i = 0$, that is, from Eq. (3.3) $V_2 = V_1$

So that, $$I_2 = \frac{V_1}{R_f} \tag{3.7}$$

KCL at node 'a' gives,

$$I_B^- = I_2 + I_1 = \frac{V_1}{R_f} + \frac{V_1}{R_1} = V_1 \frac{(R_1 + R_f)}{R_1 R_f} \tag{3.8}$$

Assuming $I_B^- = I_B^+$ and using Eqs. (3.4) and (3.8) we get,

$$V_1 \frac{(R_1 + R_f)}{R_1 R_f} = \frac{V_1}{R_{comp}}$$

or, $$R_{comp} = \frac{R_1 R_f}{R_1 + R_f} = R_1 \,||\, R_f \tag{3.9}$$

that is, to compensate for bias currents, the compensating resistor R_{comp} should be equal to the parallel combination of resistors tied to the inverting input terminal.

3.2.2 Input Offset Current

Bias current compensation will work if both bias currents I_B^+ and I_B^- are equal. Since the input transistors cannot be made identical, there will always be some small difference between I_B^+ and I_B^-. This difference is called the offset current I_{os} and can be written as

$$|I_{os}| = I_B^+ - I_B^- \tag{3.10}$$

The absolute value sign indicates that there is no way to predict which of the bias currents will be larger.

Offset current I_{os} for BJT op-amp is 200 nA and that for FET op-amp is 10 pA. Even with bias current compensation, offset current will produce an output voltage when the input voltage V_i is zero. Referring to Fig. 3.1 (c),

$$V_1 = I_B^+ R_{comp} \tag{3.11}$$

and $$I_1 = \frac{V_1}{R_1} \tag{3.12}$$

KCL at node 'a' gives,

$$I_2 = (I_B^- - I_1) = I_B^- - \left(I_B^+ \frac{R_{comp}}{R_1}\right) \tag{3.13}$$

Again

$$\begin{aligned} V_o &= I_2 R_f - V_1 \\ &= I_2 R_f - I_B^+ R_{comp} \\ &= \left(I_B^- - I_B^+ \frac{R_{comp}}{R_1}\right) R_f - I_B^+ R_{comp} \end{aligned} \tag{3.14}$$

Substituting Eq. (3.9) and after algebraic manipulation,

$$V_o = R_f [I_B^- - I_B^+] \tag{3.15}$$

So, $$V_o = R_f I_{os} \tag{3.16}$$

So even with bias current compensation and with the feedback resistor of 1 MΩ, a 741 BJT op-amp has an output offset voltage

$$V_o = 1\ \text{MΩ} \times 200\ \text{nA} = 200\ \text{mV}$$

with a zero input voltage. It can be seen from Eq. (3.16) that the effect of offset current can be minimized by keeping feedback resistance small. Unfortunately, to obtain high input impedance, R_1 must be kept large. With R_1 large, the feedback resistor R_f must also be high so as to obtain reasonable gain.

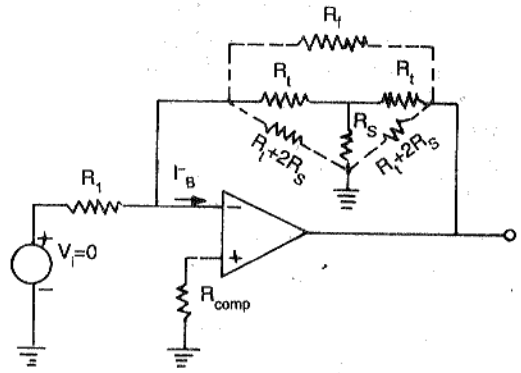


Fig. 3.1 (d) Inverting amplifier with T-feedback network

The T-feedback network in Fig. 3.1 (d) is a good solution. This will allow large feedback resistance, while keeping the resistance to ground (seen by the inverting input) low as shown in the dotted network. The T-network provides a feedback signal as if the network were a single feedback resistor. By T to π conversion,

$$R_f = \frac{R_t^2 + 2 R_t R_s}{R_s} \tag{3.17}$$

To design a T-network, first pick

$$R_t << \frac{R_f}{2} \tag{3.18}$$

Then calculate $R_s = \dfrac{R_t^2}{R_f - 2R_t}$ (3.19)

Example 3.1

Design an inverting amplifier of the type shown in Fig. 3.1 (d) using 741 op-amp to get a gain of – 10 and an input impedance of 10 MΩ. That is, calculate R_t, R_s and R_1.

Solution

In Fig. 3.1 (d), to set input impedance R_i = 10 MΩ, pick R_1 = 10 MΩ

Since, $$A_{CL} = -\frac{R_f}{R_1}$$

Therefore $R_f = A_{CL}R_1 = (10)\ (10\ \text{M}\Omega) = 100\ \text{M}\Omega$

Choose $R_t = 47\ \text{k}\Omega$

$$R_s = \frac{R_t^2}{R_f - 2R_t} = \frac{(47\ \text{k}\Omega)^2}{100\ \text{M}\Omega - 2(47\ \text{k}\Omega)} = 22\ \Omega$$

3.2.3 Input Offset Voltage

Inspite of the use of the above compensating techniques, it is found that the output voltage may still not be zero with zero input voltage. This is due to unavoidable imbalances inside the op-amp and one may have to apply a small voltage at the input terminals to make output voltage zero. This voltage is called input offset voltage V_{os}. This is the voltage required to be applied at the input for making output voltage to zero volts as shown in Fig. 3.2. (a).

Let us now examine the effect of V_{os} on the output of a non-inverting and inverting op-amp amplifier as shown in Fig. 3.2 (b, c). If V_i is set to zero, the circuits of Fig. 3.2 (b and c) become the same as in Fig. 3.2 (d). The voltage V_2 at the (–) input terminal is given by

$$V_2 = \left(\frac{R_1}{R_1 + R_f}\right)V_o \tag{3.20}$$

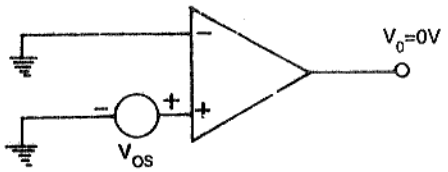


Fig. 3.2 (a) Op-amp showing input offset voltage

or $$V_o = \left(\frac{R_1 + R_f}{R_1}\right)V_2 = \left(1 + \frac{R_f}{R_1}\right)V_2 \tag{3.21}$$

Since, $V_{os} = |V_i - V_2|$ and $V_i = 0$,

$$V_{os} = |0 - V_2| = V_2 \tag{3.22}$$

or, $$V_o = \left(1 + \frac{R_f}{R_1}\right)V_{os} \tag{3.23}$$

Thus, the output offset voltage of an op-amp in closed-loop configuration (inverting or non-inverting) is given by Eq. (3.23).

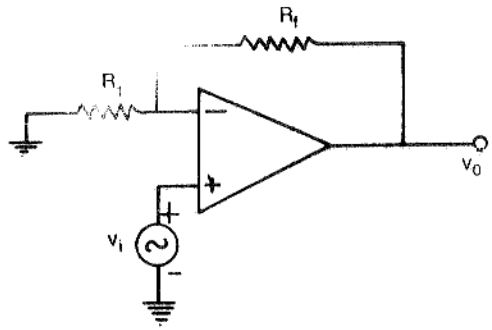


Fig. 3.2 (b) Non-inverting amplifier

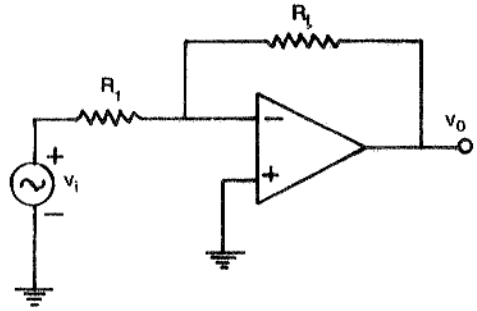


Fig. 3.2 (c) Inverting amplifier

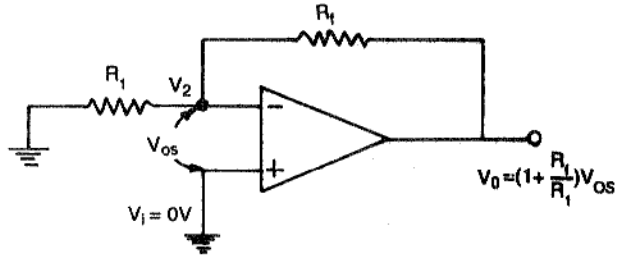


Fig. 3.2 (d) equivalent circuit for $V_i = 0$

3.2.4 Total Output Offset Voltage

The total output offset voltage V_{oT} could be either more or less than the offset voltage produced at the output due to input bias current or input offset voltage alone. This is because input offset voltage V_{os} and input bias current I_B could be either positive or negative with respect to ground. Therefore, the maximum offset voltage at the output of an inverting and non-inverting amplifier of Fig. 3.2 (b, c) without any compensating technique used, is given by

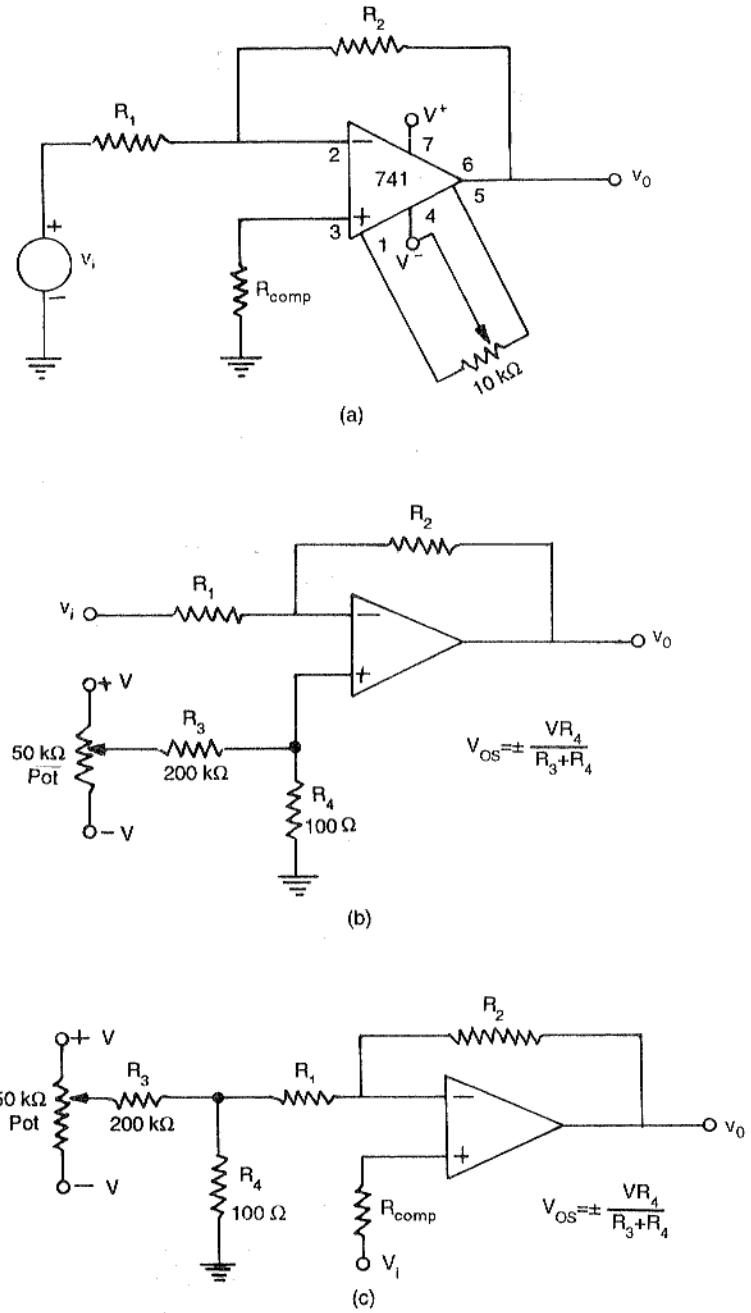


Fig. 3.3 (a) Offset null pin connection for μA741. Balancing circuit for (b) Inverting amplifier (c) Non-inverting amplifier

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B \tag{3.24}$$

However, with R_{comp} in the circuit, the total output offset voltage will be given by

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os} \tag{3.25}$$

Many op-amps provide offset compensation pins to nullify the offset voltage. So one must refer to the manufacturer's specifications while using the offset null connections. Figure 3.3 (a) gives the connections for the 741 op-amp. The manufacturers recommend that a 10 kΩ potentiometer be placed across offset null pins 1 and 5 and the wiper be connected to the negative supply pin 4. The position of the wiper is adjusted to nullify the output offset voltage. However, when the given op-amp does not have these offset null pins, external balancing techniques are used. Figures 3.3 (b, c) show the balancing circuits used for inverting and non-inverting operational amplifiers.

Example 3.2

(a) For the non-inverting amplifier of Fig. 3.2 (b), R_1 = 1 kΩ and R_f = 10 kΩ. Calculate the maximum output offset voltage due to V_{os} and I_B. The op-amp is LM 307 with V_{os} = 10 mV and I_B = 300 nA, I_{os} = 50 nA.

(b) Calculate the value of R_{comp} needed to reduce the effect of I_B.

(c) Calculate the maximum output offset voltage if R_{comp} as calculated in (b) is connected in the circuit.

Solution

(a) $$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_B$$

$$= \left(1 + \frac{10\ \text{k}\Omega}{1\ \text{k}\Omega}\right) (10\ \text{mV}) + (10\ \text{k}\Omega)\ (300\ \text{nA})$$

$$= 110\ \text{mV} + 3\ \text{mV} = 113\ \text{mV}$$

(b) The value of R_{comp} needed is,

$$R_{comp} = 1\ \text{k}\Omega \,\|\, 10\ \text{k}\Omega = 990\ \Omega$$

(c) With R_{comp} in the circuit,

$$V_{oT} = \left(1 + \frac{R_f}{R_1}\right) V_{os} + R_f I_{os}$$

$$= 110\ \text{mV} + 0.5\ \text{mV} = 110.5\ \text{mV}$$

It can be seen from this example that it is the input offset voltage which is more responsible for producing an output offset voltage compared to input bias current I_B or the input offset current I_{os}.

3.2.5 Thermal Drift

Bias current, offset current and offset voltage change with temperature. A circuit carefully nulled at 25°C may not remain so when the temperature rises to 35°C. This is called drift. Often, offset current drift is expressed in nA/°C and offset voltage drift in mV/°C. These indicate the change in offset for each degree celsius change in temperature.

There are very few circuit techniques that can be used to minimize the effect of drift. Careful printed circuit board layout must be used to keep op-amps away from source of heat. Forced air cooling may be used to stabilize the ambient temperature.

Example 3.3

A non-inverting amplifier with a gain of 100 is nulled at 25°C. What will happen to the output voltage if the temperature rises to 50°C for an offset voltage drift of 0.15 mV/°C ?

Solution

Input offset voltage due to temperature rise = 0.15 mV/°C × (50°C – 25°C) = 3.75 mV. Since this is an input change, the output voltage will change by

$$V_o = V_{os} \times A_{CL}$$
$$= 3.75 \text{ mV} \times 100 = 375 \text{ mV}$$

This could represent a very major shift in the output voltage.

3.3 AC CHARACTERISTICS

We have discussed so far the dc characteristics such as bias current, offset current, offset voltage and thermal drift. These will affect the steady state (dc) response of the op-amp only. For small signal sinusoidal (ac) applications, one has to know the ac characteristics such as frequency response and slew-rate which will be discussed in this section.

3.3.1 Frequency Response

Ideally, an op-amp should have an infinite bandwidth. This means that, if its open-loop gain is 90 dB with dc signal its gain should remain the same 90 dB through audio and on to high radio frequencies. The practical op-amp gain, however, decreases (rolls-off) at higher frequencies.

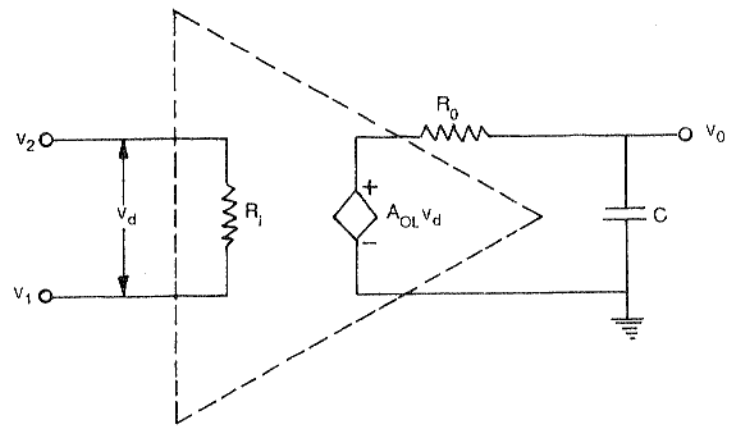


Fig. 3.4 (a) High frequency model of an op-amp with single corner frequency

What causes the gain of the op-amp to roll-off after a certain frequency is reached? Obviously, there must be a capacitive component in the equivalent circuit of the op-amp. This capacitance is due to the physical characteristics of the device (BJT or FET) used and the internal construction of op-amp. For an op-amp with only one break (corner) frequency, all the capacitor effects can be represented by a single capacitor C as shown in Fig. 3.4 (a). This figure represents the high frequency model of the op-amp with a single corner frequency. It may be observed that the high frequency model of Fig. 3.4 (a) is a modified version of the low frequency model with a capacitor C at the output. There is one pole due to R_oC and obviously one – 20 dB/decade roll-off comes into effect.

The open loop voltage gain of an op-amp with only one corner frequency is obtained from Fig. 3.4 (a) as

$$v_o = \frac{-jX_c}{R_o - jX_c} A_{OL} v_d \tag{3.26}$$

or,
$$A = \frac{v_o}{v_d} = \frac{A_{OL}}{1 + j\,2\pi f R_o C}$$

or,
$$A = \frac{A_{OL}}{1 + j(f/f_1)} \tag{3.27}$$

where
$$f_1 = \frac{1}{2\pi R_o C} \tag{3.28}$$

is the corner frequency or the upper 3-dB frequency of the op-amp. The magnitude and the phase angle of the open loop voltage gain are function of frequency and can be written as

$$|A| = \frac{A_{OL}}{\sqrt{1+(f/f_1)^2}} \tag{3.29}$$

$$\phi = -\tan^{-1}(f/f_1) \tag{3.30}$$

The magnitude and phase characteristics from Eq. (3.29) and (3.30) are shown in Fig. 3.4 (b, c). It can be seen that

(i) For frequency $f << f_1$, the magnitude of the gain is 20 log A_{OL} in dB.

(ii) At frequency $f = f_1$, the gain is 3 dB down from the dc value of A_{OL} in dB. This frequency f_1 is called corner frequency.

(iii) For $f >> f_1$, the gain rolls-off at the rate of –20 dB/decade or –6 dB/octave.

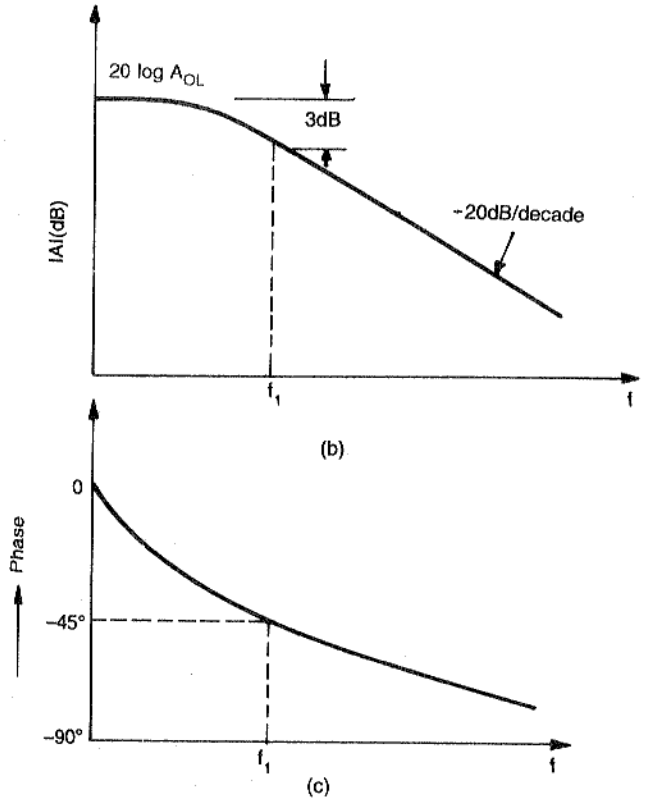


Fig. 3.4 (b) Open loop magnitude characteristics in semilog paper and (c) phase characteristics for an op-amp with single break frequency

It can further be seen from the phase characteristics that the phase angle is zero at frequency $f = 0$. At corner frequency f_1 the phase angle is $-45°$ (lagging) and at infinite frequency the phase angle is $-90°$. This shows that a maximum of 90° phase change can occur in an

op-amp with a single capacitor. It may be mentioned here, that zero frequency does not occur in log scale. From all practical purposes, zero frequency is taken as one decade below the corner frequency and infinite frequency is one decade above the corner frequency. The voltage transfer function is s-domain can be written as

$$A = \frac{A_{OL}}{1+j(f/f_1)} = \frac{A_{OL}}{1+j(\omega/\omega_1)}$$

$$= \frac{A_{OL}\cdot\omega_1}{j\omega+\omega_1} = \frac{A_{OL}\cdot\omega_1}{s+\omega_1}$$

A practical op-amp, however, has number of stages and each stage produces a capacitive component. Thus due to a number of RC pole pairs, there will be a number of different break frequencies. The transfer function of an op-amp with three break frequencies can be assumed as

$$A = \frac{A_{OL}}{\left(1+j\frac{f}{f_1}\right)\left(1+j\frac{f}{f_2}\right)\left(1+j\frac{f}{f_3}\right)};\ 0<f_1<f_2<f_3 \tag{3.31}$$

or,
$$A = \frac{A_{OL}\cdot\omega_1\cdot\omega_2\cdot\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \tag{3.32}$$

with $0 < \omega_1 < \omega_2 < \omega_3$.

For a typical op-amp, straight line approximation of open-loop gain vs frequency in logarithmic scale is shown in Fig. 3.5. The open loop

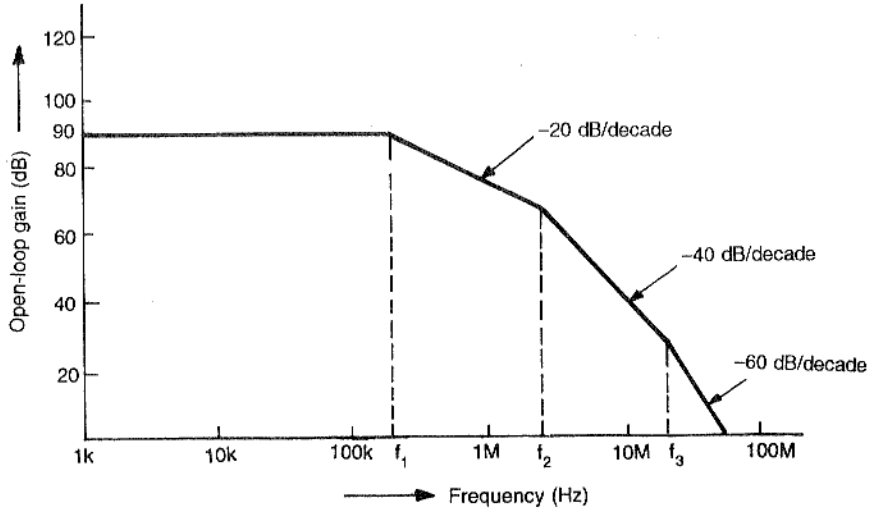


Fig. 3.5 Approximation of open loop gain vs frequency curve

equency response is flat (90 dB) from low frequencies (including dc) to 200 kHz, the first break frequency. From 200 kHz to 2 MHz, the gain drops from 90 dB to 70 dB which is at a –20 dB/decade or –6 dB/octave rate. At frequencies from 2 MHz to 20 MHz, the roll-off rate is –40 dB/decade or –12 dB/octave. Accordingly, as frequency is increasing, cascading effect of RC pairs (poles) come into effect and roll-off rate increases successively by –20 dB/decade at each corner frequency. Each RC pole pair also introduces a lagging phase of maximum up to –90°.

3.3.2 Stability of an Op-Amp

Op-amps are rarely used in open loop configuration because of its high gain. Let us now consider the effect of feedback on op-amp frequency response. Consider an op-amp amplifier of Fig. 3.6. (a). It uses resistor feedback network and may be used as an inverting amplifier for $v_2 = 0$ and as non-inverting amplifier for $v_1 = 0$.

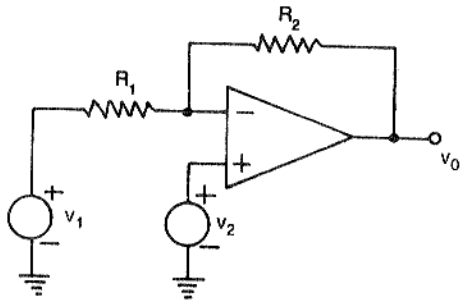


Fig. 3.6 (a) Resistive feedback provided in op-amp

From the negative feedback concepts, we may write the closed loop transfer function as

$$A_{CL} = \frac{A}{1 + A\beta} \tag{3.33}$$

where A is the open loop voltage gain and β is the feedback ratio. In Eq. (3.33), if characteristic equation $(1 + A\beta) = 0$, the circuit will become just unstable, that is, leads into sustained oscillation.

Rewriting the characteristic equation as, $1 - (-A\beta) = 0$ leads to

$$\text{loop gain}, -A\beta = 1 \tag{3.34}$$

Since $A\beta$ is a complex quantity, the magnitude condition become

$$|A\beta| = 1 \tag{3.35}$$

and phase condition is

$$\underline{/-A\beta} = 0 \text{ (or multiple of } 2\pi)$$

or,

$$\underline{/A\beta} = \pi \text{ (or odd multiple of } \pi) \tag{3.36}$$

In the given circuit, feedback network is a resistive network, so it does not provide any phase shift. Since op-amp is used in the inverting mode, it provides a phase shift of 180° at low frequencies. However, at high frequencies, due to each corner frequency, an additional phase shift of maximum –90° can take place in open loop gain A. So for two corner frequencies, a maximum of phase shift that can be associated with gain A is –180°. Thus at high frequencies, it is quite possible that for some value of β, the magnitude of $A\beta$ becomes unity when A has an additional phase shift of 180° which makes the total phase shift equal to zero. In this case, there is every possibility that the amplifier may begin to oscillate as both the magnitude and phase conditions laid down by Eqs. (3.35) and (3.36) are satisfied. This may be noted that oscillation is just the starting point of instability, or, to be more precise, it is just at the verge of instability. The instability means unbounded output; which can arise from Eq. (3.33), when

$$(1 + A\beta) < 1$$

or $$A\beta < 0 \qquad \text{i.e. negative}$$

and then $A_{CL} > A$, i.e. the closed loop gain increases and leads to instability. The phase contribution by the resistive feedback network is zero. At low frequency, the additional phase contribution of A is zero, so $A\beta > 0$ and obviously $A_{CL} < A$ and the system is stable. But at high frequencies, the system A having three corner frequencies or three RC pole pair, there is a chance of open loop gain A to contribute a maximum of $-270°$ phase shift and for which $A\beta$ may become negative and instability occurs at high frequencies. This is further elaborated in Fig. 3.6 (b).

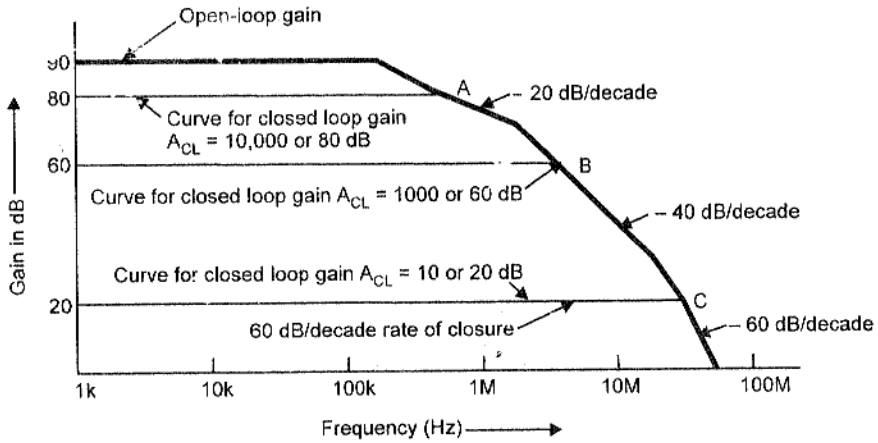


Fig. 3.6 (b) Effect of feedback on open loop gain vs frequency curve

Let us say that a closed loop gain of 80 dB ($|A_{CL}| = 10{,}000$) is desired. The projection of 80 dB curve to the open loop frequency response curve intersects it at a – 20 dB/decade rate of closure (point A)

as shown in Fig. 3.6 (b). The bandwidth is approximately 600 kHz and a maximum of –90° phase shift is added to open loop gain A. The amplifier will remain stable.

Now, if the feedback resistors are so chosen that the op-amp has a closed loop gain of 1,000 or 60 dB, the bandwidth is about 3.5 MHz. However, now the 60 dB projection on the open-loop curve intersects at a –40 dB/decade rate of closure (point B). The maximum phase shift that may get added to is now (– 90° – 90°), that is –180°. This circuit is likely to be unstable and should not be used without modification. Similarly, a closed loop gain of 20 dB causes a – 60 dB/decade rate of closure (point C). A maximum –270° phase shift is added to the open loop gain A to cause unstable operation. Thus, we may conclude that for stable operation, the rate of closure between the closed loop gain projection and the open-loop curve should not exceed –20 dB/decade. At higher frequencies for lower closed loop gains, the feedback becomes significant and regenerative and may result in sustained oscillations.

So far, we have discussed stability of an op-amp qualitatively. To provide a quantitative discussion about stability, let us rewrite the transfer function of an op-amp characterized by three poles, as,

$$A = -\frac{A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)};\ 0 < \omega_1 < \omega_2 < \omega_3$$

Obviously the poles of the open-loop transfer function are at $-\omega_1$, $-\omega_2$ and $-\omega_3$. The closed loop poles, that is the poles of A_{CL} in Eq. (3.33) will be given by the roots of the characteristic equation

$$1 + A\beta = 0$$

Putting the value of A from Eq. (3.32) we get,

$$1 + \frac{\beta A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} = 0$$

or, $$(s+\omega_1)(s+\omega_2)(s+\omega_3) + \beta A_{OL}\,\omega_1\,\omega_2\,\omega_3 = 0$$

or, $$s^3 + s^2(\omega_1+\omega_2+\omega_3) + s(\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3) + \omega_1\omega_2\omega_3 (1 + \beta A_{OL}) = 0 \quad (3.37)$$

The roots of the cubic equation depend upon βA_{OL}, the dc loop gain and therefore, (βA_{OL}) becomes critical parameter that determines the new pole location. Further, βA_{OL} can take any value between zero for no feedback ($\beta = 0$) and A_{OL} for maximum feedback ($\beta = 1$). For variable β in the range $0 < \beta A_{OL} < \infty$, the root loci is shown in Fig. 3.7. When $\beta A_{OL} = 0$, the roots are at $-\omega_1$, $-\omega_2$ and $-\omega_3$ and lie on the negative real axis. For small values of βA_{OL} the roots still lie on the left half os s-plane with one real root and two complex conjugate roots (a, a′). If βA_{OL} is increased further beyond a critical value $(\beta A_{OL})_c$, the two roots will move to the right half of s-plane causing instability. We

will find out that critical value of βA_{OL} for which the closed loop system becomes just unstable. Rewriting Eq. (3.37) as

$$a_3 s^3 + a_2 s^2 + a_1 s + a_o = 0 \quad (3.38)$$

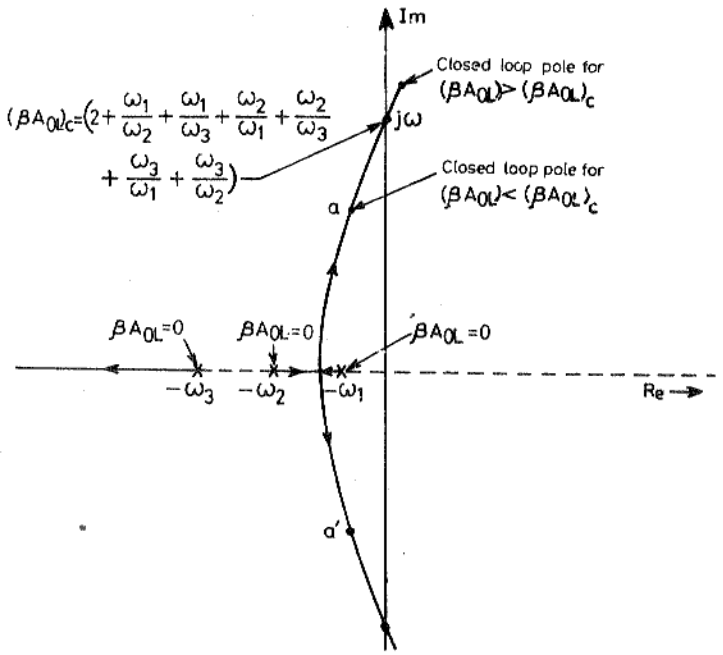


Fig. 3.7 Root loci as a function of βA_{OL}

where,

$$a_3 = 1$$
$$a_2 = \omega_1 + \omega_2 + \omega_3$$
$$a_1 = \omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3$$
$$a_o = \omega_1\omega_2\omega_3\,(1 + \beta A_{OL})$$

In order to find the critical value of βA_{oL}, apply Routh's stability criterion to Eq. (3.38). That is,

(i) All the coefficients a_3, a_2, a_1 and a_o should be positive.

(ii) $a_2 a_1 - a_3 a_o \le 0 \quad (3.39)$

Put $s = j\omega$ in Eq. (3.38)

$$a_3(j\omega)^3 + a_2(j\omega)^2 + a_1(j\omega) + a_o = 0$$
$$(a_o - a_2\omega^2) + j\omega(a_1 - a_3\omega^2) = 0$$

Equating real and imaginary parts to zero, we get

$$a_o - a_2\omega^2 = 0, \quad (3.40)$$
$$a_1 - a_3\omega^2 = 0 \quad (3.41)$$

Thus, the frequency of oscillation is given by,

$$\omega_{osc} = \pm\sqrt{\frac{a_0}{a_2}} = \pm\sqrt{\frac{a_1}{a_3}} \qquad (3.42)$$

Putting values of coefficients,

$$\omega_{osc} = \sqrt{\frac{a_1}{a_3}} = \sqrt{\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3}$$

Also from Eq. (3.39), we get,

$$a_0 = \frac{a_2\, a_1}{a_3}$$

or $\omega_1\omega_2\omega_3\,\{1 + (\beta A_{OL})_c\} = (\omega_1 + \omega_2 + \omega_3)\,(\omega_1\omega_2 + \omega_1\omega_3 + \omega_2\omega_3)$

or, $$(\beta A_{OL})_c = 2 + \frac{\omega_1}{\omega_2} + \frac{\omega_1}{\omega_3} + \frac{\omega_2}{\omega_1} + \frac{\omega_2}{\omega_3} + \frac{\omega_3}{\omega_1} + \frac{\omega_3}{\omega_2} \qquad (3.44)$$

It is obvious that $(\beta A_{OL})_c$ depends upon the ratio of open loop pole locations. The minimum value of $(\beta A_{OL})_c$ will occur when all the poles are located at the same place giving $(\beta A_{OL})_c = 8$.

As an example, if $A_{OL} = 10^5$ and $\omega_1 = \omega_2 = \omega_3 = 10^7$ rad/s, then the circuit will oscillate at a frequency of

$$\omega_{osc} = \omega_1\sqrt{3} = 10^7\sqrt{3}\ \text{rad/s}.$$

On the other hand, if 10000 $\omega_1 = \omega_2 = \omega_3$, the critical loop gain is,

$$(\beta A_{OL})_c \simeq 2\frac{\omega_2}{\omega_1} \simeq 20000$$

and, $$\beta_c < \frac{20000}{A_{OL}} = \frac{20000}{100000} = 0.2$$

In the Fig. 3.6 (a), $\beta = R_1/(R_1 + R_2)$.

For, $\beta < 0.2$,

$$\frac{R_1 + R_2}{R_1} > \frac{1}{0.2} = 5$$

or, $$\frac{R_2}{R_1} \geq 4$$

This means that if op-amp is used as an inverting amplifier in Fig. 3.6 (a), the inverting gain magnitude should be greater than 4 and if used as non-inverting amplifier, the non-inverting gain should be greater than 5 for oscillation to sustain.

If it is desired that the amplifier should remain stable for any resistive network, that is, $0 < \beta < 1$, then A_{OL} must satisfy the most stringent condition for $\beta = 1$, that is,

$$A_{OL} < \left(2 + \frac{\omega_1}{\omega_2} + \frac{\omega_1}{\omega_3} + \frac{\omega_2}{\omega_1} + \frac{\omega_2}{\omega_3} + \frac{\omega_3}{\omega_1} + \frac{\omega_3}{\omega_2}\right) \qquad (3.45)$$

3.3.3 Frequency Compensation

In applications where one desires large bandwidth and lower closed loop gain, suitable compensation techniques are used. Two types of compensating techniques are used (i) External Compensation, (ii) Internal Compensation.

External Frequency Compensation

Some types of op-amps are made to be used with externally connected compensating components specially if they are to be used for relatively low closed loop gain. The compensating network alters the open-loop gain so that the roll-off rate is –20 dB/decade over a wide range of frequency.

The common methods for accomplishing this are:

Dominant-pole compensation
Pole-zero (lag) compensation

Dominant-pole Compensation: Suppose A is the uncompensated transfer function of the op-amp in open-loop condition as given by Eq. (3.32). Introduce a dominant pole by adding RC-network in series with op-amp as in Fig. 3.8 (a) or by connecting a capacitor C from a suitable high resistance point to ground. The compensated transfer function A' becomes

$$A' = \frac{v_o}{v_i}$$

$$= A \cdot \frac{\frac{-j}{\omega C}}{R - \frac{j}{\omega C}} = \frac{A}{1 + j\frac{f}{f_d}} \qquad (3.46)$$

where, $$f_d = \frac{1}{2\pi RC}$$

using Eq. (3.31) we get,

$$A' = \frac{A_{OL}}{\left(1 + j\frac{f}{f_d}\right)\left(1 + j\frac{f}{f_1}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)}$$

where $f_d < f_1 < f_2 < f_3$

The capacitance C is chosen so that the modified loop gain drops to 0 dB with a slop of –20 dB/decade at a frequency where the poles of uncompensated transfer function A contribute negligible phase shift. Usually $f_d = \omega_d/2\pi$ is selected so that the compensated transfer function A' passes through 0 dB at the pole f_1 of the uncompensated A. The frequency can be found graphically by having A' pass through 0 dB at the frequency f_1 with a slope of – 20 dB per decade as shown in the Fig. 3.8 (b). The value of capacitor C now can be calculated since $f_d = 1/2\pi RC$. There is, however, one disadvantage of this compensating technique. It reduces the open-loop bandwidth drastically. But the noise immunity of the system is improved since the noise frequency components outside the bandwidth are eliminated.

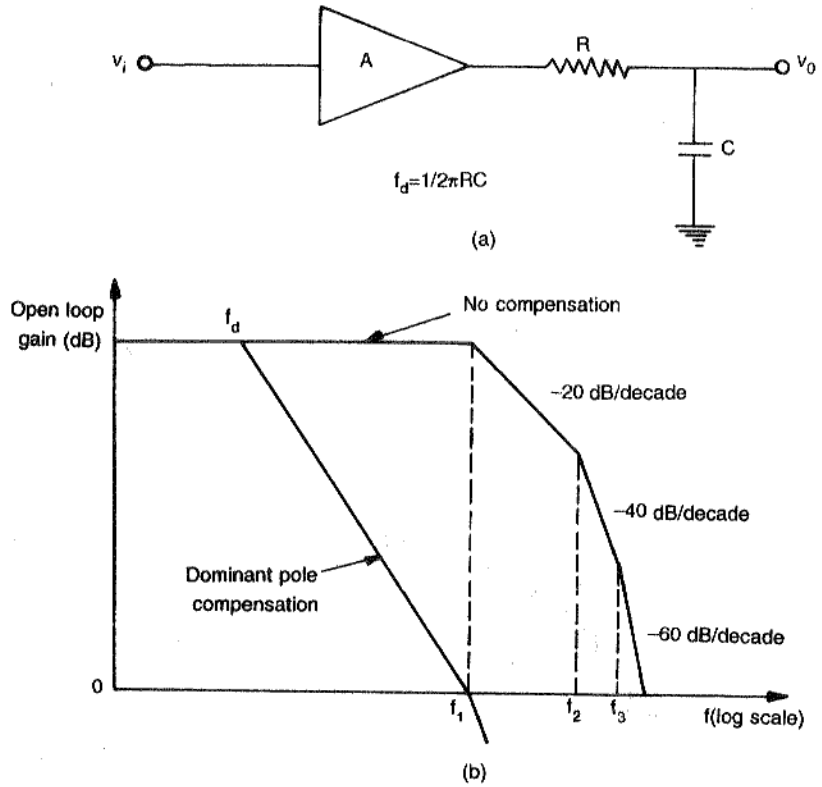


Fig. 3.8 (a) Dominant pole compensation (b) Gain vs frequency curve for dominant pole compensation

Pole-zero Compensation: Here the uncompensated transfer function A is altered by adding both pole and a zero as shown in Fig. 3.9 (a). The zero should be at higher frequency than pole. The transfer function of the compensating network alone is,

$$\frac{v_o}{v_2} = \frac{Z_2}{Z_1 + Z_2} = \frac{R_2}{R_1 + R_2} \frac{1 + j\dfrac{f}{f_1}}{1 + j\dfrac{f}{f_0}} \tag{3.47}$$

where $Z_1 = R_1$, $Z_2 = R_2 + \dfrac{1}{j\omega C_2}$, $f_1 = \dfrac{1}{2\pi R_2 C_2}$, $f_0 = \dfrac{1}{2\pi(R_1 + R_2)C_2}$

The compensating network is designed to produce a zero at the first corner frequency f_1 of the uncompensated transfer function A. This zero will cancel the effect of the pole at f_1. The pole of the compensating network at $f_0 = \omega_0/2\pi$ is selected so that the compensated transfer function A' passes through 0 dB at the second corner frequency f_2 of the uncompensated transfer function A in Eq. (3.31). The frequency can be found graphically by having A' pass through 0 dB at the frequency f_2 with a slope of –20 dB/decade as shown in Fig. 3.9 (b). Assuming that the compensating network does not load the amplifier, i.e. $R_2 >> R_1$, then the overall transfer function becomes.

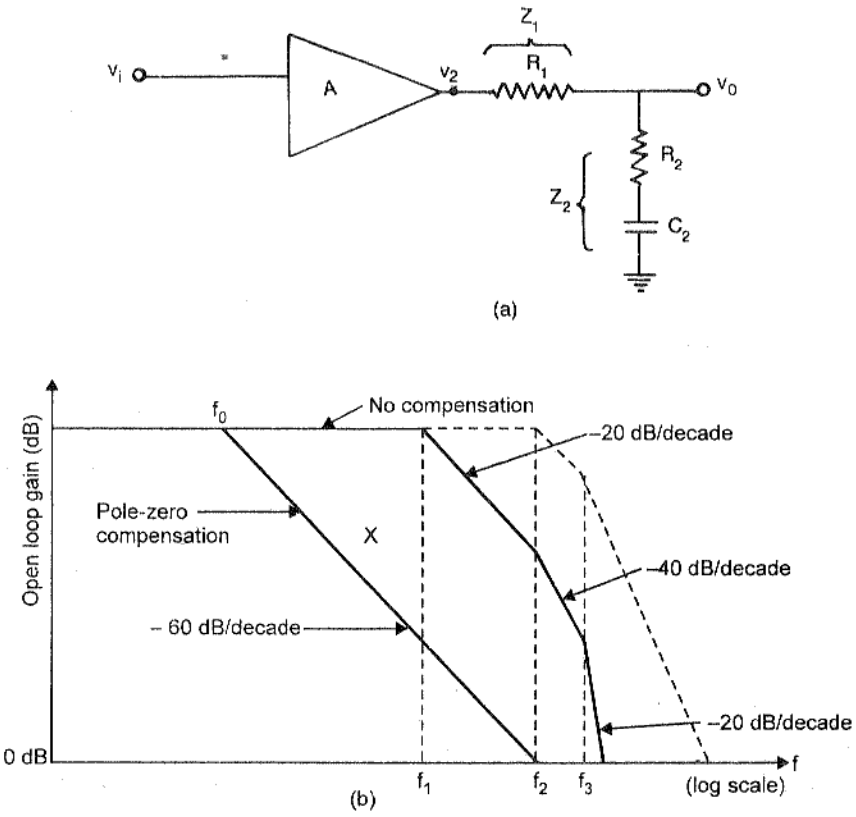


Fig. 3.9 (a) Pole-zero compensation (b) Open loop gain vs. frequency for pole-zero compensation

$$A' = \frac{v_o}{v_i} = \frac{v_o}{v_2} \cdot \frac{v_2}{v_i} = A \cdot \frac{R_2}{R_1 + R_2} \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_o}}$$

$$= \frac{A_{OL}}{\left(1 + j\frac{f}{f_1}\right)\left(1 + \frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \cdot \frac{R_2}{R_1 + R_2} \frac{1 + j\frac{f}{f_1}}{1 + j\frac{f}{f_o}}$$

$$= \frac{A_{OL}}{\left(1 + j\frac{f}{f_o}\right)\left(1 + j\frac{f}{f_2}\right)\left(1 + j\frac{f}{f_3}\right)} \qquad (3.48)$$

with $0 < f_o < f_1 < f_2 < f_3$

and note that $R_2 >> R_1$, so that $\frac{R_2}{R_1 + R_2} \approx 1$.

Consider again the frequency response (Bode plot) for the uncompensated op-amp having three poles at frequencies f_1, f_2 and f_3. Now select R_2 and C_2 so that the zero of the compensating network is equal to the pole at the frequency f_1 (lowest). If there had been no pole added by the compensating network, the response would have changed to that of the dotted curve. However, because of the predominance of the pole of the compensating network at f_o, the rate of closure will be – 20 dB/decade throughout as shown in the curve *X* of Fig. 3.9 (b). The pole at f_o should be selected so that the –20 dB/decade fall should meet the 0-dB line at f_2 which is the second pole of *A*.

A comparison of dominant pole and pole-zero compensation technique is shown in Fig. 3.10. The dominant pole is selected so that the compensated transfer function goes through 0-dB at the first pole f_1 of the uncompensated system. In pole-zero compensation, the zero is chosen at f_1 and pole is selected so that the modified transfer function goes through 0-dB at the second pole f_2 of uncompensated transfer function. The improvement in bandwidth is clearly shown in Fig. 3.10 and is given by $(f_2 - f_1)$.

With either type of compensation, the value of the compensating capacitance is too large to be easily built into standard integrated circuit and as a result, many IC op-amps have internal connections brought out to allow attachment of an external compensating network. However, recently, several op-amps have become available with built-in lag compensation which is accomplished by making use of Miller effect to generate large capacitance needed from fixed small capacitance which can be built into the IC.

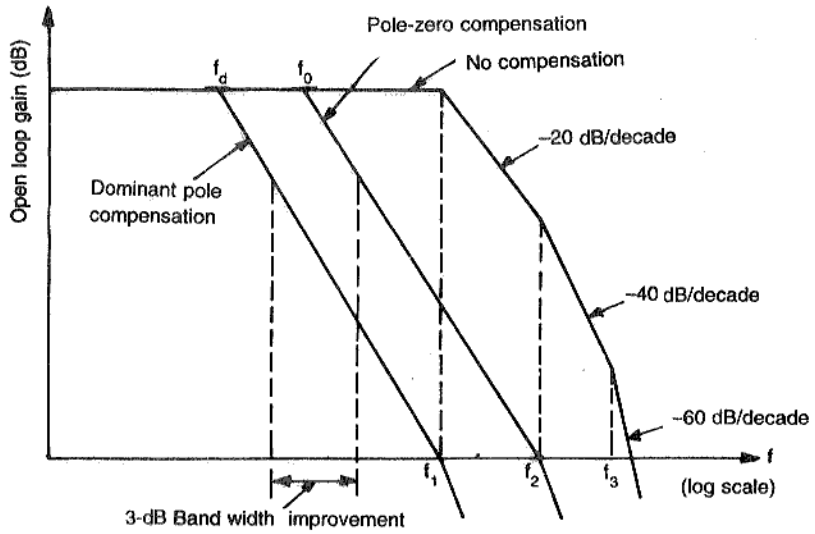


Fig. 3.10 Comparison of dominant pole and pole-zero techniques

Internally Compensated Operational Amplifier

Sometimes, the relatively broad bandwidth of the uncompensated op-amp is not needed. For example, in the instrumentation circuit, the op-amp required is to amplify relatively slow changing signals and therefore it does not require good high-frequency response. In this and similar applications, internally compensated op-amps can be used. They are sometimes called compensated op-amps. Also they are stable regardless of the value of closed-loop gain and without externally connected compensating components. The type 741 op-amp is compensated and has an open-loop gain vs frequency response as shown in Fig. 3.11. The op-amp IC 741 contains a capacitance C_1 of 30 pF (see Fig. 2.22 (a)) that internally shunts off signal current and thus reduces the available output signal at higher frequencies. This internal capacitance, which is an internal compensating component, causes the open-loop gain to roll-off at –20 dB/decade rate and thus assures for a stable circuit. The 741 op-amp has a 1 MHz gain-bandwidth product. This means that the product of the coordinates, gain and frequency of any point on the open-loop gain vs frequency curve is about 1 MHz. If 741 op-amp is wired for a closed-loop gain of 10^4 or 80 dB, its bandwidth is 100 Hz as can be seen by projecting to the right from 10^4 in the curve of Fig. 3.11. For gain of 10^2, the bandwidth increases to 10 kHz and for gain 1, the bandwidth is 1 MHz. For 741 op-amp, unity gain-bandwidth product is specified as 1 MHz in the data sheet. This simply means that op-amp 741 has 1 MHz bandwidth with unity gain as seen in Fig. 3.11. Some internally compensated op-amps are Fairchild's μA 741, National Semiconductor's LM741, LM107 and LM112 and Motorola's MC1558.

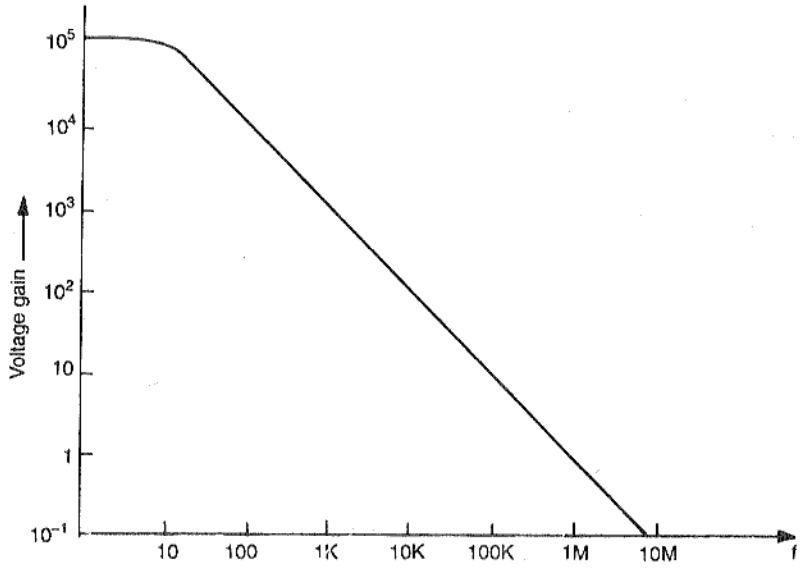


Fig. 3.11 Frequency response of μA741 op-amp

3.3.4 Slew Rate

The rise time of an amplifier is defined as the time the output takes to change from 10 to 90 percent of the final value for a step input and is given as 0.35/BW, where BW is the bandwidth of the amplifier. Ideal response time should be zero second as BW is infinite for ideal op-amp, that is, output voltage should respond instantaneously to any change in the input. Rise time is usually specified for small signals, usually when the peak output voltage is less than one volt. However, for large signal output (i.e., $V_m > 1$ volt), the op-amp's speed is limited by slew rate, Manufacturers specify slew rate that gives the circuit designer a good idea of how quickly a given op-amp responds to changes of input voltage. An op-amp's slew rate is related to its frequency response. Usually op-amps with wide bandwidth will have higher (better) slew rates.

The slew rate is defined as the maximum rate of change of output voltage caused by a step input voltage and is usually specified in V/μs. For example, a 1V/μs slew rate means that the output rises or falls by 1 V in one microsecond. An ideal slew rate is infinite which means that op-amp's output voltage should change instantaneously in response to input step voltage. Practical IC op-amps have specified slew rates from 0.1 V/μs to well above 1000 V/μs. Slew rate listed in the data sheet is usually specified for unity gain and no load. The slew rate improves with higher closed loop gain and dc supply voltage. It is also a function to termperature and generally decreases with an increase in temperature.

What causes slew rate? There is usually a capacitor within or outside an op-amp to prevent oscillation. It is this capacitor which prevents the output voltage from responding immediately to a fast changing input. The rate at which the voltage across the capacitor v_c increases is given by,

$$\frac{dv_c}{dt} = \frac{I}{C} \tag{3.49}$$

Here, I is the maximum current furnished by op-amp to the capacitor C. This means that for obtaining faster slew rate, op-amp should have either a higher current or a small compensating capacitor. For the 741 C, the maximum internal capacitor charging current is limited to about 15 μA. So the slew rate (SR) of 741 C is,

$$SR = \left.\frac{dv_c}{dt}\right|_{max} = \frac{I_{max}}{C} = \frac{15\ \mu A}{30\ pF} = 0.5\ V/\mu s$$

Slew rate limits the response speed of all large signal waveshapes. For a sine wave input, the effect of slew rate limiting can be calculated as follows:

Consider a voltage follower shown in Fig. 3.12 (a). The input is large amplitude, high frequency sine wave.

If $v_s = V_m \sin \omega t$

Then, output $v_o = V_m \sin \omega t$

Figure 3.12 (b) shows the input-output waveform.

The rate of change of the output is given by,

$$\frac{dv_o}{dt} = V_m\, \omega \cos \omega t$$

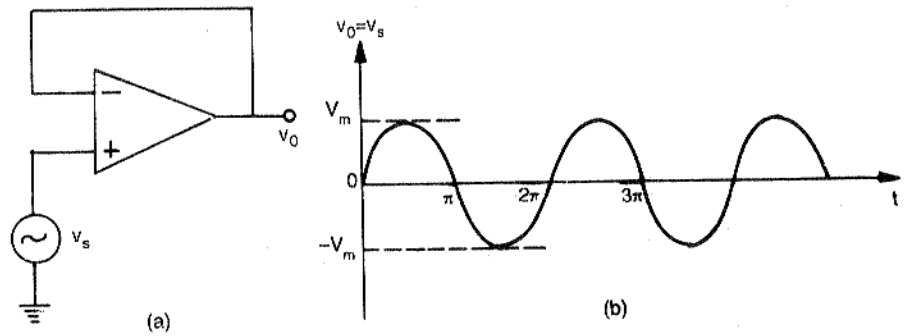


Fig. 3.12 (a) Voltage follower (b) Input/output waveform

The maximum rate of change of the output occurs when cos $\omega t = 1$. That is,

$$SR = \left.\frac{dv_o}{dt}\right|_{max} = \omega V_m$$

Therefore, Slew Rate $= 2\pi f V_m$ V/s

$$= \frac{2\pi f V_m}{10^6} \text{ V/}\mu\text{s}$$

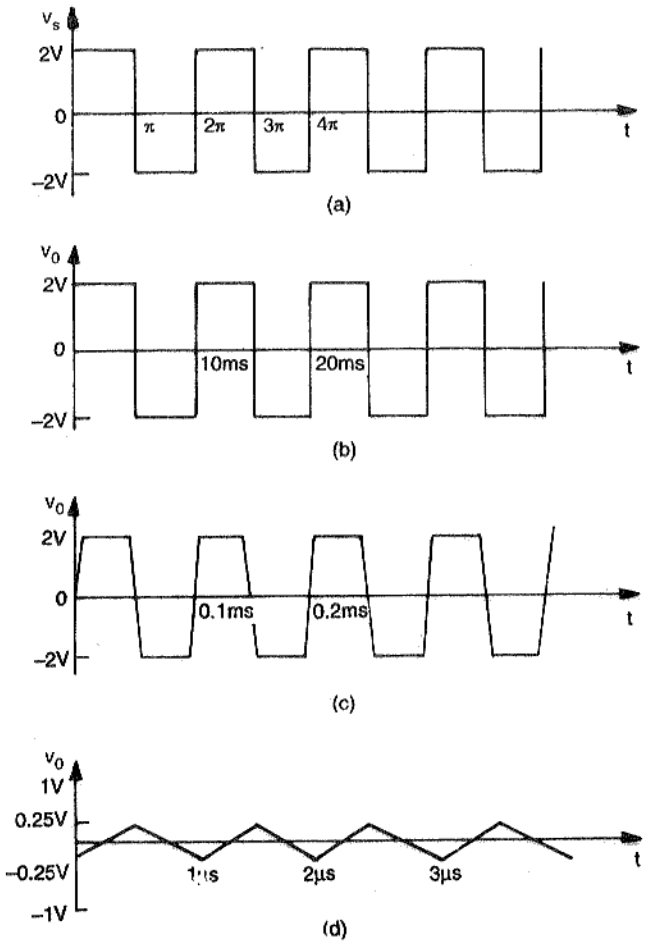


Fig. 3.13 (a) Voltage follower using op-amp with slew rate 1V/µs (b) square wave voltage signal applied (c) output for input frequency of 100 Hz (d) output for input frequency of 100 kHz (e) output for input frequency of 1 MHz

Thus the maximum frequency f_{max} at which we can obtain an undistorted output voltage of peak value V_m is given by,

$$f_{max} \text{ (Hz)} = \frac{\text{Slew Rate}}{6.28 \times V_m}$$

This f_{max} is also called the full power response. It is the maximum frequency of a large amplitude sine wave with which op-amp can have without distortion.

A less than ideal slew rate causes remarkable distortion for non-sinusoidal waveform of higher frequencies. Figure 3.13 shows typical waveforms of a voltage follower with square waves of various frequencies applied as input. The op-amp has a slew rate of 1 V/µs. The output gets worst due to limited slew rate as frequency increases. A 100 Hz square wave input produces a distortionless output as shown in Fig. 3.13 (b). And, a 10 kHz square wave gets distorted as shown in Fig. 3.13 (c). However, due to the limited slew rate, the square wave input of 1 MHz becomes distorted into sawtooth as in Fig. 3.13 (d). This has occurred because of the predominance of capacitance present in the circuit at higher frequencies, RC pairs are in cascade and the time constants are high compared to the high frequency square wave input and the resultant output is obviously a sawtooth waveform of smaller amplitude.

Example 3.4

The output of an op-amp voltage follower is a triangular wave as shown in Fig. 3.14 for a square wave input of frequency 2 MHz and 8V peak to peak amplitude. What is the slew rate of the op-amp?

Solution

Since slew rate is defined as the maximum rate of change of the output, so from Fig. 3.14, it can be seen that,

$$SR = \frac{6 \text{ V}}{(0.5/2)\,\mu\text{s}} = 14 \text{ V/}\mu\text{s}$$

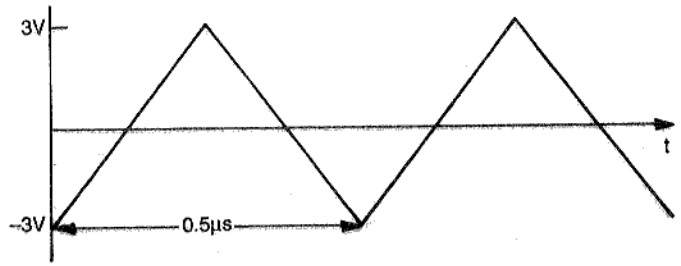


Fig. 3.14 Output waveform of Example 3.4

Example 3.5

A 741C op-amp is used as an inverting amplifier with a gain of 50. The voltage gain vs frequency curve of 741C is flat upto 20 kHz. What maximum peak to peak input signal can be applied without distorting the output.

Solution

The slew rate for 741C is 0.5 V/μs, so maximum output voltage at 20 kHz, is

$$0.5 = \frac{(2\pi)(20 \times 10^3)(V_m)}{10^6}$$

$$V_m = 3.98 \text{ V peak}$$

or, $$V_o = 7.96 \text{ V peak to peak.}$$

Hence, for the output to be undistorted sine wave, the maximum input signal should be less than

$$\frac{7.96}{50} = 159 \text{ mV peak to peak.}$$

Example 3.6

A square wave of peak to peak amplitude of 500 mV has to be amplified to a peak-to-peak amplitude of 3 volts, with a rise time of 4 μs or less. Can a 741 be used?

Solution

Since the output has a peak amplitude greater than 1 volt, the slew rate is the limiting factor. The required slew rate = $\frac{\Delta v}{\Delta t}$. From the definition of rise time, the change in the output voltage Δv in 4 μs is equal to

$$(0.9 - 0.1)\ 3V = 2.4 \text{ V}$$

Therefore, $$SR = \frac{2.4 \text{ V}}{4 \text{ μs}} = 0.6 \text{ V/μs}$$

Since the slew rate of 741 is 0.5 V/μs, it is too slow and cannot be used.

3.4 ANALYSIS OF DATA SHEETS OF AN OP-AMP

The manufacturers supply data sheets for the ICs they produce. These data sheets provide information regarding pin diagram, absolute maximum ratings, electrical characteristics, equivalent circuit of the devices etc. In this section, significance of the electrical parameters supplied in a typical op-amp data sheet is discussed.

Figure 3.15 gives the data sheet for a Fairchild μA741 op-amp. 741 series are available in models 741, 741A, 741C and 741E. The schematic diagram and electrical parameters for all these models are the same with only the values of the parameters differing from one model to another. We will consider specifications for 741C op-amp.

From the data sheet it can be seen that:

1. 741 is internally frequency compensated op-amp.
2. 741 is a monolithic IC fabricated using planar epitaxial process.
3. It is useful for integrator, summer, voltage follower and other feedback applications.
4. Absolute maximum ratings are specified for supply voltage, internal power dissipation, differential input voltage, input voltage, storage and operating temperature ranges, soldering pin temperature and output short circuit duration.
5. 741 is available in all three packages viz 8-pin metal can, 10-pin flat pack and 8 or 14 pin DIP. The pin diagrams for all these packages are shown in the data sheet.
6. For 741C, two sets of electrical specifications are available, one set is applicable at room temperature (25°C) and other set applies to the commercial temperature range (0° to + 70°C). As we are interested only in showing the significance of the parameters listed, we limit the discussion to only one model, that is 741C at 25°C.

The various electrical parameters supplied in the data sheet are as follows:

Input offset voltage: It is the voltage that must be applied between the input terminals of an op-amp to nullify the output. Since this ···age could be positive or negative its absolute value is listed on the ···a sheet. For 741C, the maximum value is 6 mV.

Input offset current: The algebraic difference between the currents into the (–) input and (+) input is referred to as input offset current. It is 200 nA maximum for 741C.

Input bias current: The average of the currents entering into the (–) input and (+) input terminals of an op-amp is called input bias current. Its value is 500 nA for 741C.

Input resistance: This is the differential input resistance as seen at either of the input terminals with the other terminal connected to ground. For the 741C, the input resistance is 2 MΩ.

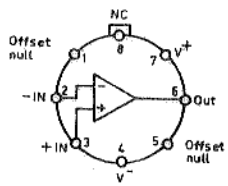
Input capacitance: It is the equivalent capacitance that can be measured at either of the input terminal with the other terminal connected to ground. A typical value of C_i is 1.4 pF.

Offset voltage adjustment range: special feature of the 741 family op-amp is the provision of offset voltage null capability. For

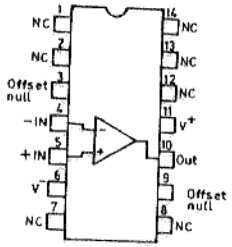
General Description: The μA741 is a high performance monolithic operational amplifier constructed using the planer epitaxial process. High common mode voltage range and absence of latch-up tendencies make the μA741 ideal for use as voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier and general feedback applications.

*No frequency compensation required
*Short circuit protection
*Offset voltage null capability
*Large common mode and differential voltage ranges
*Low power consumption
*No latch-up

8 Pin Mini Metal Can
(top view)



10 Pin DIP
(top view)

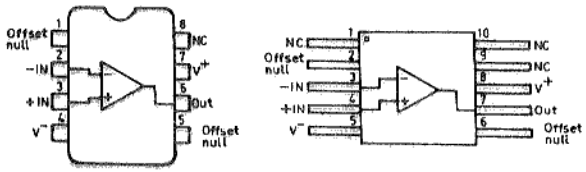


Absolute Maximum Ratings

Supply voltage	
μA741A, μA741, μA741E	± 22 V
μA741C	± 18 V
Internal Power Dissipation	
Metal Can	500 m W
Molded and Hermetic DIP	670 m W
Mini DIP	310 m W
Flatpack	570 m W
Differential Input Voltage	± 30 V
Input Voltage	± 15 V
Operating temperature Range	
Military (μA741A, μA741)	– 55 °C to 125 °C
Commercial (μA741E, μA741C)	0 °C to 70 °C

8 Pin Mini DIP
(top view)

10 Pin Flatpak
(top view)



μA741C

Electrical Characteristics V_s = ±15 V, T_A = 25°C unless otherwise specified

CHARACTERISTICS (see definitions)		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_s \leq 10$ kΩ		20		mV
Input Offset Current			20	200	nA	
Input Bias Current			80	500	nA	
Input Resistance		0.3	2.0		MΩ	
Input Capacitance			1.4		pF	
Offset Voltage Adjustment Range			± 15		mV	
Input Voltage Range		± 12	± 13		V	
Common Mode Rejection Ratio		$R_s \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio		$R_s \leq 10$ kΩ		30	150	μV/V
Large Singal Voltage Gain		$R_L \geq$ kΩ, V_{out} = ± 10V		20,000	200,000	
Output Voltage Swing		$R_L \geq 10$ kΩ	± 12	± 14		V
		$R_L \geq 2$ kΩ	± 10	± 13		V
Output Resistance				75	Ω	
Output Short Circuit Current				25	mA	
Supply Current				1.7	2.8	mA
Power Consumption				50	85	mW
Transient Response (unity Gain)	Rise Time	V_{in} = 200 mV, R_L = 2kΩ			0.3	μs
	Overshoot	C_L = 100 pF			6.0	%
Slew Rate		$R_L \geq 2$ kΩ			0.5	V/μs

Fig. 3.15 Data Sheet of μA 741

this refer to Sec. 3.2.4. For 741C offset voltage adjustment range is ± 15 mV.

Input voltage range: This is the common-mode voltage that can be applied to both input terminals without disturbing the performance of an op-amp. For the 741 C, the range of the input common-mode voltage is ± 13 V. Common-mode configuration is used only for test purpose to determine the degree of matching between the inverting and non-inverting terminals.

Common-mode rejection ratio: It has been discussed in detail in Sec. 2.3.7. For 741C, CMRR is typically 90 dB. CMRR is usually measured under the test condition that the input source resistance $R_s \leq 10$ kΩ. The higher the value of CMRR, better is the matching between the two input terminals and smaller the output common-mode voltage.

Supply voltage rejection ratio: The change in an op-amp's input offset voltage due to variations in supply voltage is called the supply voltage rejection ration (SVRR). Some manufacturers use terms like power supply rejection ratio (PSRR) or power supply sensitivity (PSS). These terms are expressed in microvolts per volt or in decibels. For 741C, SVRR = 150 μV/V. Obviously, lower the value of SVRR, better the op-amp.

Large signal voltage gain: An op-amp amplifies the difference voltage between the two input terminals and, therefore, its voltage gain is defined as,

$$\text{Voltage gain} = \frac{\text{output voltage}}{\text{differential input voltage}}$$

Since the amplitude of the output signal is much larger than the input signal, the voltage gain is commonly referred as large signal voltage gain. For 741C, typical value is, 2,00,000 under test conditions, $R_L \geq 2$ kΩ and $V_o = \pm 10$ V.

Output voltage swing: The output voltage swing indicates the value of positive and negative saturation voltages of an op-amp, and never exceeds the supply voltage V^+ and V^-. For 741C, the output voltage swing is guaranteed to be between +13 V and –13 V for $R_L \geq$ 2 kΩ.

Output resistance: Output resistance R_o is the resistance measured between the output terminal of the op-amp and the ground. It is 75 Ω for the 741C op-amp.

Output short circuit current: This is the current that may flow if an op-amp gets shorted accidentally and is generally high. The op-amp must be provided with short circuit protection. The short circuit

current I_{sc} for 741C is 25 mA. This means that the built-in short circuit protection is guaranteed to withstand 25 mA of current.

Supply current: Supply current I_s is the current drawn by the op-amp from the power supply. It is 2.8 mA for 741C.

Power consumption: This gives the amount of quiescent power (V_i = 0V) that must be consumed by the op-amp so as to operate properly. It is 85 mW for 741C.

Transient response: The rise time and overshoot are the two characteristics of the transient response of any circuit. These parameters are of importance whenever selecting an op-amp for ac applications. The transient response test circuit is included in the data sheet. For 741C, rise time is 0.3 μs and overshoot is 5%.

Slew rate: This is another parameter of importance whenever selecting an op-amp for high frequency applications. It has been discussed in detail in Sec.3.3.4. Op-amp 741C has a low slew rate (0.5 V/μs) and therefore cannot be used for high frequency applications.

Summary

1. A practical op-amp is not ideal and has finite values of input offset voltage, input offset current and input bias current. These produce a dc offset voltage at the output.
2. Input bias-current is the dc current necessary to flow into the inputs of op-amp to turn it ***on***. The effect of input bias currents can be reduced by using compensating resistor R_{comp}.
3. Input offset current results due to non-identical transistors and is minimized by using a T-network in the feedback path.
4. Input offset voltage can be nulled by using external balancing techniques.
5. The input offset voltage and current drift with the change in temperature, thereby producing a dc error voltage in the output.
6. The gain of an op-amp decreases (rolls-off) at high frequencies because of capacitances within an op-amp.
7. The open-loop gain of the op-amp decreases at the rate of –20 dB/decade or –6 dB/octave at each break frequency.
8. An open-loop op-amp gives very small bandwidth. Feedback increases the bandwidth but may cause instability.
9. For a stable circuit, the additional phase angle provided by op-amp must be less than 180° when its magnitude reaches unity.
10. Compensating networks are used to control the phase shift and hence improve the stability.
11. External compensation is done either by pole compensation or pole-zero compensation.

12. Internally compensated op-amps are also available but give smaller bandwidth.
13. Large signal output (> 1V) is limited by the speed at which the op-amp can charge compensating capacitor. This is called slew rate and is expressed in volts per micro-second.
14. The manufacturers supply data sheets for the ICs they produce. The data sheet gives pin diagrams, equivalent circuits, absolute maximum ratings, electrical characteristics and typical applications of the device.

Review Questions

3.1. List the non-ideal dc characteristics of an op-amp.
3.2. Why do we use R_{comp} resistor?
3.3. Why is R_{comp} not needed in differential amplifier?
3.4. How is input offset voltage compensated for?
3.5. What produces more offset voltage at the output: input offset current or input bias current?
3.6. Define thermal drift.
3.7. List the parameters that are important for ac applications.
3.8. What does the term roll-off mean?
3.9. What is Bode plot?
3.10. What problem can occur with an amplifier with a steep gain roll-off?
3.11. Why are low closed loop gains avoided with uncompensated op-amps?
3.12. If an op-amp is specified as being compensated, what does this mean?
3.13. If closed loop gain of an op-amp is increased, what happens to bandwidth.
3.14. If the gain-bandwidth product of an op-amp is 2 MHz, what is its bandwidth when connected as a voltage follower?
3.15. Define slew rate. What causes the slew rate?
3.16. How is the slew rate measured?
3.17. What is the effect of operation frequency on the maximum unclipped output signal capability of an op-amp.
3.18. List and explain the parameters given in manufacturer's data sheet of an op-amp.
3.19. The dc open loop gain of an op-amp is 100,000. What will be the open loop gain at its break frequency?
3.20. The transient response rise time (*unity gain*) of an op-amp is 0.07 μs. Find the small signal band width.
3.21. What is the difference between the open loop and closed loop gain of an op-amp.
3.22. Does increasing the compensating capacitor increase or decease unity-gain band-width.

3.23. How fast can the output of an op-amp change by 10 V, if its slew rate is 1V/μs.

3.24. Find the maximum frequency for a sine wave output voltage of 10 V peak with an op-amp whose slew rate is 1V/μs.

PROBLEMS

3.1. A 741 op-amp is used as an inverting amplifier shown in Fig. 3.2 (c) with R_1 = 1 kΩ and R_f = 100 kΩ. What is the maximum output offset voltage caused by the input offset voltage V_{os}. For 741, V_{os} = 6 mV.

3.2. Repeat Problem 3.1, if op-amp used is LM 307 with V_{os} = 10 mV; R_1 = 100 Ω and R_f = 4.7 kΩ.

3.3. In an inverting amplifier of the type shown in Fig. 3.2 (c), R_1 = 100 kΩ, R_f = 10 MΩ. Calculate (i) maximum output offset voltage caused by the input offset voltage V_{os}; (ii) maximum output offset voltage caused by the input bias current I_B. The op-amp used is 741 with V_{os} = 6 mV; I_B = 500 nA.

3.4. In problem 3.3, calculate the value of R_{comp} needed to eliminate the effect of input bias current.

3.5. In an inverting amplifier R_1 = 1 kΩ, R_f = 100 kΩ. The op-amp has the following specifications:

$$\frac{\Delta V_{os}}{\Delta T} = 30\ \mu V/°C \text{ max}$$

$$\frac{\Delta I_{os}}{\Delta T} = 0.3\ nA/°C \text{ max}$$

Assume that the amplifier is nulled at 25°C. Calculate the value of the error voltage and the output voltage V_o at 35°C, if (i) V_i = 1 mV dc; (ii) V_i = 5 mV dc.

3.6. Repeat Problem 3.5, for a non-inverting amplifier.

3.7. The LM312 op-amp is used as an inverting amplifier with the following specifications:

$$\frac{\Delta V_{os}}{\Delta T} = 30\ \mu V/°C;\ \frac{\Delta I_{os}}{\Delta T} = 10\ nA/°C$$

$$R_1 = 1\ k\Omega;\ R_f = 4.7\ k\Omega.$$

Assume that the amplifier is nulled at 25°C. A sine wave of 10 mV peak amplitude at 100 Hz is applied. Draw the output voltage waveform at 25°C and 45°C.

3.8. Repeat Problem 3.7 for a non-inverting amplifier.

3.9. (a) An op-amp has a slew rate of 2 V/μs. What is the maximum frequency of an output sinusoid of peak value 5 V at which distortion sets in due to the slew rate limitation.

(b) If a sinusoid of 10 V peak is specified, what is the full power bandwidth?

3.10. An op-amp has a slew rate of 2V/μs. Find the rise time for an output voltage of 10 V amplitude resulting from a rectangular pulse input if the op-amp is slew rate limited.

Experiment 3.1

To measure (a) input bias current, (b) input offset current and (c) input offset voltage of the given op-amp.

Procedure

(a) Set up the circuit shown in Fig. E. 3.1 (a) to measure I_B^- (inverting input bias current) and Fig. E. 3.1 (b) to measure I_B^+ (non-inverting input bias current). Select a large resistor (in MΩ) and measure the output voltage. Calculate $I_B^- = V_o/R_f$ and $I_B^+ = V_o R$.

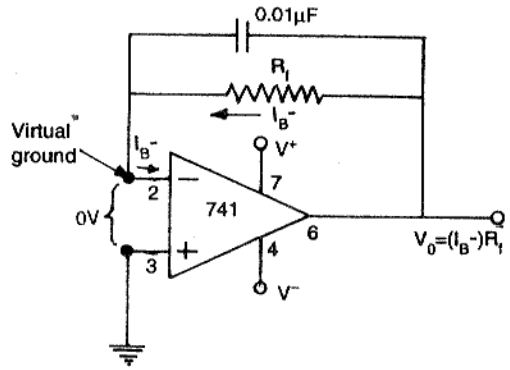


Fig. E.3.1 (a) Measurement of inverting input bias current

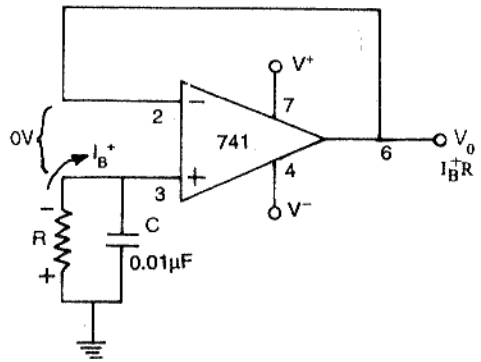


Fig. E. 3.1 (b) Measurement of non-inverting input bias current

(b) Offset current may be measured by the circuit shown in Fig. E.3.1 (c). The use of the equal resistors cancel the effect of the bias current. The offset current $I_{os} = V_o/R_f$.

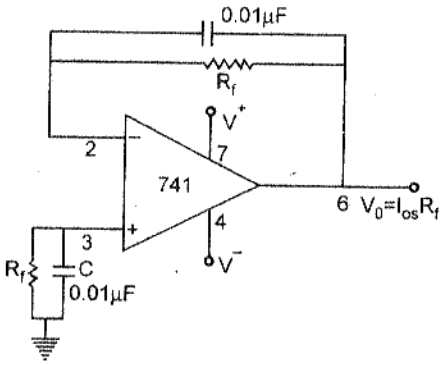


Fig. E. 3.1 (c) Offset current measurement

(c) To measure input offset voltage, set up the circuit shown in Fig. E. 3.1 (d). The effect of the bias current is compensated by R_{comp}. The output voltage is given by,

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_{os} + I_{os} R_f$$

$$\simeq \left(1 + \frac{R_f}{R_1}\right) V_{os}$$

The value of V_{os}, so obtained gives typically 98 percent accuracy.

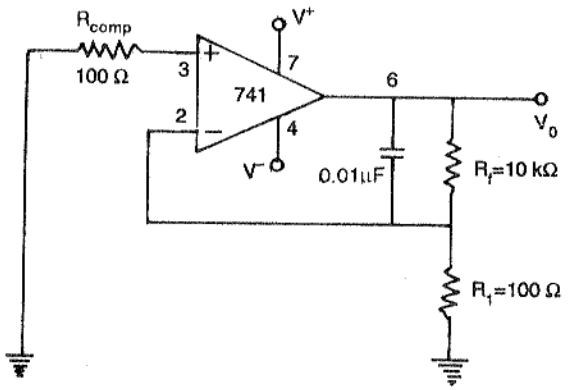


Fig. E.3.1 (d) Offset voltage measurement

Experiment 3.2

To measure the slew rate of the 741C op-amp.

Procedure

1. Connect the op-amp as shown in Fig. E.3.2.

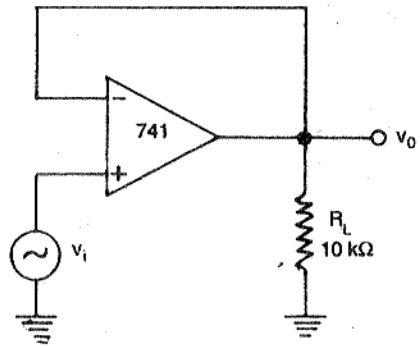


Fig. E. 3.2 Voltage follower to measure slew rate

2. Adjust the input sine-wave signal generator so that the output is 1 V peak sine wave at 1 kHz.
3. Slowly increase the input signal frequency until the output gets just distorted.
4. Calculate slew rate, $SR = \frac{2\pi f V_m}{10^6}$ V/μs where V_m = peak output amplitude in volts and f = frequency in Hz.
5. Now give a square-wave input and repeat step 2.
6. Increase the input frequency slowly until the output is just barely a triangular wave. The slew rate,

$$SR = \frac{\Delta v_o}{\Delta t} \text{ V/μs}$$

where, Δv_o = change in the output voltage amplitude in volts.
Δt = time required for Δv_o in μs.

4

Operational Amplifier Applications

4.1 INTRODUCTION

We have already discussed the electronics of op-amp, its dc and ac characteristics, parameter limitations and various configurations. Now we take a look at the applications of an op-amp. As we shall see, op-amp has countless applications and forms the basic building block of linear and non-linear analog systems. In linear circuits, the output signal varies with the input signal in a linear manner. Some of the linear applications discussed in this chapter are: adder, subtractor, voltage to current converter and current to voltage converter, instrumentation amplifier, analog computation, power amplifier etc.

There is another class of circuits with highly non-linear input to output characteristics. Rectifier, peak detector, clipper, clamper, sample and hold circuit, log and antilog amplifier, multiplier are the various non-linear circuits discussed. These non-linear circuits are very useful in industrial instrumentation, communication and general signal processing.

4.2 BASIC OP-AMP APPLICATIONS

Scale Changer/Inverter

In the basic inverting amplifier of Fig. 4.1, if the ratio $R_f/R_1 = K$, where K is a real constant, then the closed loop gain $A_{CL} = -K$. The circuit thus could be used to multiply by a constant factor if R_f and R_1 are selected as precision resistors. For $R_f = R_1$, $A_{CL} = -1$ and the circuit is called an inverter, i.e., the output is 180° out of phase with respect to input though the magnitudes are same.

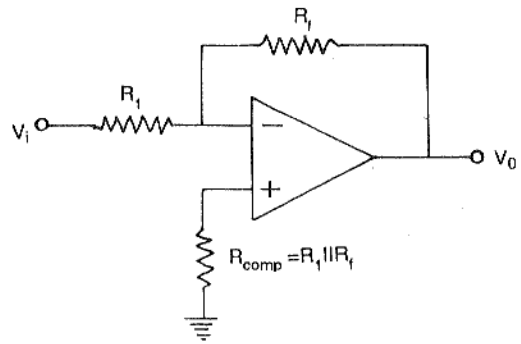


Fig. 4.1 Scale changer for ($R_f/R_1 = K$) and phase inverter for ($R_f/R_1 = 1$)

Summing Amplifier

Op-amp may be used to design a circuit whose output is the sum of several input signals. Such a circuit is called a summing amplifier or a summer. An inverting summer or a non-inverting summer may be obtained as discussed now.

Inverting Summing Amplifier

A typical summing amplifier with three input voltages V_1, V_2 and V_3, three input resistors R_1, R_2, R_3 and a feedback resistor R_f is shown in Fig. 4.2 (a). The following analysis is carried out assuming that the op-amp is an ideal one, that is, $A_{OL} = \infty$ and $R_i = \infty$. Since the input bias current is assumed to be zero, there is no voltage drop across the resistor R_{comp} and hence the non-inverting input terminal is at ground potential.

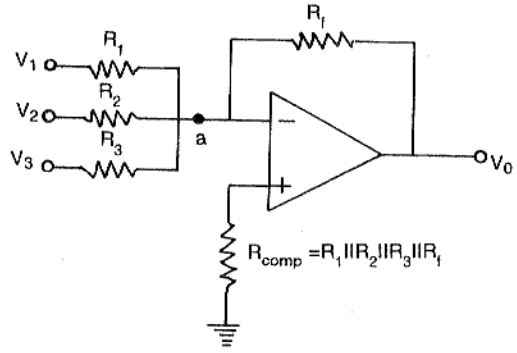


Fig. 4.2 (a) Inverting summing amplifier

The voltage at node 'a' is zero as the non-inverting input terminal is grounded. The nodal equation by KCL at node 'a' is

$$\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}+\frac{V_o}{R_f}=0$$

or,
$$V_o=-\left(\frac{R_f}{R_1}V_1+\frac{R_f}{R_2}V_2+\frac{R_f}{R_3}V_3\right) \tag{4.1}$$

Thus the output is an inverted, weighted sum of the inputs. In the special case, when $R_1 = R_2 = R_3 = R_f$, we have

$$V_o=-(V_1+V_2+V_3) \tag{4.2}$$

in which case the output V_o is the inverted sum of the input signals. We may also set

$$R_1 = R_2 = R_3 = 3R_f$$

in which case

$$V_o=-\left(\frac{V_1+V_2+V_3}{3}\right) \tag{4.3}$$

Thus the output is the average of the input signals (inverted). In a practical circuit, input bias current compensating resistor R_{comp} should be provided as discussed in Sec. 3.2.1. To find R_{comp}, make all inputs $V_1 = V_2 = V_3 = 0$. So the effective input resistance $R_i = R_1 \| R_2 \| R_3$. Therefore, $R_{comp} = R_i \| R_f = R_1 \| R_2 \| R_3 \| R_f$.

Example 4.1

Design an adder circuit using an op-amp to get the output expression as

$$V_o=-(0.1\ V_1+V_2+10\ V_3)$$

where V_1, V_2, and V_3 are the inputs.

Solution

The output in Fig. 4.2 (a) is

$$V_o=-[(R_f/R_1)\ V_1+(R_f/R_2)V_2+(R_f/R_3)V_3]$$

say $R_f = 10\ k\Omega,\ R_1 = 100\ k\Omega,\ R_2 = 10\ k\Omega,\ R_3 = 1\ k\Omega$

Then the desired output expression is obtained.

Non-inverting Summing Amplifier

A summer that gives a non-inverted sum is the non-inverting summing amplifier of Fig. 4.2 (b). Let the voltage at the (–) input terminal be V_a. The voltage at (+) input terminal will also be V_a. The nodal equation at node 'a' is given by

$$\frac{V_1-V_a}{R_1}+\frac{V_2-V_a}{R_2}+\frac{V_3-V_a}{R_3}=0$$

from which we have,

$$V_a=\frac{\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}} \tag{4.4}$$

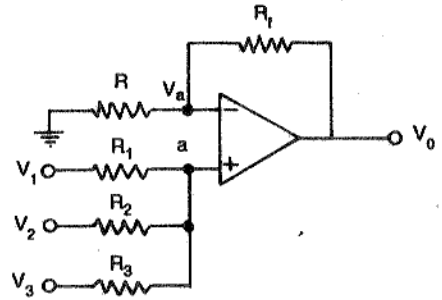


Fig. 4.2 (b) Noninverting summing amplifier

The op-amp and two resistors R_f and R constitute a non-inverting amplifier with

$$V_o=\left(1+\frac{R_f}{R}\right)V_a \tag{4.5}$$

Therefore, the output voltage is,

$$V_o=\left(1+\frac{R_f}{R}\right)\frac{\left(\frac{V_1}{R_1}+\frac{V_2}{R_2}+\frac{V_3}{R_3}\right)}{\frac{1}{R_1}+\frac{1}{R_2}+\frac{1}{R_3}} \tag{4.6}$$

which is a non-inverted weighted sum of inputs.

Let $R_1 = R_2 = R_3 = R = R_f/2$, then $V_o = V_1 + V_2 + V_3$

Subtractor

A basic differential amplifier can be used as a subtractor as shown in Fig. 4.3 (a). If all resistors are equal in value, then the output voltage can be derived by using superposition principle. To find the output V_{o1} due to V_1 alone, make $V_2 = 0$. Then the circuit of Fig. 4.3 (a) becomes a non-inverting amplifier having input voltage $V_1/2$ at the non-inverting input terminal and the output becomes

$$V_{o1}=\frac{V_1}{2}\left(1+\frac{R}{R}\right)=V_1 \tag{4.7}$$

Similarly the output V_{o2} due to V_2 alone (with V_1 grounded) can be written simply for an inverting amplifier as

$$V_{o2} = -V_2 \tag{4.8}$$

Thus the output voltage V_o due to both the inputs can be written as

$$V_o = V_{o1} + V_{o2} = V_1 - V_2 \tag{4.9}$$

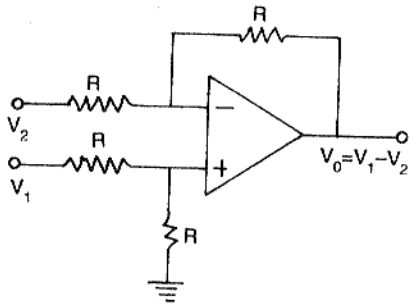


Fig. 4.3 (a) Op-amp as subtractor

Adder-Subtractor

It is possible to perform addition and subtraction simultaneously with a single op-amp using the circuit shown in Fig. 4.3 (b).

The output voltage V_o can be obtained by using superposition theorem. To find output voltage V_{o1} due to V_1 alone, make all other input voltages V_2, V_3 and V_4 equal to zero. The simplified circuit is shown in Fig. 4.3 (c). This is the circuit of an inverting amplifier and its output voltage is,

$$V_{o1} = -\frac{R}{R/2}\frac{V_1}{2} = -V_1 \tag{4.10}$$

(by Thevenin's equivalent circuit at inverting input terminal).

Similarly, the output voltage V_{o2} due to V_2 alone is,

$$V_{o2} = -V_2 \tag{4.11}$$

Now, the output voltage V_{o3} due to the input voltage signal V_3 alone applied at the (+) input terminal can be found by setting V_1, V_2 and V_4 equal to zero. The circuit now becomes a non-inverting amplifier as shown in Fig. 4.3 (d). The voltage V_a at the non-inverting terminal is

$$V_a = \frac{R/2}{R+R/2}V_3 = V_3/3 \tag{4.12}$$

So, the output voltage V_{o3} due to V_3 alone is

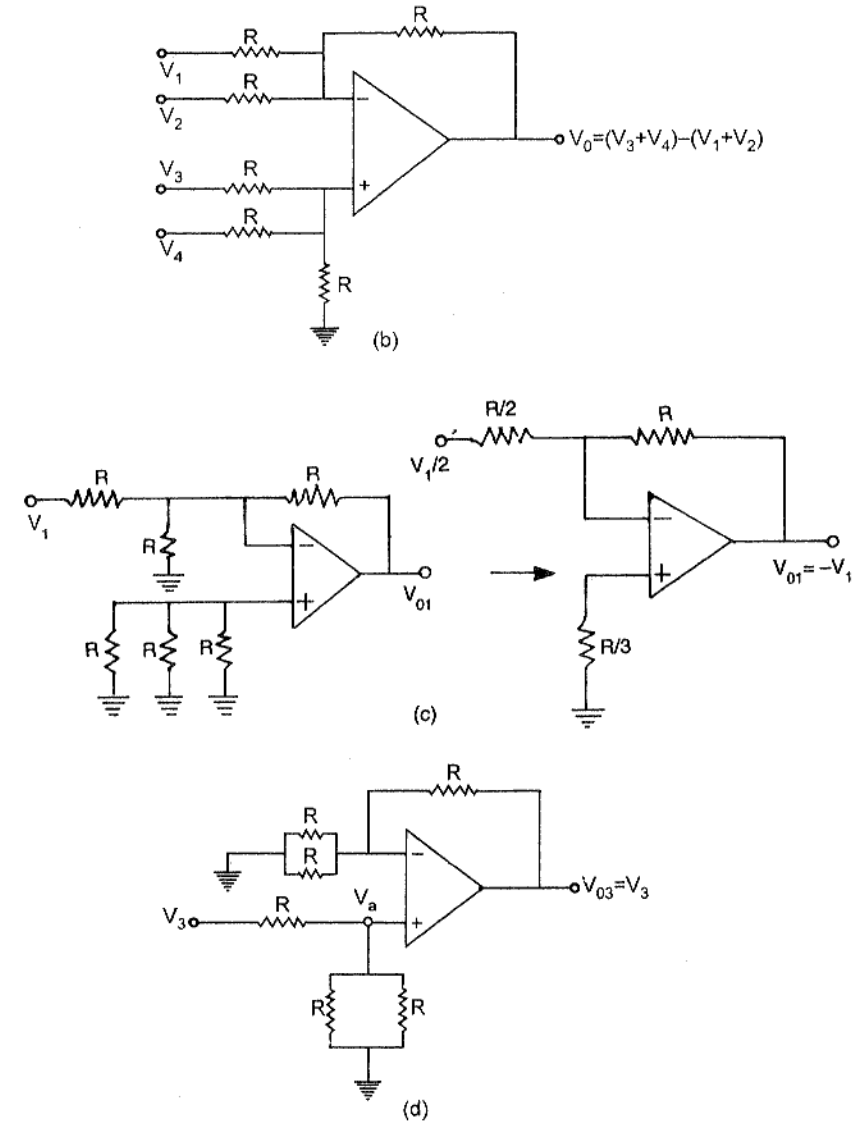


Fig. 4.3 (b) Op-amp adder-subtractor (c) Simplifier circuit for $V_2 = V_3 = V_4 = 0$ (d) Simplified circuit for $V_1 = V_2 = V_4 = 0$

$$V_{o3} = \left(1+\frac{R}{R/2}\right)V_a = 3\left(\frac{V_3}{3}\right) = V_3 \tag{4.13}$$

Similarly, it can be shown that the output voltage V_{04} due to V_4 alone is

$$V_{o4} = V_4 \tag{4.14}$$

Thus, the output voltage V_o due to all four input voltages is given by

$$\begin{aligned} V_o &= V_{o1} + V_{o2} + V_{o3} + V_{o4} \\ &= -V_1 - V_2 + V_3 + V_4 \\ &= (V_3 + V_4) - (V_1 + V_2) \end{aligned} \tag{4.15}$$

So, the circuit is an adder-subtractor.

Example 4.2

Find V_o for the adder-subtractor shown in Fig. 4.4 (a).

Solution

The negative sum is obtained by setting $V_3 = V_4 = 0$. Thus,

$$V_o' = -\frac{50}{40}V_1 - \frac{50}{25}V_2$$

$$= -1.25\ V_1 - 2\ V_2$$

Now set $V_1 = V_2 = 0$ to find the output voltage due to V_3 and V_4. The voltage V_+ at the (+) input terminal due to V_3 and V_4 can be found by using superposition theorem as shown in Fig. 4.4 (b) as

$$V_+ = \frac{12}{10+12}V_3 + \frac{7.5}{20+7.5}V_4$$

or,

$$V_+ = 0.545\ V_3 + 0.273\ V_4$$

The output voltage V_o'' due to V_3 and V_4 now can be determined from the equivalent circuit of Fig. 4.4 (c) as

$$V_o'' = \left(1 + \frac{R'}{R}\right)V_+$$

Here $R' = 50\ \text{k}\Omega$ and $R = 40 \,||\, 25 = 15.38\ \text{k}\Omega$

Therefore,

$$V_o'' = \frac{50 + 15.38}{15.38}(0.545\ V_3 + 0.273\ V_4)$$

$$= 2.32\ V_3 + 1.16\ V_4$$

The total output voltage V_o is given by

$$V_o = V_o' + V_o''$$

$$= -1.25\ V_1 - 2.0\ V_2 + 2.32\ V_3 + 1.16\ V_4$$

Putting the value of V_1, V_2, V_3 and V_4, we get

$$V_o = -1.25 \times 2 - 2.0 \times 3 + 2.32 \times 4 + 1.16 \times 5$$

$$= -2.5 - 6.0 + 9.28 + 5.80$$

$$= 6.58\ \text{V}$$

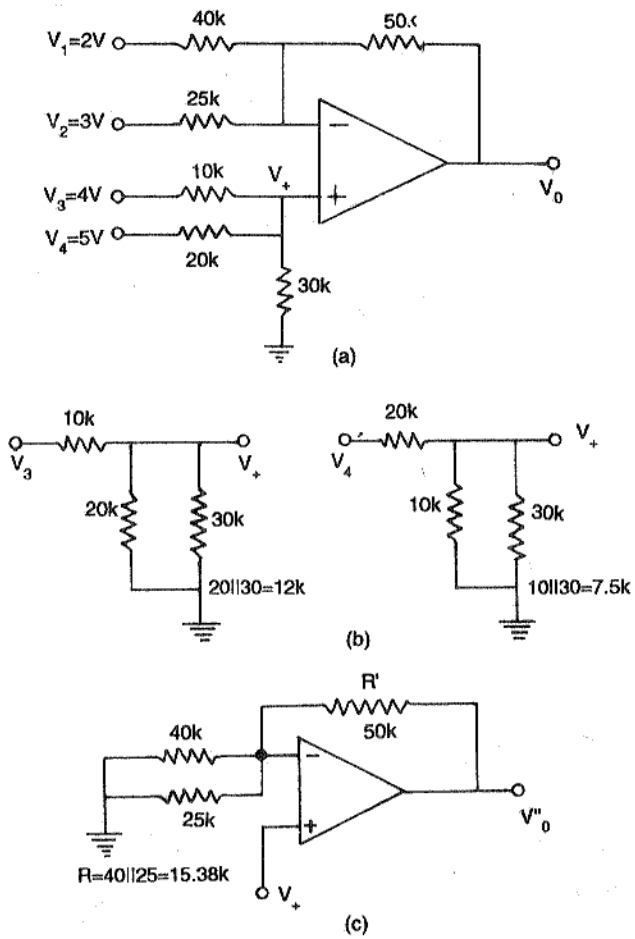


Fig. 4.4 (a) Circuit for Example 4.2. (b-c) Equivalent circuit

4.3 INSTRUMENTATION AMPLIFIER

In a number of industrial and consumer applications, one is required to measure and control physical quantities. Some typical examples are measurement and control of temperature, humidity, light intensity, water flow etc. These physical quantities are usually measured with the help of transducers. The output of transducer has to be amplified so that it can drive the indicator or display system. This function is performed by an instrumentation amplifier. The important features of an instrumentation amplifier are:

(i) high gain accuracy
(ii) high CMRR
(iii) high gain stability with low temperature coefficient
(iv) low dc offset
(v) low output impedance

There are specially designed op-amps such as μA725 to meet the above stated requirements of a good instrumentation amplifier. Monolithic (single chip) instrumentation amplifier are also available commercially such as AD521, AD524, AD624 by Analog Devices, LH0036, LH0037 by National Semiconductor and INA104, 3626, 3629 by Burr-Brown.

Consider the basic differential amplifier shown in Fig. 4.5 (a). It can be easily seen that the output voltage V_o is given by,

$$V_o = -\frac{R_2}{R_1} V_2 + \frac{1}{1+\frac{R_3}{R_4}} V_1 \left(1+\frac{R_2}{R_1}\right)$$

or,
$$V_o = -\frac{R_2}{R_1}\left[V_2 - \frac{1}{1+\frac{R_3}{R_4}}\left(\frac{R_1}{R_2}+1\right)V_1\right] \quad (4.16)$$

For $R_1/R_2 = R_3/R_4$, we obtain

$$V_o = \frac{R_2}{R_1}(V_1 - V_2) \quad (4.17)$$

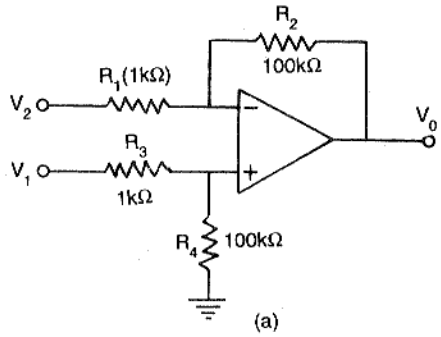
In the circuit of Fig. 4.5 (a), source V_1 sees an input impedance $= R_3 + R_4$ (= 101 kΩ) and the impedance seen by source V_2 is only R_1 (1 kΩ). This low impedance may load the signal source heavily. Therefore, high resistance buffer is used proceeding each input to avoid this loading effect as shown in Fig. 4.5 (b).

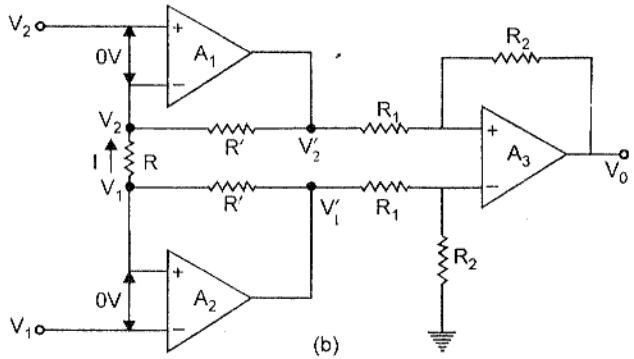
The op-amps A_1 and A_2 have differential input voltage as zero. For $V_1 = V_2$, that is, under common mode condition, the voltage across R will be zero. As no current flows through R and R' the non-inverting amplifier A_1 acts as voltage follower, so its output $V_2' = V_2$. Similarly op-amp A_2 acts as voltage follower having output $V_1' = V_1$. However, if $V_1 \neq V_2$, current flows in R and R', and $(V_2' - V_1') > (V_2 - V_1)$. Therefore, this circuit has differential gain and CMRR more compared to the single op-amp circuit of Fig. 4.5 (a). The output voltage V_o can be calculated as follows:

The voltage at the (+) input terminal of op-amp A_3 is $\frac{R_2 V_1'}{R_1 + R_2}$.

Using superposition theorem, we have,

$$V_o = -\frac{R_2}{R_1} V_2' + \left(1+\frac{R_2}{R_1}\right)\left(\frac{R_2 V_1'}{R_1 + R_2}\right)$$





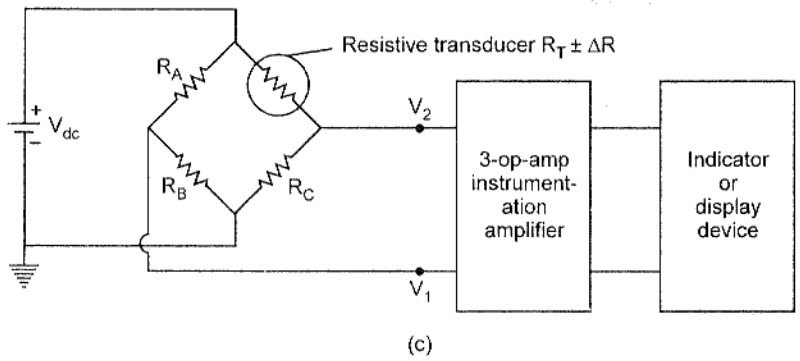


Fig. 4.5 (a) Differential amplifier using single op-amp (b) An improved instrumentation amplifier (c) Instrumentation amplifier using transducer bridge

$$= \frac{R_2}{R_1}(V_1' - V_2') \quad (4.18)$$

Since, no current flows into op-amp, the current I flowing (upwards) in R is $I = (V_1 - V_2)/R$ and passes through the resistor R'.

$$V_1' = R'I + V_1 = \frac{R'}{R}(V_1 - V_2) + V_1 \tag{4.19}$$

and

$$V_2' = -R'I + V_2 = -\frac{R'}{R}(V_1 - V_2) + V_2 \tag{4.20}$$

Putting the values of V_1' and V_2' in Eq. (4.18), we obtain,

$$V_o = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right] \tag{4.21}$$

or,

$$V_o = \frac{R_2}{R_1}\left(1 + \frac{2R'}{R}\right)(V_1 - V_2) \tag{4.22}$$

The difference gain of this instrumentation amplifier can be varied by using a variable resistance R.

Figure 4.5 (c) shows a differential instrumentation amplifier using transducer bridge. The circuit uses a resistive transducer whose resistance changes as a function of the physical quantity to be measured. The bridge is initially balanced by a dc supply voltage V_{dc} so that $V_1 = V_2$. As the physical quantity changes, the resistance R_T of the transducer also changes, causing an unbalance in the bridge ($V_1 \neq V_2$). This differential voltage now gets amplified by the three op-amp differential instrumentation amplifier.

4.4 AC AMPLIFIER

The inverting and non-inverting op-amp amplifier configurations discussed earlier, respond to both ac and dc signals. However, if one wants to get the ac frequency response of an op-amp or if the ac input signal is superimposed with dc level, it becomes essential to block the dc component. This is achieved by using an AC amplifier with a coupling capacitor. AC amplifiers are of inverting and non-inverting type.

Inverting AC Amplifier

The circuit is shown in Fig. 4.6 (a). The capacitor C blocks the dc component of the input and together with the resistor R_1 sets the lower 3 dB frequency of the amplifier.

Since node 'a' is at virtual ground, the output voltage V_o (as a function of complex variable s) is given by,

$$V_o = -IR_f = \frac{V_i}{R_1 + 1/sC} R_f \tag{4.23}$$

Therefore,

$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}\frac{s}{s + 1/R_1C} \tag{4.24}$$

It is seen from Eq. (4.24) that the lower 3dB frequency is,

$$f_L = \frac{1}{2\pi R_1 C} \tag{4.25}$$

In the mid-band range of frequencies, capacitor C behaves as a short circuit and therefore, Eq. (4.24) becomes,

$$A_{CL} \approx -\frac{R_f}{R_1} \tag{4.26}$$

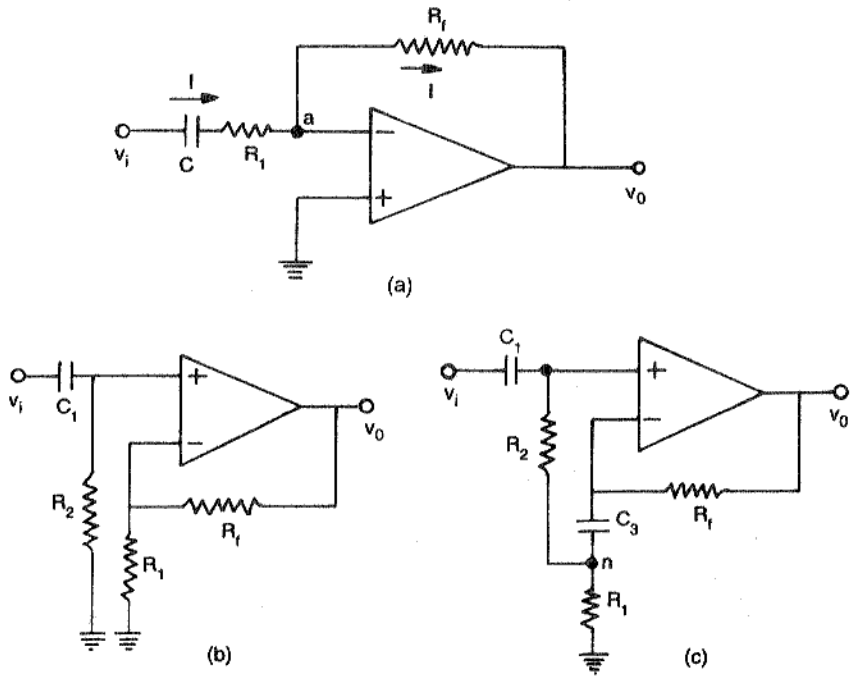


Fig. 4.6 (a) Inverting ac amplifier (b) Non-inverting ac amplifier (c) High input impedance noninverting ac amplifier

Non-inverting AC Amplifier

The circuit is shown in Fig. 4.6 (b). Here a resistor R_2 is added to provide a dc return to ground. However, this reduces the overall input impedance of the amplifier, which now becomes approximately R_2. This problem of low input impedance is eliminated by connecting

a capacitor C_3 as in Fig. 4.6 (c). Capacitor C_3 is large enough to act as short circuit to ac signals. The non-inverting terminal and the node 'n' will be almost at the same potential so that R_2 carries almost no current. Hence the circuit will have an extremely high input impedance.

AC Voltage Follower

The circuit of a practical ac voltage follower is shown in Fig. 4.7. The circuit is used as a buffer to connect a high impedance signal source to a low impedance load which may even be capacitive. The capacitor C_1 and C_2 are chosen high so that they are short circuit at all frequencies of operation. Resistors R_1 and R_2 provide a path for dc input current into the non-inverting terminal. C_2 acts as a bootstrapping capacitor and connects the resistance R_1 to the output terminal for ac operation. Hence the input resistance that the source sees is approximately $R_1/(1 - A_{CL})$ [from Miller's theorem] where A_{CL} is the gain of the voltage follower which is close to unity (0.9997). Thus very high input impedance can be obtained.

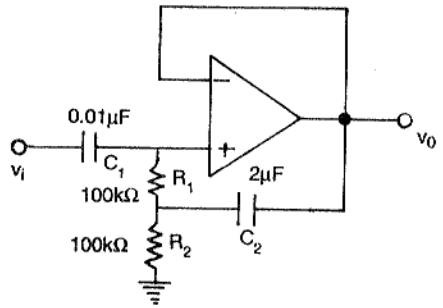


Fig. 4.7 AC voltage follower

4.5 *V* TO *I* AND *I* TO *V* CONVERTER

Voltage to Current Converter (Transconductance Amplifier)

In many applications, one may have to convert a voltage signal to a proportional output current. For this, there are two types of circuits possible.

V-I Converter with floating load
V-I Converter with grounded load

Figure 4.8 (a) shows a voltage to current converter in which load Z_L is floating. Since voltage at node 'a' is v_i, therefore,

$$v_i = i_L R_1 \qquad (\text{as } I_B^- = 0)$$

or,
$$i_L = \frac{v_i}{R_1} \tag{4.27}$$

That is the input voltage v_i is converted into an output current of v_i/R_1. It may be seen that the same current flows through the signal source and load and, therefore, signal source should be capable of providing this load current.

A voltage-to-current converter with grounded load is shown in Fig. 4.8 (b). Let v_1 be the voltage at node 'a'. Writing KVL, we get

$$i_1 + i_2 = i_L \tag{4.28}$$

or,
$$\frac{v_i - v_1}{R} + \frac{v_o - v_1}{R} = i_L$$

or,
$$v_i + v_o - 2v_1 = i_L R$$

Therefore,
$$v_1 = \frac{v_i + v_o - i_L R}{2} \tag{4.29}$$

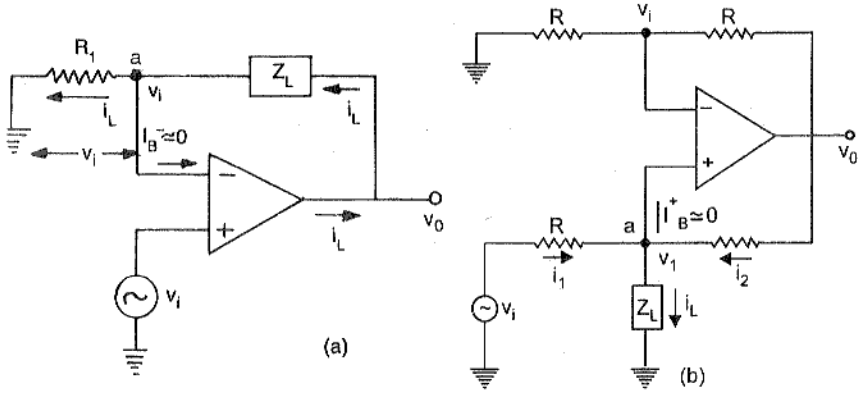


Fig. 4.8 Voltage to current converter with (a) floating load (b) grounded load

Since the op-amp is used in non-inverting mode, the gain of the circuit is $1 + R/R = 2$. The output voltage is,

$$v_o = 2v_1 = v_i + v_o - i_L R$$

that is,
$$v_i = i_L R$$

or,
$$i_L = \frac{v_i}{R} \tag{4.30}$$

As the input impedance of a non-inverting amplifier is very high, this circuit has the advantage of drawing very little current from the source. A voltage to current converter is used for low voltage dc and ac voltmeter, LED and zener diode tester.

Current to Voltage Converter (Transresistance Amplifier)

Photocell, photodiode and photovoltaic cell give an output current that is proportional to an incident radiant energy or light. The current through these devices can be converted to voltage by using a current-to-voltage converter and thereby the amount of light or radiant energy incident on the photo-device can be measured.

Figure 4.9. shows an op-amp used as I to V converter. Since the (–) input terminal is at virtual ground, no current flows through R_s and current i_s flows through the feedback resistor R_f. Thus the output voltage $v_o = -i_s R_f$. It may be pointed out that the lowest current that this circuit can measure will depend upon the bias current I_B of the op-amp. This means that μA741 (I_B = 3 nA) can be used to detect lower currents. The resistor R_f is sometimes shunted with a capacitor C_f to reduce high frequency noise and the possibility of oscillations.

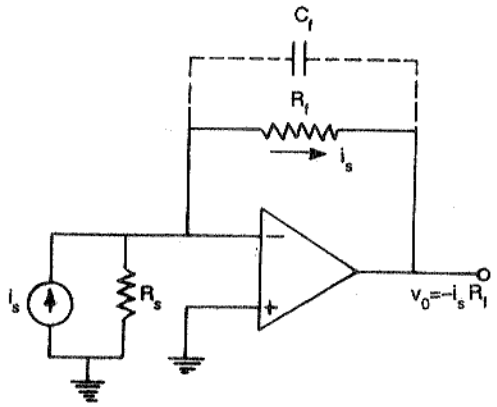


Fig. 4.9 Current to voltage converter

4.6 OP-AMP CIRCUITS USING DIODES

The major limitation of ordinary diode is that it cannot rectify voltages below V_γ (~ 0.6 V), the cut-in voltage of the diode. A circuit that acts like an ideal diode can be designed by placing a diode in the feedback loop of an op-amp as in Fig. 4.10 (a). Here the cut-in voltage is divided by the open loop gain A_{OL} (~ 10^4) of the op-amp so that V_γ is virtually eliminated. When the input $v_i > V_\gamma/A_{OL}$ then v_{oA}, the output of the op-amp exceeds V_γ and the diode D conducts. Thus the circuit acts like a voltage follower for input $v_i > V_\gamma/A_{OL}$ (i.e., $0.6/10^4 = 60$ μV) and the output v_o follows the input voltage v_i during the positive half cycle as shown in Fig. 4.10 (b). When v_i is negative or less than V_γ/A_{OL}, the diode D is ***off*** and no current is delivered to the load R_L except for

small bias current of the op-amp and the reverse saturation current of the diode. This circuit is called the precision diode and is capable of rectifying input signals of the order of millivolt. Some typical applications of a precision diode discussed are:

Half-wave rectifier
Full-wave rectifier
Peak-value detector
Clipper
Clamper

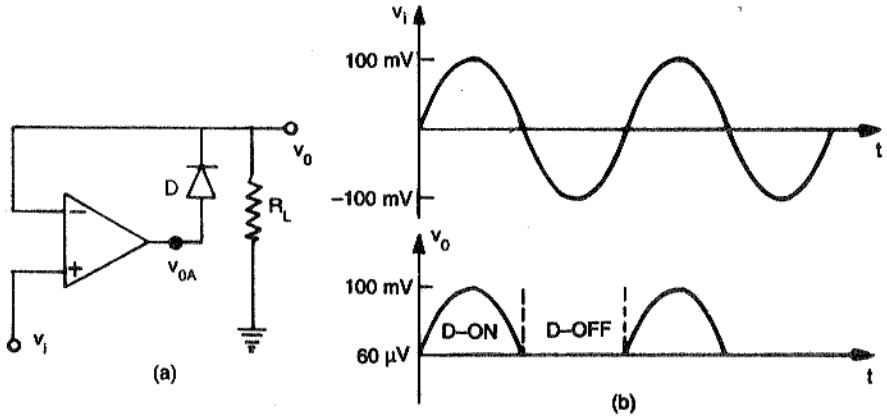


Fig. 4.10 (a) Precision diode (b) Input and output waveforms

4.6.1 Half-Wave Rectifier

An inverting amplifier can be converted into an idea half-wave rectifier by adding two diodes as shown in Fig. 4.11 (a). When v_i is positive, diode D_1 conducts causing v_{OA} to go to negative by one diode drop (~ 0.6 V). Hence diode D_2 is reverse biased. The output voltage v_o is zero, because, for all practical purposes, no current flows through R_f and the input current flows through D_1.

For negative input, i.e., $v_i < 0$, diode D_2 conducts and D_i is ***off***. The negative input v_i forces the op-amp output v_{OA} positive and causes D_2 to conduct. The circuit then acts like an inverter for $R_f = R_1$ and output v_o becomes positive.

The input, output waveforms are shown in Fig. 4.11 (b). The op-amp in the circuit of Fig. 4.11 (a) must be a high speed op-amp since it alternates between open loop and closed loop operations. The principal limitation of this circuit is the slew rate of the op-amp. As the input passes through zero, the op-amp output v_{oA} must change from 0.6 V to – 0.6 V or vice-versa as quickly as possible in order to switch over the conduction from one diode to the other.

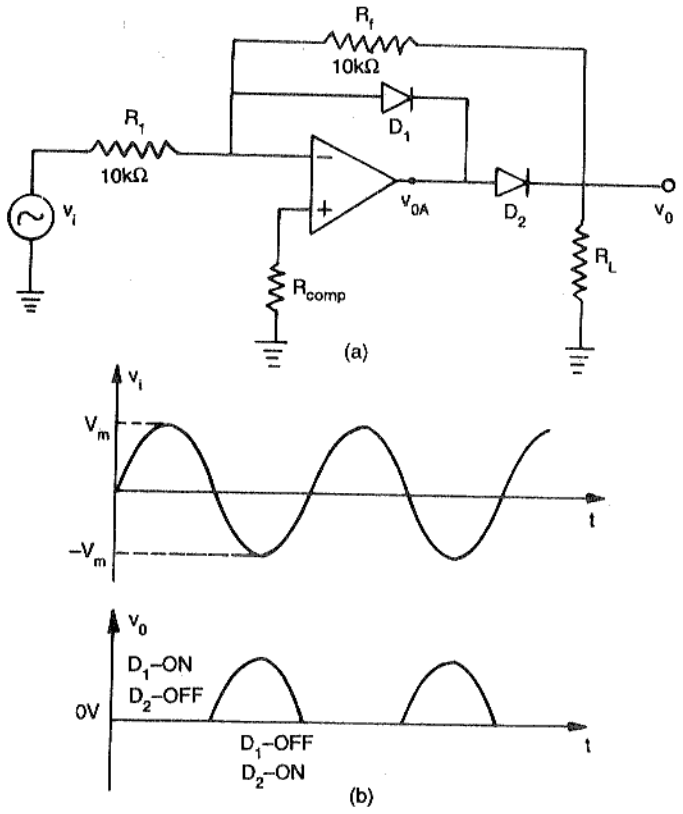


Fig. 4.11 (a) Ideal half wave rectifier (b) Input/output waveforms

4.6.2 Full-wave Rectifier

A full wave rectifier or absolute value circuit is shown in Fig. 4.12 (a). For positive input, i.e. $v_i > 0$, diode D_1 is ***on*** and D_2 is ***off***. Both the op-amps A_1 and A_2 act as inverter as shown in equivalent circuit in Fig. 4.12 (b). It can be seen that $v_0 = v_i$.

For negative input, i.e. $v_i < 0$, diode D_1 is ***off*** and D_2 is ***on***. The equivalent circuit is shown in Fig. 4.12 (c). Let the output voltage of op-amp A_1 be v. Since the differential input to A_2 is zero, the inverting input terminal is also at voltage v.

KCL at node 'a' gives

$$\frac{v_i}{R} + \frac{v}{2R} + \frac{v}{R} = 0$$

or

$$v = -\frac{2}{3} v_i \qquad (4.31)$$

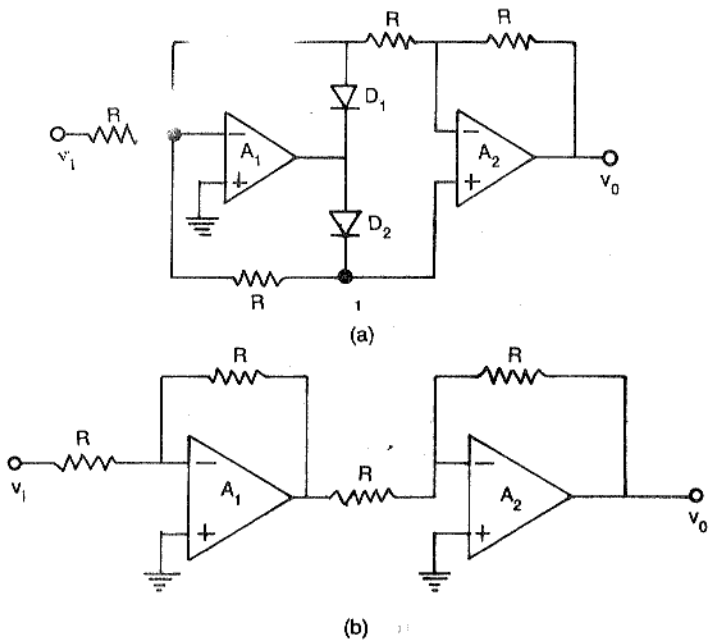


Fig. 4.12 (a) Precision full wave rectifier (b) Equivalent circuit for $v_i > 0$

The equivalent circuit of Fig. 4.12 (c) is a non-inverting amplifier as shown in Fig. 4.12 (d). The output v_o is,

$$v_o = \left(1 + \frac{R}{2R}\right)\left(-\frac{2}{3} v_i\right) = v_i \qquad (4.32)$$

Hence for $v_i < 0$, the output is positive. The input and output waveforms are shown in Fig. 4.12 (e).

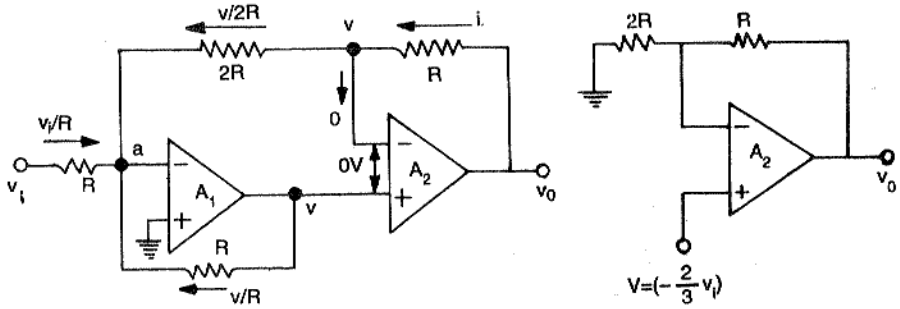


Fig. 4.12 (c) Equivalent circuit for $v_i < 0$ (d) Equivalent circuit of (c)

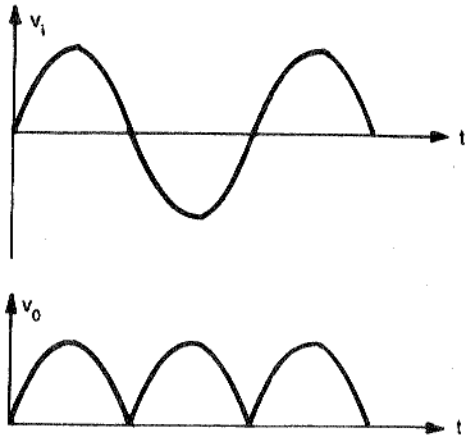


Fig. 4.12 (e) Input and output waveforms

4.6.3 Peak Detector

The function of a peak detector is to compute the peak value of the input. The circuit follows the voltage peaks of a signal and stores the highest value (almost indefinitely) on a capacitor. If a higher peak signal value comes along, this new value is stored. The highest peak value is stored until the capacitor is discharged.

Consider the circuit of Fig. 4.13 (a). When input v_i exceeds v_c, the then voltage across the capacitor, the diode D is forward biased and the circuit becomes a voltage follower. Consequently, the output voltage v_o follows v_i as long as v_i exceeds v_c. When v_i drops below v_c, the diode

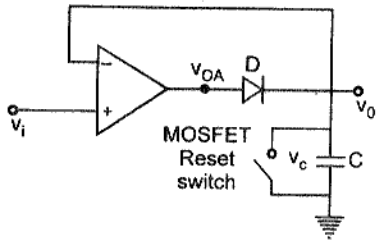


Fig. 4.13 (a) Positive peak detector

becomes reverse-biased and the capacitor holds the charge till input voltage again attains a value greater than v_c. Figure 4.13 (b) shows the voltage waveshape for the positive peak detector. It may be noted that the peak at time t' is missed, the reason is obvious. The circuit can be reset, that is, capacitor voltage can be made zero by connecting a low leakage MOSFET switch across the capacitor. The circuit can be modified to hold the lowest or most negative voltage of a signal by reversing the diode. Peak detectors find application in test and measurement instrumentation as well as in amplitude modulation (AM) communication.

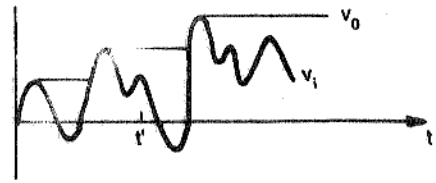


Fig. 4.13 (b) Output v_0 corresponding to arbitrary input v_i

4.6.4 Clipper

A precision diode may also be used to clip-off a certain portion of the input signal to obtain a desired output waveform.

Figure 4.14 (a) shows a positive clipper. The clipping level is determined by the reference voltage V_{ref} and could be obtained from the positive supply voltage V^+. The input and output waveforms are shown in Fig. 4.14 (b). It can be seen that the portion of the output voltage for $v_o > V_{ref}$ are clipped off.

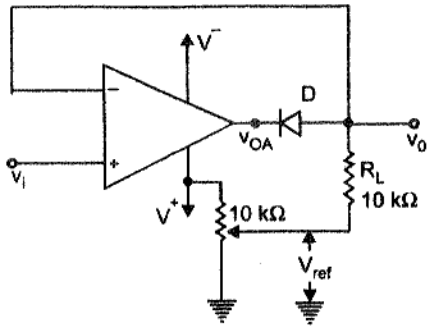


Fig. 4.14 (a) Positive clipper circuit

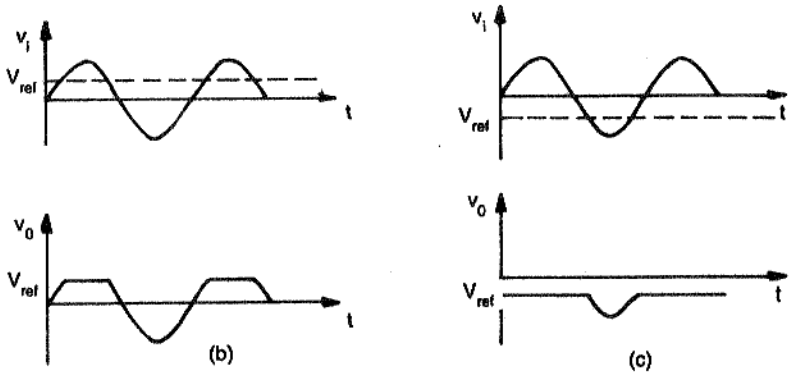


Fig. 4.14 Input and output waveforms for (b) positive V_{ref} (c) Negative V_{ref}

For input voltage $v_i < V_{ref}$, diode D conducts. The op-amp works as a voltage follower and output v_o follows input v_i till $v_i \leq V_{ref}$. When v_i is greater than V_{ref}, the output v_{oA} of the op-amp is large enough of drive D into cut-off. The op-amp operates in the open-loop and output voltage $v_o = V_{ref}$. However, if V_{ref} is made negative, then the entire output waveform above V_{ref} will get clipped off as shown in fig. 4.14 (c).

The positive clipper of Fig. 4.14. (a) can be easily converted into a negative clipper by simply reversing diode D and changing the polarity of the reference voltage V_{ref} as shown in Fig. 4.15 (a). The negative clipper clips off the negative parts of the input signal below the reference voltage. The circuit diagram of a negative clipper and the expected waveforms for negative V_{ref} and positive V_{ref} are shown in Fig. 4.15 (b and c).

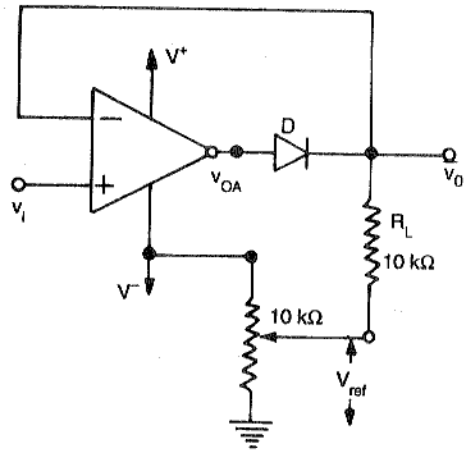


Fig. 4.15 (a) Negative clipper circuit

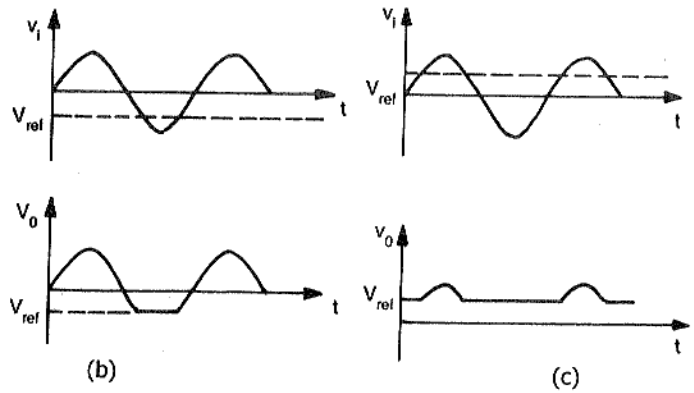


Fig. 4.15 (b, c) Input-output waveforms for negative and positive V_{ref}

4.6.6 Clamper

The clamper is also known as dc inserter or restorer. The circuit is used to add a desired dc level to the output voltage. In other words, the output is clamped to a desired dc level. If the clamped dc level is positive, it is called positive clamper. Similarly if the clamped dc level is negative, the clamper is called negative clamper.

Figure 4.16 (a) shows a clamper with a variable positive dc voltage applied at the (+) input terminal. This circuit clamps the peaks of the input waveform and therefore is also called a peak clamper. The output voltage in the circuit is the net result of ac and dc input voltages applied to the (–) and (+) input terminals respectively. Let us first see the effect of V_{ref} applied at the (+) input terminal. For positive V_{ref}, the voltage v' is also positive, so that the diode D is forward biased. The circuit operates as a voltage follower and therefore output voltage $v_o = + V_{ref}$.

Now consider the ac input signal $v_i = V_m \sin \omega t$ applied at the (–) input terminal. During the negative half cycle of v_i, diode D conducts. The capacitor C_1 charges through diode D to the negative peak voltage V_m. However, during the positive half cycle of v_i, diode D is reverse biased. The capacitor retains its previous voltage V_m. Since this voltage V_m is in series with the ac input signal, the output voltage now will be $v_i + V_m$. The total output voltage is, therefore,

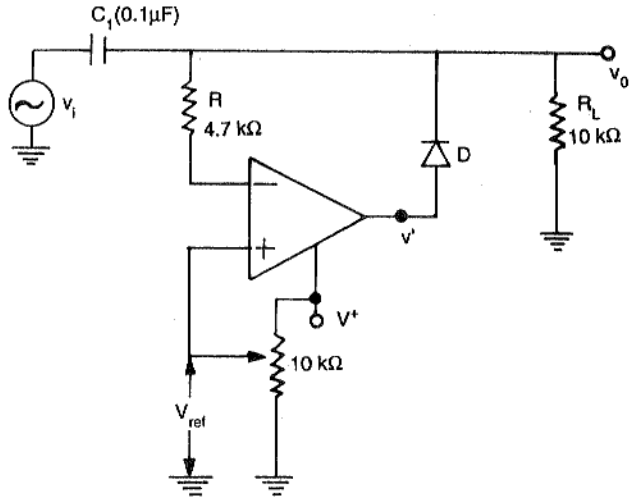


Fig. 4.16 (a) Peak clamper circuit

$V_{ref} + v_i + V_m$. The input and output waveforms are shown in Fig. 4.16 (b). It is possible to obtain negative peak clamping by reversing the diode D and using a negative reference voltage $-V_{ref}$. The expected waveforms are shown in Fig. 4.16 (c). The resistor R is used for

protecting the op-amp against excessive discharge currents from capacitor C_1 especially when the dc supply voltages are switched off.

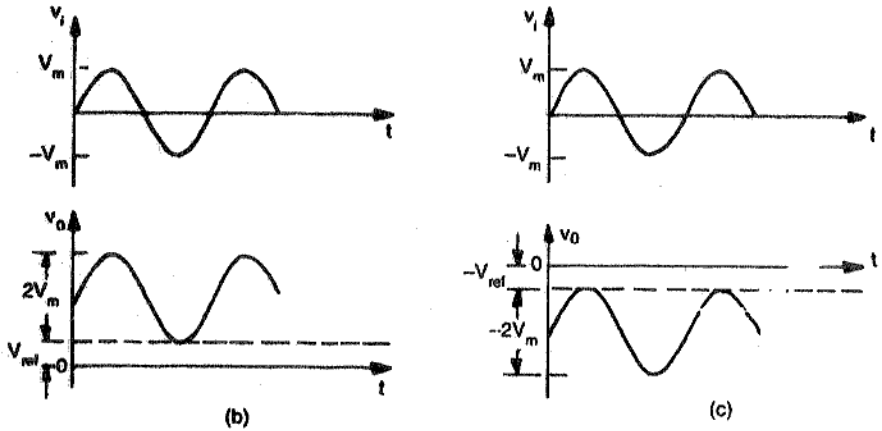


Fig. 4.16 (b) Waveforms for + V_{ref} (c) Waveforms for − V_{ref}

4.7 SAMPLE AND HOLD CIRCUIT

A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This type of circuit is very useful in digital interfacing and analog to digital and pulse code modulation systems. One of the simplest practical sample and hold circuit configuration is shown in Fig. 4.17 (a). The *n*-channel E-MOSFET works as a switch and is controlled by the control voltage v_c and the capacitor C stores the charge. The analog signal v_i to be

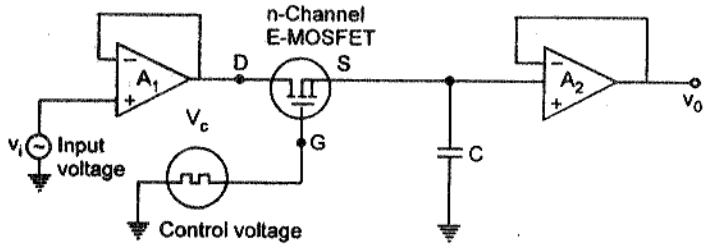


Fig. 4.17 (a) Sample and hold circuit

sampled is applied to the drain of E-MOSFET and the control voltage v_c is applied to its gate. When v_c is positive, the E-MOSFET turns ***on*** and the capacitor C charges to the instantaneous value of input v_i with a time constant $[(R_o + r_{DS}\ (on)]\ C$. Here R_o is the output resistance of the voltage follower A_1 and r_{DS} (***on***) is the resistance of the MOSFET

when ***on***. Thus the input voltage v_i appears across the capacitor C and then at the output through the voltage follower A_2. The waveforms are as shown in Fig. 4.17 (b).

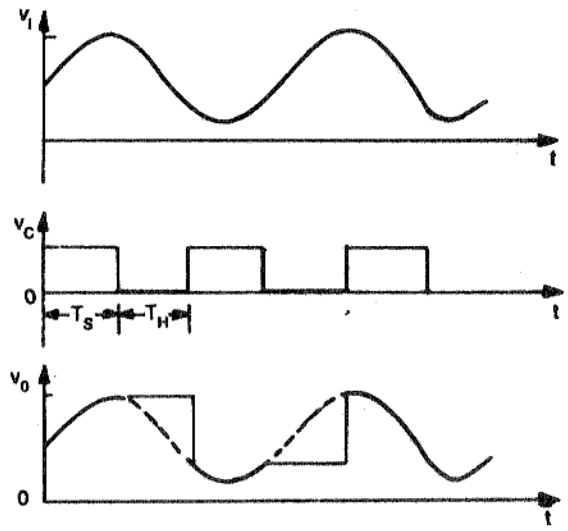


Fig. 4.17 (b) Input and output waveforms

During the time when control voltage v_c is zero, the E-MOSFET is ***off***. The capacitor C is now facing the high input impedance of the voltage follower A_2 and hence cannot discharge. The capacitor holds the voltage across it. The time period T_S, the time during which voltage across the capacitor is equal to input voltage is called sample period. The time period T_H of v_c during which the voltage across the capacitor is held constant is called hold period. The frequency of the control voltage should be kept higher than (at least twice) the input so as to retrieve the input from output waveform. A low leakage capacitor such as Polystyrene, Mylar, or Teflon should be used to retain the stored charge.

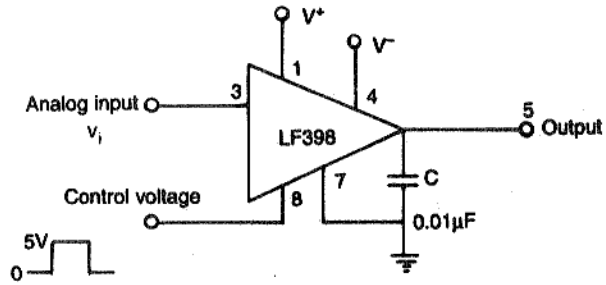


Fig. 4.17 (c) Typical connection diagram

Specially designed sample and hold ICs of make Harris semiconductor HA2420, National semiconductor such as LF198, LF398 are also available. A typical connection diagram of the LF398 is shown in Fig. 4.17 (c). It may be noted that the storage capacitor C is connected externally.

4.8 LOG AND ANTILOG AMPLIFIER

There are several applications of log and antilog amplifiers. Antilog computation may require functions such as ln x, log x or sinh x. These can be performed continuously with log-amps. One would like to have direct dB display on digital voltmeter and spectrum analyser. Log-amp can easily perform this function. Log-amp can also be used to compress the dynamic range of a signal.

Log Amplifier

The fundamental log-amp circuit is shown in Fig. 4.18 (a) where a grounded base transistor is placed in the feedback path. Since the collector is held at virtual ground and the base is also grounded, the transistor's voltage-current relationship becomes that of a diode and is given by,

$$I_E = I_s\,(e^{qV_E/kT} - 1) \tag{4.33}$$

Since, $I_C = I_E$ for a grounded base transistor,

$$I_C = I_s\,(e^{qV_E/kT} - 1) \tag{4.34}$$

I_s = emitter saturation current $\approx 10^{-13}$ A
k = Boltzmann's Constant
T = absolute temperature (in °K)

Therefore, $$\frac{I_C}{I_s} = (e^{q\,V_E/kT} - 1) \tag{4.35}$$

or, $$e^{q\,V_E/kT} = \frac{I_C}{I_s} + 1$$

$$\approx \frac{I_C}{I_s} \qquad [\text{as } I_s \approx 10^{-13}\text{ A},\ I_C >> I_s]$$

Taking natural log on both sides, we get

$$V_E = \frac{kT}{q} \ln\left(\frac{I_C}{I_s}\right) \tag{4.36}$$

Also in Fig. 4.18 (a), $I_C = \dfrac{V_i}{R_1}$

$$V_E = -V_o$$

so, $$V_o = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) = -\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.37}$$

where $$V_{ref} = R_1 I_s$$

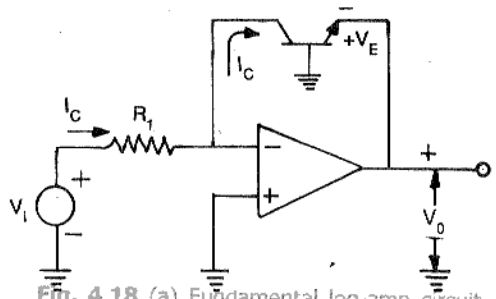


Fig. 4.18 (a) Fundamental log-amp circuit

The output voltage is thus proportional to the logarithm of input voltage. Although the circuit gives natural log (ln), one can find $\log_{10}$ by proper scaling

$$\log_{10} X = 0.4343 \ln X \tag{4.38}$$

The circuit, however, has one problem. The emitter saturation current I_s varies from transistor to transistor and with temperature. Thus a stable reference voltage V_{ref} cannot be obtained. This is eliminated by the circuit given in Fig. 4.18 (b). The input is applied to one log-amp, while a reference voltage is applied to another log-amp. The two transistors are integrated close together in the same silicon wafer. This provides a close match of saturation currents and ensures good thermal tracking.

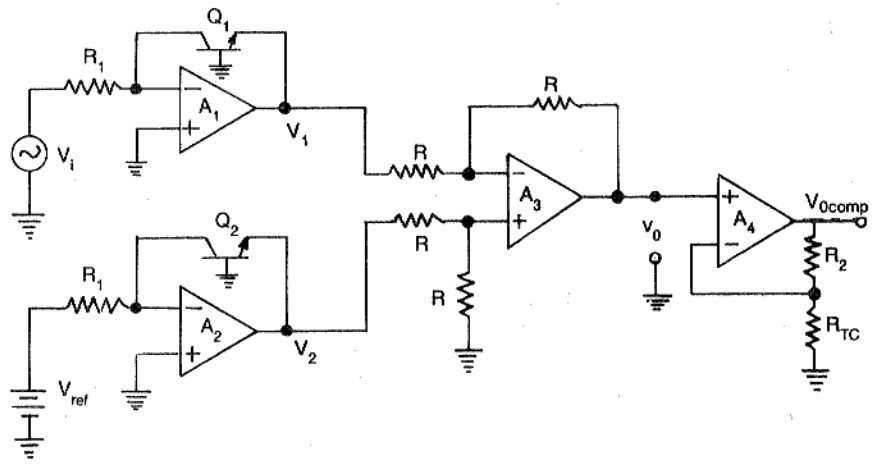


Fig. 4.18 (b) Log-amp with saturation current and temperature compensation

Assume, $$I_{s1} = I_{s2} = I_s \tag{4.39}$$

and then, $$V_1 = -\frac{kT}{q} \ln\left(\frac{V_i}{R_1 I_s}\right) \tag{4.40}$$

and $$V_2 = -\frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.41}$$

Now, $$V_o = V_2 - V_1 = \frac{kT}{q}\left[\ln\left(\frac{V_i}{R_1 I_s}\right) - \ln\left(\frac{V_{ref}}{R_1 I_s}\right)\right] \tag{4.42}$$

or, $$V_o = \frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.43}$$

Thus reference level is now set with a single external voltage source. Its dependence on device and temperature has been removed. The voltage V_o is still dependent upon temperature and is directly proportional to T. This is compensated by the last op-amp stage A_4 which provides a non-inverting gain of $(1 + R_2/R_{TC})$. Now, the output voltage is,

$$V_{o\ comp} = \left(1 + \frac{R_2}{R_{TC}}\right)\frac{kT}{q} \ln\left(\frac{V_i}{V_{ref}}\right) \tag{4.44}$$

where R_{TC} is a temperature-sensitive resistance with a positive coeffecient of temperature (sensistor) so that the slope of the equation becomes constant as the temperature changes.

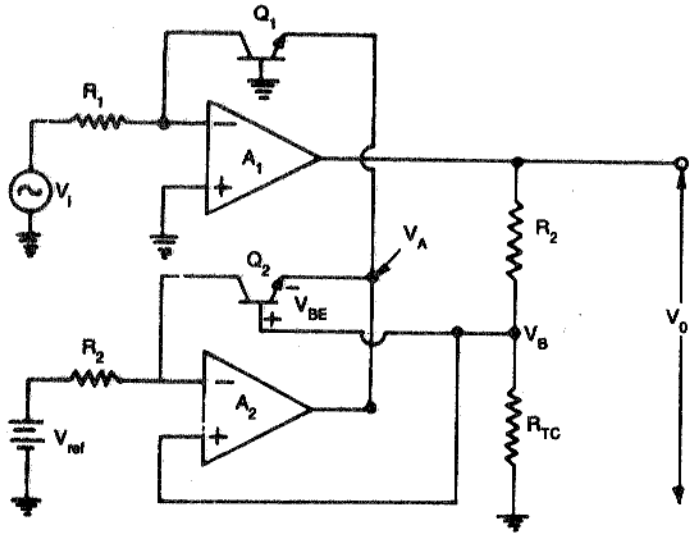


Fig. 4.18 (c) Log-amp using two op-amps only

The circuit in Fig. 4.18. (b) requires four op-amps, and becomes expensive if FET op-amps are used for precision. The same output (with an inversion) can be obtained by the circuit of Fig. 4.18 (c) using two op-amps only.

Antilog Amplifier

The circuit is shown in Fig. 4.19. The input V_i for the antilog-amp is fed into the temperature compensating voltage divider R_2 and R_{TC} and then to the base of Q_2. The output V_o of the antilog-amp is fed back to the inverting input of A_1 through the resistor R_1. The base to emitter voltage of transistors Q_1 and Q_2 can be written as

$$V_{Q1\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.45}$$

and $$V_{Q2\ B\text{-}E} = \frac{kT}{q} \ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.46}$$

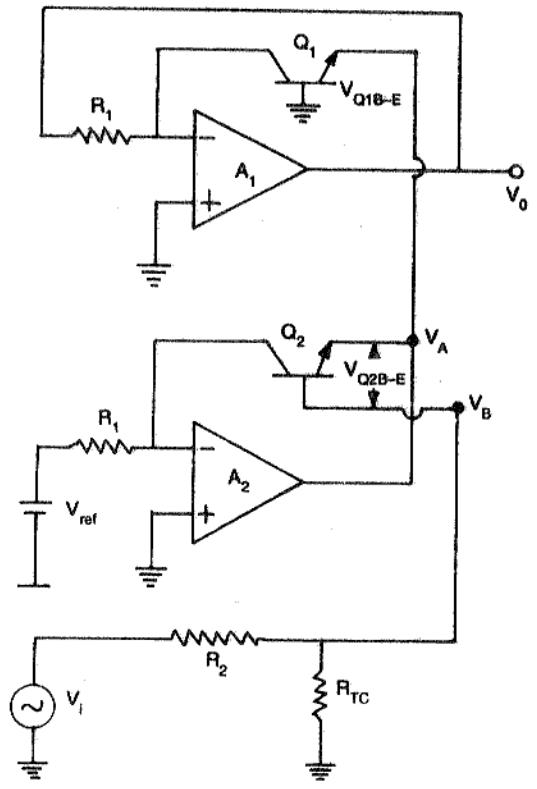


Fig. 4.19 Antilog amplifier

Since the base of Q_1 is tied to ground, we get

$$V_A = -V_{Q1\ B\text{-}E} = -\frac{kT}{q}\ln\left(\frac{V_o}{R_1 I_s}\right) \tag{4.47}$$

The base voltage V_B of Q_2 is

$$V_B = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i \tag{4.48}$$

The voltage at the emitter of Q_2 is

$$V_{Q2\ E} = V_B + V_{Q2\ E\text{-}B}$$

or,
$$V_{Q2\ E} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i - \frac{kT}{q}\ln\left(\frac{V_{ref}}{R_1 I_s}\right) \tag{4.49}$$

But the emitter voltage of Q_2 is V_A, that is,

$$V_A = V_{Q2\ E}$$

or,
$$-\frac{kT}{q}\ln\frac{V_o}{R_1 I_s} = \frac{R_{TC}}{R_2 + R_{TC}}V_i - \frac{kT}{q}\ln\frac{V_{ref}}{R_1 I_s} \tag{4.50}$$

or,
$$\frac{R_{TC}}{R_2 + R_{TC}}V_i = -\frac{kT}{q}\left(\ln\frac{V_o}{R_1 I_s} - \ln\frac{V_{ref}}{R_1 I_s}\right)$$

or,
$$-\frac{q}{kT}\frac{R_{TC}}{R_2 + R_{TC}}V_i = \ln\left(\frac{V_o}{V_{ref}}\right) \tag{4.51}$$

Changing natural log, i.e., ln to $\log_{10}$ using Eq. (4.38) we get

$$-0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right)V_i = 0.4343 \times \ln\left(\frac{V_o}{V_{ref}}\right) \tag{4.52}$$

or,
$$-K'V_i = \log_{10}\left(\frac{V_o}{V_{ref}}\right)$$

or,
$$\frac{V_o}{V_{ref}} = 10^{-K'V_i}$$

or,
$$V_o = V_{ref}\,(10^{-K'V_i}) \tag{4.53}$$

where
$$K' = 0.4343\left(\frac{q}{kT}\right)\left(\frac{R_{TC}}{R_2 + R_{TC}}\right) \tag{4.54}$$

Hence an increase of input by one volt causes the output to decrease by a decade. The 755 log/antilog amplifier IC chip is available as a

functional module which may require some external components also to be connected to it.

4.9 MULTIPLIER AND DIVIDER

Multiplier

There are a number of applications of analog multiplier such as frequency doubling, frequency shifting, phase angle detection, real power computation, multiplying two signals, dividing and squaring of signals. A basic multiplier schematic symbol is shown in Fig. 4.20 (a). Two signal inputs (v_x and v_y) are provided. The output is the product of the two inputs divided by a reference voltage V_{ref}.

$$v_o = \frac{v_x\, v_y}{V_{ref}} \tag{4.55}$$

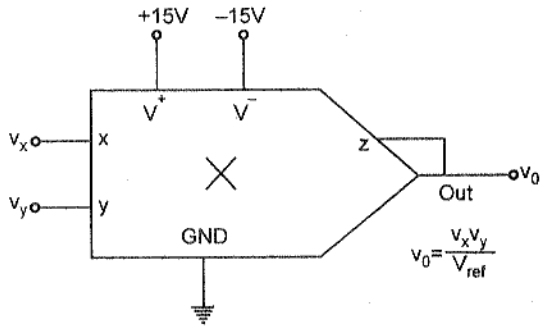


Fig. 4.20 (a) Multiplier schematic symbol

Normally, V_{ref} is internally set to 10 volts. So,

$$v_o = \frac{v_x\, v_f}{10}$$

As long as

$$v_x < V_{ref}$$

and
$$v_y < V_{ref}$$

the output of the multiplier will not saturate.

If both inputs are positive, the IC is said to be a one quadrant multiplier. A two quadrant multiplier will function properly if one input is held positive and the other is allowed to swing both positive and negative. If both inputs may be either positive or negative, the IC is called a four quadrant multiplier.

There can be several ways to make a circuit which will multiply according to Eq. (4.55). One commonly used technique is log-antilog method. The log-antilog method relies on the mathematical relationship

that the sum of the logarithm of two numbers equals the logarithm of the product of those numbers.

$$\ln v_x + \ln v_y = \ln (v_x v_y) \tag{4.56}$$

Figure 4.20 (b) is a block diagram of a log-antilog multiplier IC. Log -amps require the input and reference voltages to be of the same polarity. This restricts log-antilog multipliers to one quadrant operation. A technique that provides four quadrant multiplication is transconductance multiplier. Some of the multiplier IC chips available are AD533 and AD534. We now discuss two applications of multiplier IC.

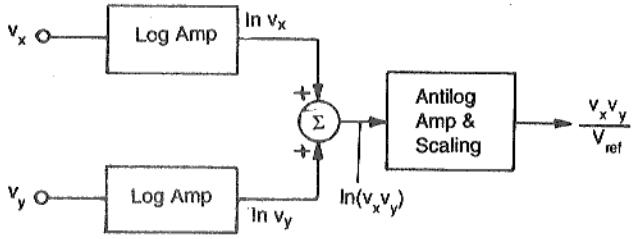


Fig. 4.20 (b) Block diagram of a log-antilog

Frequency Doubling

The multiplication of two sine waves of the same frequency, but of possibly different amplitudes and phase allows to double a frequency and to directly measure real power. Let

$$v_x = V_x \sin \omega t \tag{4.57}$$

$$v_y = V_y \sin (\omega t + \theta) \tag{4.58}$$

where θ is the phase difference between the two signals. Applying these two signals to the inputs of a four quadrant multiplier will yield an output as,

$$v_o = \frac{V_x \sin \omega t \, V_y \sin (\omega t + \theta)}{V_{ref}} \tag{4.54}$$

$$v_o = \frac{V_x V_y}{V_{ref}} \sin \omega t (\sin \omega t \cos \theta + \sin \theta \cos \omega t)$$

$$= \frac{V_x V_y}{V_{ref}} (\sin^2 \omega t \cos \theta + \sin \theta \sin \omega t \cos \omega t)$$

But $\sin^2 a = 1 - \cos^2 a$

and $\cos^2 a = 2 \cos^2 a - 1$

so $\cos^2 a = \frac{1}{2} + \left(\frac{1}{2}\right) \cos 2a$

$$\sin^2 a = 1 - \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a = \frac{1}{2} - \left(\frac{1}{2}\right) \cos 2a$$

so $$v_o = \frac{V_x V_y}{V_{ref}} \left[\cos \theta \left(\frac{1}{2} - \left(\frac{1}{2}\right) \cos 2 \omega t \right) + \sin \theta \sin \omega t \cos \omega t \right] \tag{4.60}$$

But, $\sin a \cos a = \left(\frac{1}{2}\right) \sin 2a$

Hence, $$v_o = \frac{V_x V_y}{2 V_{ref}} (\cos \theta - \cos \theta \cos 2\omega t + \sin \theta \sin 2\omega t)$$

or, $$v_o = \frac{V_x V_y}{2V_{ref}} \cos \theta + \frac{V_x V_y}{2V_{ref}} (\sin \theta \sin 2 \omega t - \cos \theta \cos 2 \omega t) \tag{4.61}$$

The first term is a DC and is set by the magnitude of the signals and their phase difference. The second term varies with time, but at twice the frequency of the inputs (2ω).

Divider

Division, the complement of multiplication, can be accomplished by placing the multiplier circuit element in the op-amp's feedback loop. The output voltage from the divider in Fig. 4.20 (c) with input signals v_z and v_x as dividend and divisor respectively, is given by

$$v_o = -V_{ref} \frac{v_z}{v_x} \tag{4.62}$$

The result can be derived as follows. The op-amp's inverting terminal is at virtual ground. Therefore,

$$I_z = I_A \tag{4.63}$$

and $$I_z = \frac{v_z}{R} \tag{4.64}$$

The output voltage V_A of the multiplier is determined by the multiplication of v_x and v_y

$$V_A = \frac{v_x v_y}{V_{ref}} = \frac{v_x v_o}{V_{ref}} \tag{4.65}$$

Again $V_A = -I_A R$

so, $$I_A = -V_A/R = -\frac{v_x v_o}{V_{ref} R} \tag{4.66}$$

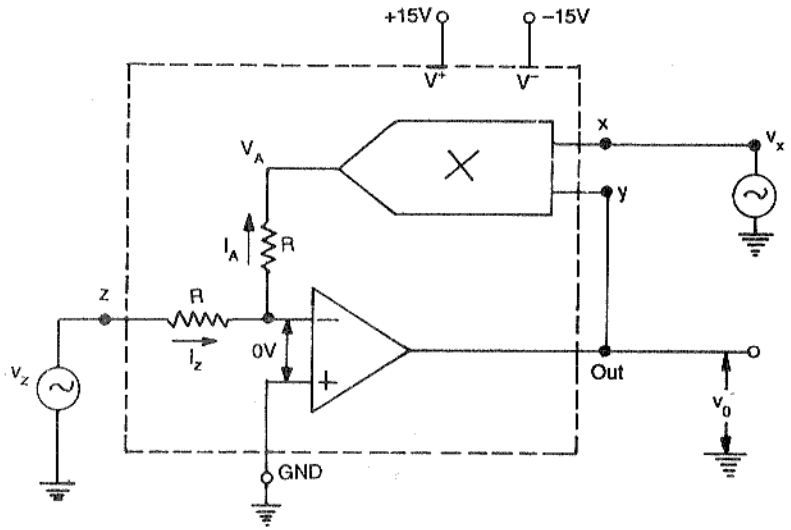


Fig. 4.20 (c) Multiplier IC configured as divider

As, $$I_z = I_A$$

so, $$I_z = -\frac{v_x v_0}{V_{ref} R}$$

From Eq. (4.64), wt get

$$v_z = I_z R = -\frac{v_x v_0}{V_{ref}}$$

or, $$v_0 = -V_{ref}\frac{v_z}{v_x} \qquad (4.67)$$

Division by zero is, of course, prohibited. Multiplier IC can be used for squaring a signal. Similarly, divider circuit can be used to take the square root of a signal.

4.10 DIFFERENTIATOR

One of the simplest of the op-amp circuits that contain capacitor is the differentiating amplifier, or differentiator. As the name suggests, the circuit performs the mathematical operation of differentiation, that is, the output waveform is the derivative of input waveform. A differentiator circuit is shown in Fig. 4.21 (a).

Analysis

The node N is at virtual ground potential i.e., $v_N = 0$. The current i_C through the capacitor is,

$$i_C = C_1 \frac{d}{dt}(v_i - v_N) = C_1 \frac{dv_i}{dt} \qquad (4.68)$$

The current i_f through the feedback resistor is v_o/R_f and there is no current into the op-amp. Therefore, the nodal equation at node N is,

$$C_1 \frac{dv_i}{dt} + \frac{v_o}{R_f} = 0$$

from which we have

$$v_o = -R_f C_1 \frac{dv_i}{dt} \qquad (4.69)$$

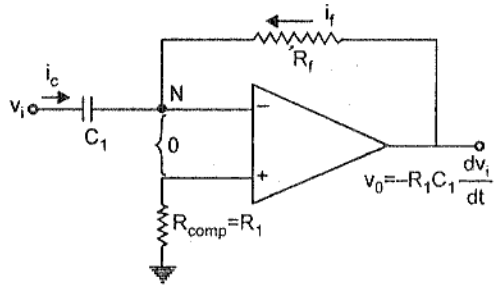


Fig. 4.21 (a) Op-amp differentiator

Thus the output voltage v_o is a constant ($-R_f C_1$) times the derivative of the input voltage v_i and the circuit is a differentiator. The minus sign indicates a 180° phase shift of the output waveform v_o with respect to the input signal.

The phasor equivalent of Eq. (4.69) is, $V_o(s) = -R_f C_1 s V_i(s)$ where V_o and V_i is the phasor representation of v_o and v_i. In steady state, put $s = j\omega$. We may now write the magnitude of gain A of the differentiator as,

$$|A| = \left|\frac{V_o}{V_i}\right| = |-j\omega R_f C_1| = \omega R_f C_1 \qquad (4.70)$$

From Eq. (4.70), one can draw the frequency response of the op-amp differentiator. Equation (4.70) may be rewritten as

$$|A| = \frac{f}{f_a}$$

where $$f_a = \frac{1}{2\pi R_f C_1} \qquad (4.71)$$

At $f = f_a$, $|A| = 1$, i.e., 0 dB, and the gain increases at a rate of +20 dB/decade. Thus at high frequency, a differentiator may become unstable and break into oscillation. There is one more problem in the

differentiator of Fig. 4.21 (a). The input impedance (i.e., $1/\omega C_1$) decreases with increase in frequency, thereby making the circuit sensitive to high frequency noise.

Practical Differentiator

A practical differentiator of the type shown in Fig. 4.21 (b) eliminates the problem of stability and high frequency noise.

The transfer function for the circuit in Fig. 4.21 (b) is given by,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{Z_i} = -\frac{s R_f C_1}{(1 + s R_f C_f)(1 + s C_1 R_1)} \tag{4.72}$$

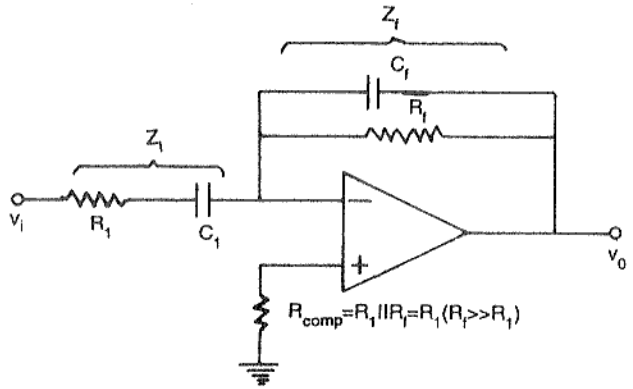


Fig. 4.21 (b) Practical differentiator

For $R_f C_f = R_1 C_1$, we get

$$\frac{V_o(s)}{V_i(s)} = -\frac{sR_fC_1}{(1 + sR_1C_1)^2} = -\frac{sR_fC_1}{\left(1 + j\dfrac{f}{f_b}\right)^2} \tag{4.73}$$

where, $$f_b = \frac{1}{2\pi R_1 C_1} \tag{4.74}$$

From Eq. (4.73) it is evident that the gain increases at +20 dB/decade for frequency $f < f_b$ and decreases at –20 dB/decade for $f > f_b$ as shown by dashed lines in Fig. 4.21 (c). This 40 dB/decade change in gain is caused by $R_1 C_1$ and $R_f C_f$ factors. For the basic differentiator of Fig. 4.21 (a) the frequency response would have increased continuously at the rate of +20 dB/decade even beyond f_b causing stability problem at high frequency. Thus the gain at high frequency is reduced significantly, thereby avoiding the high frequency noise and stability problems. The value of f_b should be selected such that,

$$f_a < f_b < f_c$$

where f_c is the unity gain-bandwidth of the op-amp in open-loop configuration.

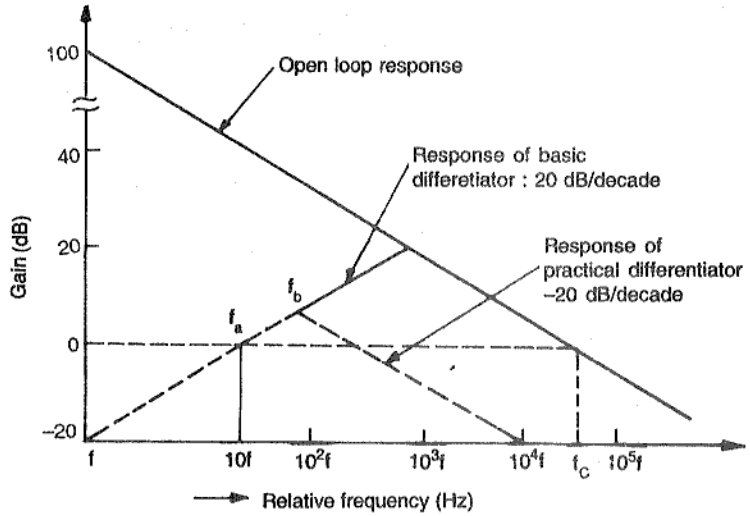


Fig. 4.21 (c) Frequency response

For good differentiation, one must ensure that the time period T of the input signal is larger than or equal to $R_f C_1$, that is,

$$T \geq R_f C_1 \tag{4.75}$$

It may be noted that for $R_f C_1$ much greater than $R_1 C_1$ or $R_f C_f$, Eq. (4.72) is reduced to, $V_o/V_i = -sR_f C_1$, that is, the expression of the output voltage remains the same as in the case of an ideal differentiator as

$$v_o = -R_f C_1 \frac{dv_i}{dt} \tag{4.76}$$

A resistance R_{comp} $(= R_1 \| R_f)$ is normally connected to the (+) input terminal to compensate for the input bias circuit.

A good differentiator may be designed as per the following steps:

1. Choose f_a equal to the highest frequency of the input signal. Assume a practical value of C_1 (< 1μF) and then calculate R_f.
2. Choose $f_b = 10\, f_a$ (say). Now calculate the values of R_1 and C_f so that $R_1 C_1 = R_f C_f$.

Example 4.3

(a) Design an op-amp differentiator that will differentiate an input signal with f_{max} = 100 Hz.
(b) Draw the output waveform for a sine wave of 1V peak at 100 Hz applied to the differentiator.
(c) Repeat part (b) for a square wave input.

Solution

(a) select, $f_a = f_{max} = 100\ \text{Hz} = \dfrac{1}{2\pi R_f C_1}$ [from Eq. (4.71)]

Let $C_1 = 0.1\ \mu\text{F}$,

then $R_f = \dfrac{1}{2\pi (10^2)(10^{-7})} = 15.9\ \text{k}\Omega$

Now choose $f_b = 10 f_a$

$= 1\ \text{kHz}$

$= \dfrac{1}{2\pi R_1 C_1}$ [from Eq. (4.74)]

Therefore, $R_1 = \dfrac{1}{2\pi (10^3)(10^{-7})} = 1.59\ \text{k}\Omega$

Since $R_f C_f = R_1 C_1$,

we get, $C_f = \dfrac{1.59 \times 10^3 \times 10^{-7}}{15.9 \times 10^3} = 0.01\ \mu\text{F}$

(b) $v_i = 1 \sin 2\pi(100)t$

From Eq. (4.69),

$$v_o = -R_f C_1 \frac{dv_i}{dt}$$

$$= -(15.9\ \text{k}\Omega)\ (0.1\mu\text{F})\ \frac{d}{dt}[(1\ \text{V}) \sin (2\pi)\ (10^2)\ t]$$

$$= -(15.9\ \text{k}\Omega)\ (0.1\ \mu\text{F})\ (2\pi)\ (10^2) \cos [(2\pi)\ (10^2)t]$$

$$= -0.999 \cos [2\pi\ (10^2)t]$$

$$= -1 \cos [(2\pi)\ (10^2)\ t]$$

The input and output waveforms are shown in Fig. 4.22 (a).

(c) For a square wave input, say 1V peak and 1 KHz, the output waveform will consist of positive and negative spikes of magnitude V_{sat} which is approximately 13V for ± 15V op-amp power supply. During the time periods for which input is constant at ± 1V, the differentiated output will be zero. However, when input transits between ± 1V levels, the slope of the input is infinite for an ideal square wave. The output, therefore, gets clipped to about ± 13V for a ± 15V op-amp power supply as shown in Fig. 4.22 (b).

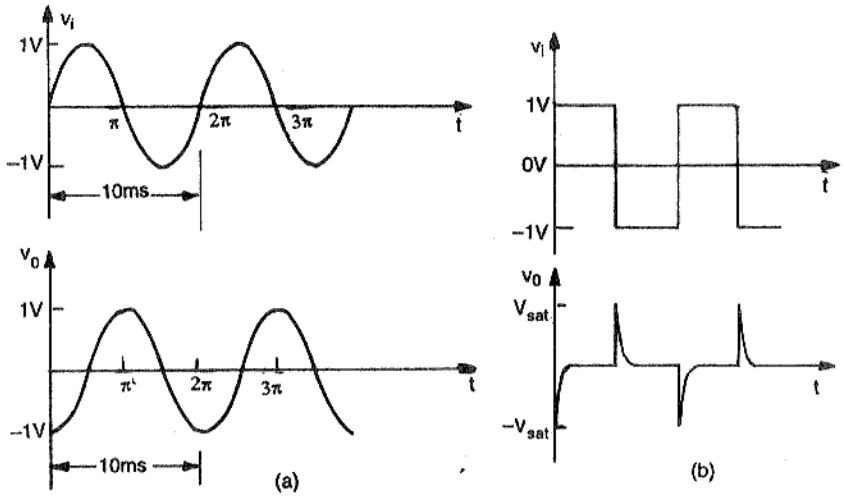


Fig. 4.22 (a) Sine-wave input and cosine output (b) Square wave input and spike output

4.11 INTERGATOR

If we interchange the resistor and capacitor of the differentiator of Fig. 4.21 (a), we have the circuit of Fig. 4.23 (a) which as we will see, is an integrator. The nodal equation at node N is,

$$\frac{v_i}{R_1} + C_f \frac{dv_o}{dt} = 0 \qquad (4.77)$$

or, $$\frac{dv_o}{dt} = -\frac{1}{R_1 C_f} v_i$$

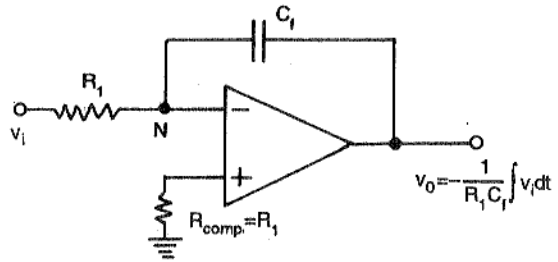


Fig. 4.23 (a) Op-amp integrator

Integrating both sides, we get,

$$\int_0^t dv_o = -\frac{1}{R_1 C_f} \int_0^t v_i\, dt$$

$$v_o(t) = -\frac{1}{R_1 C_f}\int_0^t v_i(t)\,dt + v_o(0) \tag{4.78}$$

where $v_o(0)$ is the initial output voltage.

The circuit, thus provides an output voltage which is proportional to the time integral of the input and R_1C_f is the time constant of the integrator. It may be noted that there is a negative sign in the output voltage, and therefore, this integrator is also known as an inverting integrator. A resistance, $R_{comp} = R_1$ is usually connected to the (+) input terminal to minimize the effect of input bias current.

A simple low pass RC circuit can also work as an integrator when time constant is very large. This requires very large values of R and C. The components R and C cannot be made infinitely large because of practical limitations. However, in the op-amp integrator of Fig. 4.23, by Miller's theorem, the effective input capacitance becomes $C_f(1 - A_v)$ where A_v is the gain of the op-amp. The gain A_v is infinite for an ideal op-amp, so the effective time constant of the op-amp integrator becomes very large which results in perfect integration.

The operation of the integrator can also be studied in the frequency domain. In phasor notation, Eq. (4.78) can be written as

$$V_o(s) = -\frac{1}{sR_1C_f}V_i(s) \tag{4.79}$$

In steady state, put $s = j\omega$ and we get

$$V_o(j\omega) = -\frac{1}{j\omega R_1C_f}V_i(j\omega) \tag{4.80}$$

So, the magnitude of the gain or integrator transfer function is

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \left|-\frac{1}{j\omega R_1C_f}\right| = \frac{1}{\omega R_1C_f} \tag{4.81}$$

The frequency response (or Bode Plot of this basic integrator is shown in Fig. 4.23 (b). The Bode plot is a straight line of slope –6B/octave (or equivalently – 20 dB/decade). The frequency f_b in Fig. 4.23 (b) is the frequency at which the gain of the integrator is 0 dB and is given by

$$f_b = \frac{1}{2\pi R_1C_f}$$

It can further be seen from Eq. (4.81) that at $\omega = 0$, the magnitude of the integrator transfer function is infinite. At dc, the capacitor C_f behaves as an open circuit and there is no negative feedback. The op-amp thus operates in open loop, resulting in an infinite gain. In practice, of course, output never becomes infinite, rather the output of the

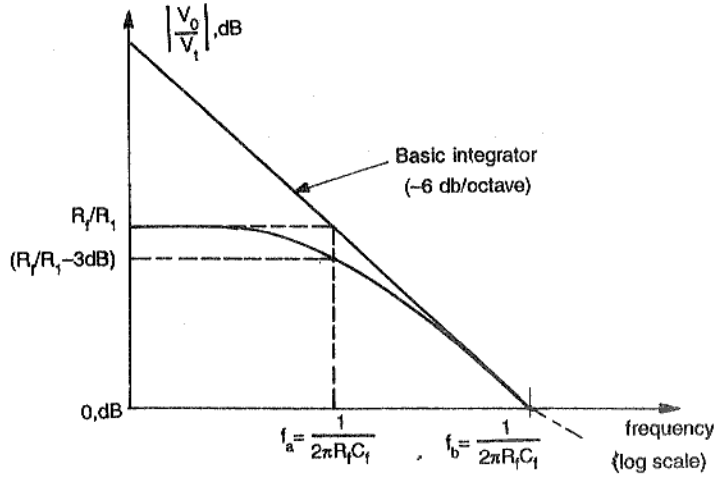


Fig. 4.23 (b) Frequency response of a basic and Lossy integrator

amplifier saturates at a voltage close to the op-amp positive or negative power supply depending on the polarity of the input dc signal.

As the gain of the integrator decreases with increasing frequency, the integrator circuit does not have any frequency problem as faced in a differentiator. However, at low frequencies such as at dc ($\omega \equiv 0$), the gain becomes infinite (or saturates). The solution to this problem is discussed in the following.

Practical Integrator Circuit (Lossy Integrator)

The gain of an integrator at low frequency (dc) can be limited to avoid the saturation problem if the feedback capacitor is shunted by a resistance R_f as shown in Fig. 4.23 (c). The parallel combination of R_f and C_f behaves like a practical capacitor which dissipates power unlike an ideal capacitor. For this reason, this circuit is also called a lossy integrator. The resistor R_f limits the low frequency gain to $-R_f/R_1$ (generally $R_f = 10\ R_1$) and thus provides dc stabilization.

Analysis

The nodal equation at the inverting input terminal of the op-amp of Fig. 4.23 (c) is,

$$\frac{V_i(s)}{R_1} + s\,C_f\,V_o(s) + \frac{V_o(s)}{R_f} = 0 \tag{4.82}$$

from which we have,

$$V_o(s) = -\frac{1}{sR_1C_f + R_1/R_f}V_i(s) \tag{4.83}$$

If R_f is large, the lossy integrator approximates the ideal integrator. For $s = j\omega$, magnitude of the gain of lossy integrator is given by

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{1}{\sqrt{\omega^2 R_1^2 C_f^2 + R_1^2/R_f^2}} = \frac{R_f/R_1}{\sqrt{1+(\omega R_f C_f)^2}} \qquad (4.84)$$

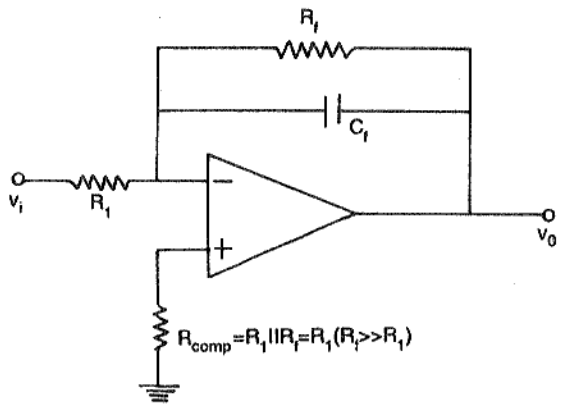


Fig. 4.23 (c) Practical or lossy integrator circuit

The Bode plot of the lossy integrator is also shown in Fig. 4.23 (b). At low frequencies gain is constant at R_f/R_1. The break frequency ($f = f_a$) at which the gain is 0.707 (R_f/R_1) (or – 3dB below its value of R_f/R_1) is calculated from Eq. (4.84) as

$$\sqrt{1+(\omega R_f C_f)^2} = \sqrt{2}$$

Solving for $f = f_a$, we get

$$f_a = \frac{1}{2\pi R_f C_f}$$

This is a very important frequency. It tells us where the useful integration range starts. If the input frequency is lower than f_a the circuit acts like a simple inverting amplifier and no integration results. At input frequency equal to f_a, 50% accuracy results. The practical thumb rule is that if the input frequency is 10 times f_a, than 99% accuracy can result.

Initial Conditions

An integrator must also be provided with an external circuit to introduce initial conditions as shown in Fig. 4.24. When ganged switch S is in position 1, the input is zero and the capacitor is charged to the voltage V almost instantaneously* setting an initial condition of

*In about four time constant, that is, 4 $R_o C_f$ where R_o is the small internal resistance of the voltage source V

v_o (0) = V. When the switch S is in position 2, the amplifier is connected as in integrator and its output will be V plus a constant $-1/R_1 C_f$ times the time integral of the input voltage v_i. The capacitor C_f should have very low leakage and is usually a Teflon, Polystyrene or Mylar dielectric with typical capacitance value ranging from 0.001 to 10 μF is used.

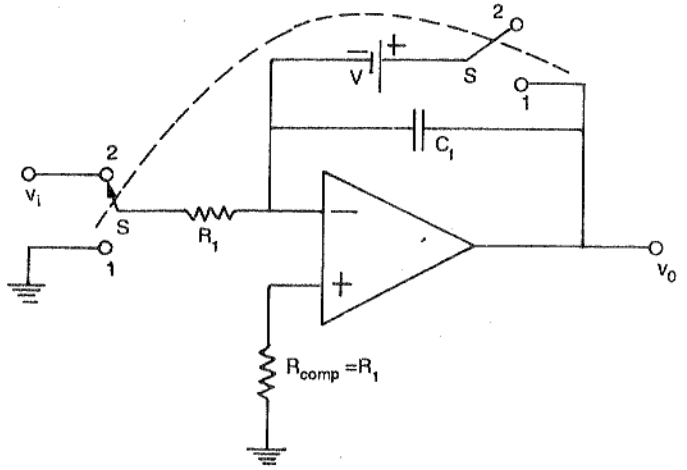


Fig. 4.24 Integrator circuit showing initial condition

Example 4.4

Consider the lossy integrator shown in Fig. 4.23 (c). For the component values. R_1 = 10 kΩ, R_f = 100 kΩ, C_f = 10 nF, determine the lower frequency limit of integration and study the response for the inputs (i) sine wave, (ii) step input (iii) square wave.

Solution

For the given component values, the lower frequency limit of integration f_a is

$$f_a = \frac{1}{2\pi R_f C_f}$$

$$= \frac{1}{2\pi \times 100\ \text{K} \times 10\ nF}$$

$$= 159\ \text{Hz}$$

For 99% accuracy, the input frequency should be at least one decade above f_a i.e., 1.59 KHz. Accurate integration can be achieved beyond this frequency. However, there is an upper limit up to which circuit will integrate and it is determined by the frequency response of op-amp. However, as input frequency is increased, the output amplitude reduces as the gain of the integrator falls at a rate of 6 dB/octave.

Sine wave input: For an input of 1V peak sine wave at 5 kHz, the output v_0 is

$$v_0(t) = -\frac{1}{R_1 C_f}\int v_i(t)\,dt$$

$$= -\frac{1}{10\ \text{k}\Omega \times 10\ nF}\int 1 \sin(2\pi\, 5000\, t)\,dt$$

$$= -10^4 \int \sin(2\pi\, 5000\, t)\,dt$$

$$= -\frac{10^4}{2\pi\, 5000}\left[-\cos(2\pi\, 5000\, t)\right]$$

$$= 0.318 \cos(2\pi\ 5000\ t)$$

The output is a cosine wave with a peak amplitude of 0.318 V only as shown in Fig. 4.25 (a). It the frequency of the input were raised by a factor of 10 to 50 kHz, the output would be a cosine wave of frequency 50 KHz but with an amplitude of 31.8 mV only.

Step input: If input is a step voltage $v_i = 1$V for $o \le t \le 0.3$ ms, then the output voltage at $t = 0.3$ ms is

$$v_o = -\frac{1}{R_1 C_f}\int_0^{0.3\ \text{ms}} 1.\,dt$$

$$= -\frac{1}{10\ \text{k}\Omega \times 10\ nF} \times t\Big|_{t=0}^{t=0.3\ \text{ms}}$$

$$= -10^4 \times 0.3 \times 10^{-3}$$

$$= -3\text{V}$$

The output voltage is a ramp function with a slope of 10 V/ms and is shown in Fig. 4.25 (b).

Square wave input: The output waveform for an input of 5 KHz, 1 V peak square wave is shown in Fig. 4.25 (c).

It can be seen that input is of constant amplitude of 1V from 0 to 0.1 ms and -1V from 0.1 ms to 0.2 ms. The output for each of these half periods will be ramps as seen above for step inputs. Thus, the expected output wave form will be a triangular wave. The peak value of the output for first half cycle is

$$v_o = -\frac{1}{R_1 C_f}\int_0^{0.1\ \text{ms}} 1.\,dt$$

$$= -10^4 \times 0.1 \times 10^{-3}$$

$$= -1\text{V}$$

This represents the total change in the output voltage over the first half cycle from 0 to 0.1 ms. Similarly, integration over the next half cycle produces a positive change of 1V.

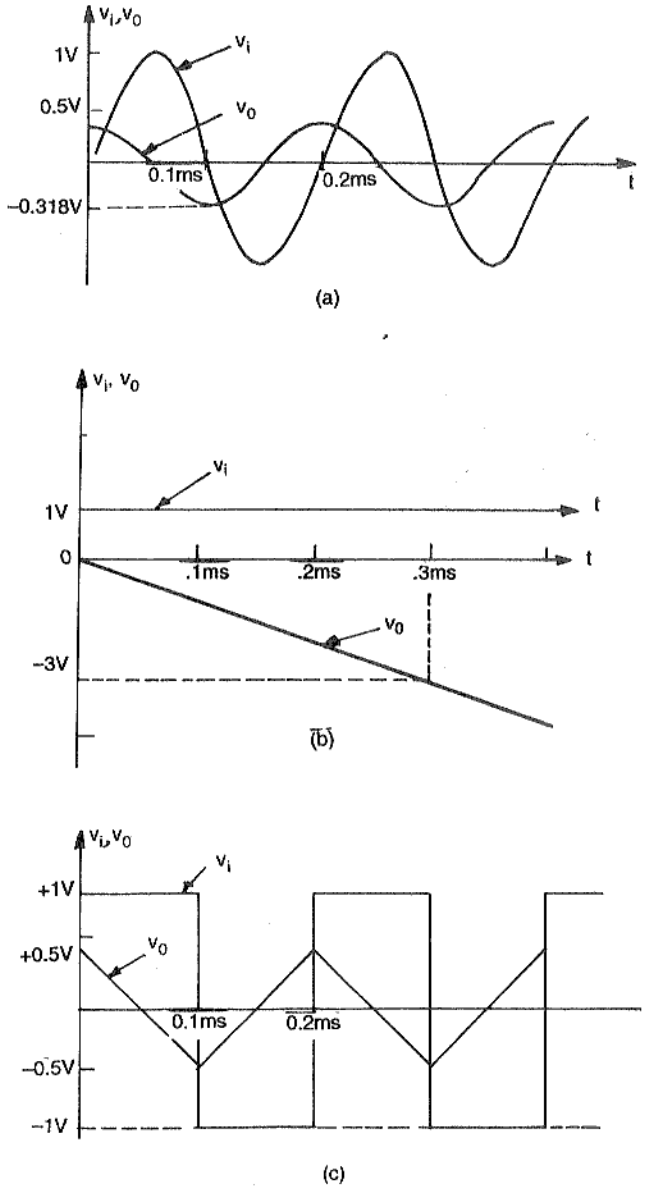


Fig. 4.25 Input and output wave forms for the integrator in Example 4.4 (a) Sine wave input (b) Step Input (c) Square wave input

Example 4.5

Find R_1 and R_f in the lossy integrator so that the peak gain is 20 dB and the gain is 3 dB down from its peak when $\omega = 10{,}000$ rad/s. Use a capacitance of 0.01 μF.

Solution

From Eq. (4.84) we see that gain is at its peak when $\omega = 0$. The peak value in dB is therefore,

$$A\,(\text{dB}) = 20 \log_{10} \frac{R_f/R_1}{\sqrt{1+0}} = 20 \qquad \text{(given)}$$

or, $$\log_{10} \frac{R_f}{R_1} = 1$$

Thus we have, $$\frac{R_f}{R_1} = 10$$

or, $$R_1 = \frac{R_f}{10}$$

At $\omega = 10^4$ rad/s, gain in dB is down by 3 dB from its peak of 20 dB, and thus is 17 dB. Therefore, converting gain to dB in Eq. (4.84) and substituting for ω, C and R_f/R, we have

$$20 \log_{10} \frac{10}{\sqrt{1+[(10^4)\,10^{-8}\,R_f]^2}} = 17 \text{ dB}$$

or, $$20 \log_{10} 10 - 20 \log_{10} \sqrt{1+(10^{-4}\,R_f)^2} = 17 \text{ dB}$$

This simplifies to

$$20 \log_{10} \left[1+(10^{-4}\,R_f)^2\right] = 3 \text{ dB}$$

or, $$1 + (10^{-4}\,R_f)^2 = 10^{3/10} = 2$$

Thus we have $$(10^{-4}\,R_f)^2 = 1$$

or, $$R_f = 10^4\ \Omega = 10\ \text{k}\Omega$$

and $$R_1 = 10\ \text{k}\Omega/10 = 1\ \text{k}\Omega$$

Example 4.6

Show that the output of an op-amp integrator to a step input of magnitude V volts is given by

$$v_o = A_v V(1 - e^{-t/R_1 C_f(1-A_v)})$$

Compare this result with the output obtained from a low pass RC circuit.

Solution

Figure 4.26 is a simple op-amp integrator where Miller's theorem is applied across the feedback capacitor C_f. The input time constant $T = R_1 C_f\,(1 - A_v)$. Therefore,

$$v_i = V(1 - e^{-t/T}) \tag{4.86}$$

and $$v_o = A_v\, v_i = A_v V(1 - e^{-t/R_1 C_f(1-A_v)}) \tag{4.87}$$

or, $$v_o = A_v V\left[1 - \left(1 - \frac{t}{R_1 C_f (1-A_v)} - \frac{t^2}{2\left(R_1 C_f (1-A_v)\right)^2} - \ldots\right)\right]$$

$$= \frac{A_v V t}{R_1 C_f (1-A_v)}\left[1 - \frac{t}{2 R_1 C_f (1-A_v)} - \ldots.\right]$$

or, $$v_o \approx -\frac{V t}{R_1 C_f}\left[1 - \frac{t}{2R_1 C_f (1-A_v)}\right];\ \text{if } A_v >> 1 \tag{4.88}$$

Also we know that for a simple low pass RC integrating network (without op-amp) the output v_o for a step input of V becomes

$$v_o = V(1 - e^{-t/RC}) \tag{4.89}$$

For large RC, $$v_o \approx \frac{V t}{RC}\left(1 - \frac{t}{2RC}\right) \tag{4.90}$$

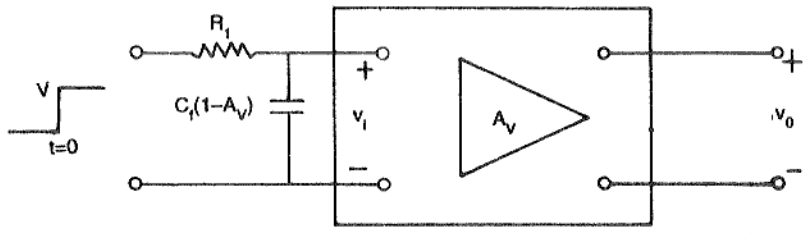


Fig. 4.26 Circuit for Example 4.6

It can be seen that the output voltage of both circuits varies approximately linearly with time (for a large RC) and for either case, $\frac{dv_o}{dt} = \frac{V}{RC}$. However, the second term in both the expressions represent deviation from the linearity. We see that op-amp integrator is more linear than the simple RC circuit by a factor of $1/(1 - A_v)$.

Example 4.7

For the circuit shown in Fig. 4.27 if the input is a constant V, show that the output $v_o(t)$ is given by a differential equation.

Solution

The transfer gain of the circuit is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{Z_f}{R_1} = -\frac{R_2 + \dfrac{R_3/sC}{R_3 + 1/sC}}{R_1}$$

$$= \frac{(R_2 + R_3) + sC R_2 R_3}{R_1 (1 + sC R_3)} \qquad (4.91)$$

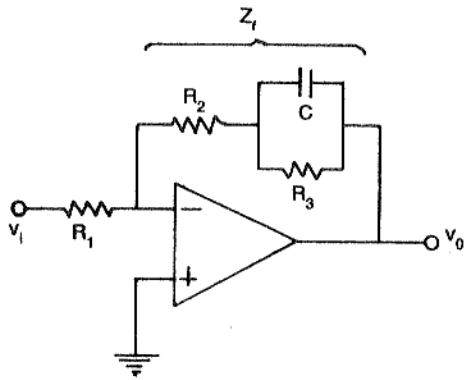


Fig. 4.27 Circuit for Example 4.7

or, $R_1(1 + s\,C\,R_3)\,V_o(s) + [(R_2 + R_3) + s\,C\,R_2R_3]\,V_i(s) = 0 \qquad (4.92)$

Writing Eq. (4.92) in time domain $\left(s \to \dfrac{d}{dt}\right)$, we get

$$R_1\left(1 + CR_3\frac{d}{dt}\right)v_o(t) + \left[(R_2 + R_3) + CR_2R_3\frac{d}{dt}\right]v_i(t) = 0 \qquad (4.93)$$

Since $v_i(t) = V$

Therefore, $\dfrac{dv_i(t)}{dt} = 0$

Hence $CR_1R_3\dfrac{dv_o}{dt} + R_1v_o + (R_2 + R_3)V = 0$

or, $$C\frac{dv_o}{dt} + \frac{v_o}{R_3} + \frac{V}{R_1} + \frac{R_2}{R_1R_3}V = 0 \qquad (4.94)$$

Example 4.8

Figure 4.28 shows a non-inverting integrator. Show that $v_o = \dfrac{1}{RC}\int v_i\,dt$.

Solution

The voltage at the (+) input terminal of the op-amp due to the potential divider is,

$$V(+) = \frac{1/sC}{R + 1/sC}V_i(s) \qquad (4.95)$$

The output voltage $V_o(s)$ for the non-inverting amplifier is

$$V_o(s) = \left(1 + \frac{1/sC}{R}\right)V(+)$$

$$= \frac{1}{sRC}V_i(s) \qquad (4.96)$$

Hence in time-domain, we get,

$$v_o = \frac{1}{RC}\int v_i\,dt$$

Note that there is no phase inversion in a non-inverting integrator.

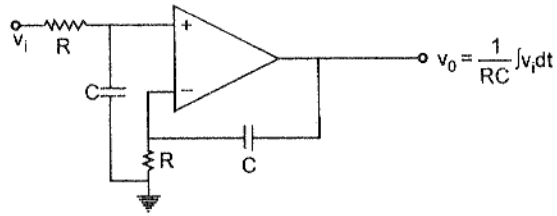


Fig. 4.28 Noninverting integrator circuit

4.12 ELECTRONIC ANALOG COMPUTATION

An analog computer performs linear operations such as multiplication by a constant, addition, subtraction and integration. Since these operations are sufficient for the solution of linear differential equation, it is possible to connect the various modules of an analog computer for obtaining the solution of differential equation.

We have already discussed the building blocks of the analog computer, that is, op-amp used as inverter, scale changer, summer, integrator, summing integrator etc. Potentiometer is widely used in analog computer to multiply voltages by a constant less than unity.

The symbolic representation of a summer, potentiometer and summing integrator is shown in Fig. 4.29 (a, b, c).

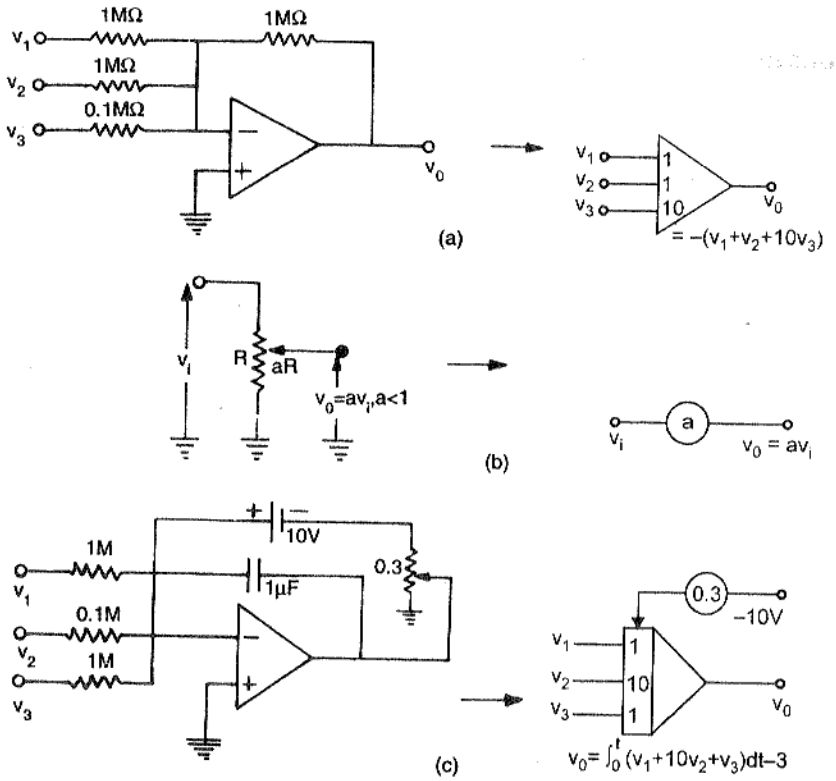


Fig. 4.29 (a) Summer and its symbolic representation (b) Potentiometer and its symbol. (c) Summing integrator and its symbol

Let us now see how an analog computer can be used to solve a second order differential equation given as,

$$\frac{d^2y}{dt^2} + 5.4\frac{dy}{dt} + 0.58\,y = u(t) \qquad (4.97)$$

with initial conditions,

$$y\,(0) = -\,4.8 \text{ and } \left.\frac{dy}{dt}\right|_{t=0} = \dot{y}(0) = 2.3$$

Rewrite Eq. (4.97) by keeping the highest order derivative on the left hand side and taking all other terms to the right side as

$$\ddot{y} = -5.4\,\dot{y} - 0.58\,y + u(t) \qquad (4.98)$$

Assuming $\ddot{y}$ is available, it may be successively integrated to obtain $\dot{y}$ and y as shown in Fig. 4.30 (a). At the output of amplifier 4, i.e. point B, we obtain the sum

$$-5.4\,\dot{y} - 0.58\,y + u(t)$$

which is precisely equal to $\ddot{y}$ with which we started in Eq. (4.98). Thus points A and B may be connected together to get the computer set-up for solving the given differential equation. The initial conditions $y(0) = -4.8$ and $\dot{y}(0) = 2.3$ have to be placed in the computer set-up with the help of the reference voltage (either $+V_{ref}$ or $-V_{ref}$ as required) and potentiometer. One has to be careful about the polarity of the reference voltage for setting up the initial condition. As in the computer set-up, the output of integrator 1 is $-\dot{y}$ which is initially set to –2.3 V to achieve $\dot{y}(0) = 2.3$ V. Similarly the output of integrator 2 is y which is initially set to – 4.8 V so that $y\,(0) = -\,4.8$ V.

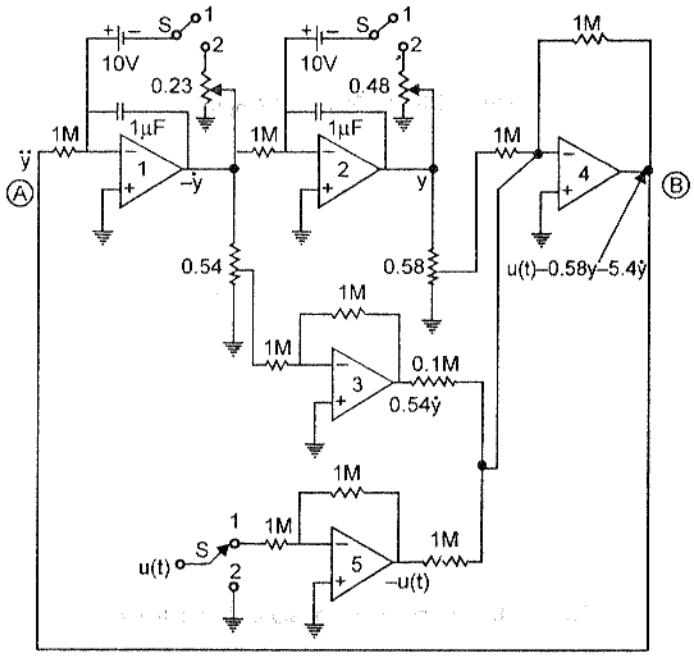


Fig. 4.30 (a) Simulation of 2nd order differential equation

The initial conditions are first established by putting the switch S in position 2. With S in position 1, the solution is obtained at the output terminal to which a CRO or plotter is connected.

Using the analog computer symbols, the set-up of Fig. 4.30 (a) is redrawn in Fig. 4.30 (b). Minimization of the components can be achieved using a summer integrator as shown in Fig. 4.30 (c).

The solution of Eq. (4.97) can also be obtained by using differentiators instead of integrators. However, the gain of a differentiator increases linearly with frequency and it tends to amplify noise, drift which may result in spurious oscillations. Therefore, integrators are invariably preferred over differentiators.

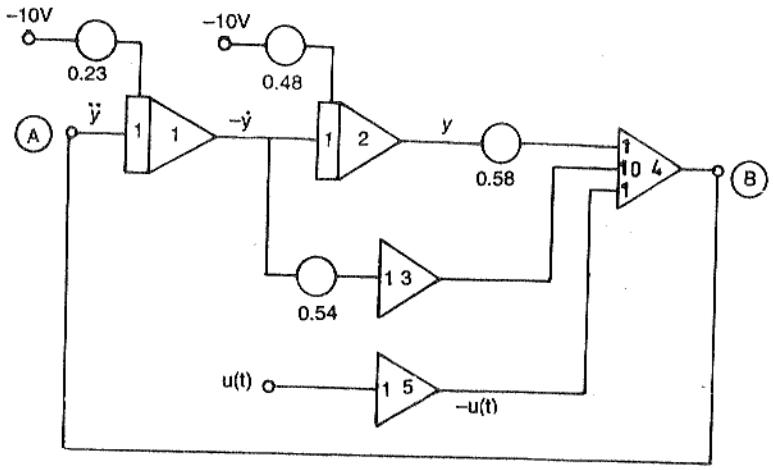


Fig. 4.30 (b) Symbolic diagram

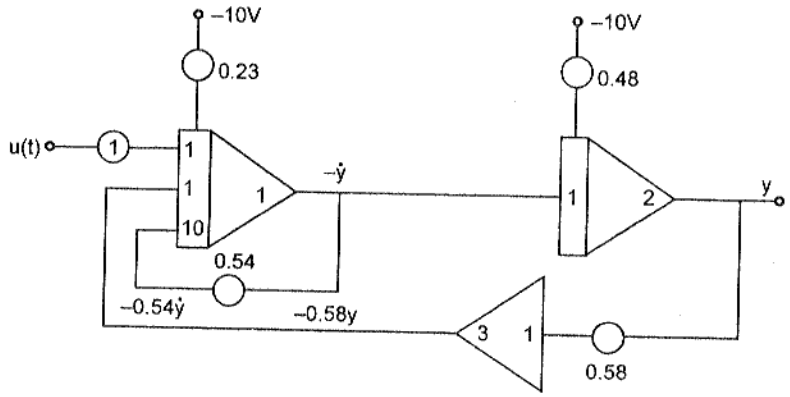


Fig. 4.30 (c) Minimum component simulation

Example 4.8

Set up an analog computer simulation to generate a sinusoidal signal 10 sin $3t$.

Solution

Let us first obtain a differential equation whose solution is 10 sin $3t$.

Let
$$x(t) = 10 \sin 3t$$
$$\dot{x}(t) = 30 \cos 3t \qquad (4.99)$$
$$\ddot{x}(t) = -90 \sin 3t = -9x$$

The required differential equation is,

$$\ddot{x} + 9x = 0$$

and the initial conditions are obtained from Eq. (4.99) putting $t = 0$ as,

$$x(0) = 0, \ \dot{x}(0) = 30$$

Assuming that $\ddot{x}$ is available, $x(t)$ can be obtained by integrating x twice. The computer set up is shown in Fig. 4.31.

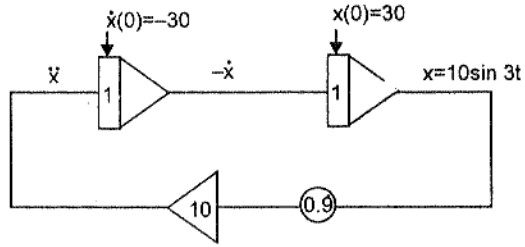


Fig. 4.31 Simulation of 10 sin $3t$

Simultaneous Equations

A set of simultaneous equations in two unknowns can also be solved using analog simulation. Consider two first order differential equations:

$$\frac{dx}{dt} = -a_1 x - b_1 y + c_1 f \qquad (4.100)$$

and
$$\frac{dy}{dt} = -a_2 x - b_2 y + c_2 f \qquad (4.101)$$

where x and y are unknown variables, f is the input and all coefficients are known constants. Equations (4.100) and (4.101) may be simulated separately as shown in Fig. 4.32 (a) and (b). Now interconnect the two systems to get the unknown x and y as shown in Fig. 4.32 (c).

The simulation procedure can be extended to any number of simultaneous equations.

Simulation of Transfer Functions

Another important problem that one come across is to develop a circuit that has a given transfer function. As an example, in the design of an electric filter consider a first order transfer function,

$$H(s) = \frac{V_o}{V_i} = \frac{-K}{s + a} \qquad (4.102)$$

so,
$$V_o(s + a) = -KV_i$$

or,
$$-s\,V_o = a\,V_o + K\,V_i \qquad (4.103)$$

which may be written in time-domain as,

$$v_o = -\int (a v_o + K v_i) \, dt$$

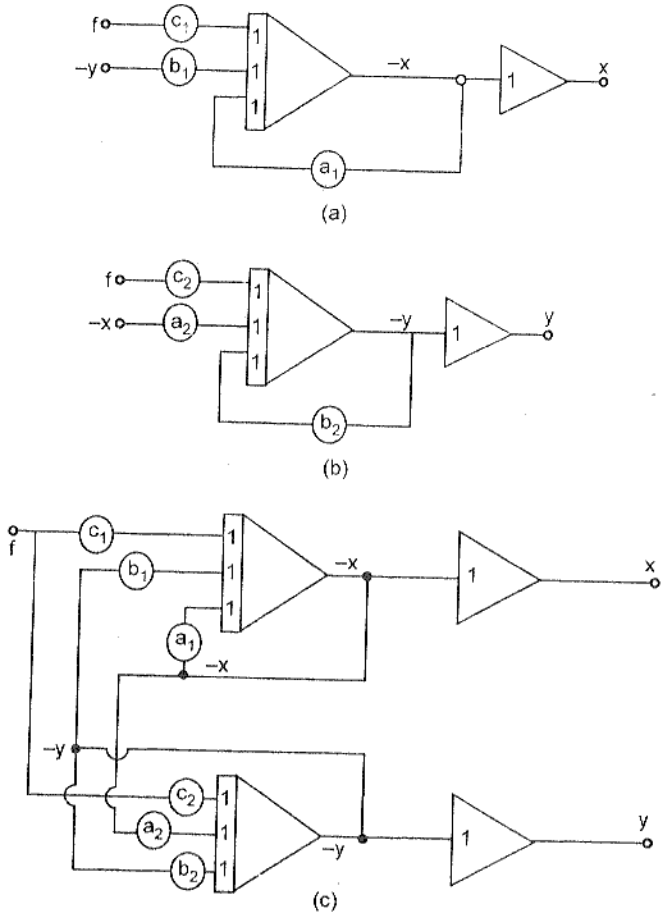


Fig. 4.32 (a) Simulation of Eq. (4.100) (b) Simulation of Eq. (4.101) (c) Final circuit

Thus we need a summing integrator and its simulation is shown in Fig. 4.33 (a). The corresponding electric circuit is shown in Fig. 4.33 (b).

In another example, let us simulate the transfer function

$$\frac{V_o}{V_i} = \frac{K(s+a)}{s^2 + sb + c} \tag{4.105}$$

which may be written in s-domain as,

$$s^2 V_o = -sbV_o - cV_o + Ks\,V_i + Ka\,V_i$$

or

$$-sV_o = bV_o - K\,V_i - \frac{1}{s}(Ka\,V_i - cV_o) \tag{4.106}$$

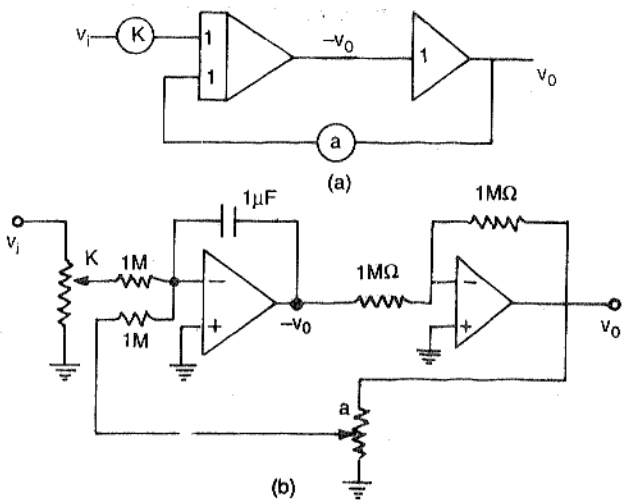


Fig. 4.33 (a) Simulation of transfer function $H(s) = -\frac{K}{s+a}$ (b) Electric circuit for (a)

Thus V_o is the output of an integrator whose input is $-sV_o$ which is the sum of the terms on the right side of Eq. (4.106). The term $-\frac{1}{s}$ $(Ka\,V_i - c\,V_o)$ is the output of an integrator whose inputs are KaV_i and $-c\,V_o$ as shown in Fig. 4.34 (a). The complete circuit is shown in Fig. 4.34 (b).

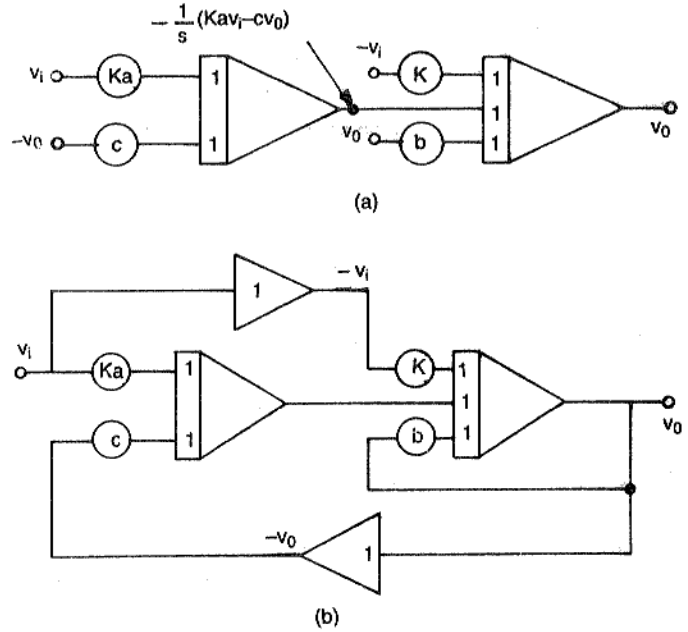


Fig. 4.34 (a) Preliminary simulation (b) Final simulation

4.13 MONOLITHIC POWER AMPLIFIERS

A wide range of IC power amplifiers are commercially available. An industry standard op-amp such as 741 can deliver about 100 mW of power with no additional external components. National Semiconductor produces the two popular IC audio power amplifiers LM380 and LM384. The LM380 is designed to deliver 2.5 W (r.m.s) to a capacitively coupled 8Ω load whereas LM384 can deliver 5W power and both are available in DIP packages. Figure 4.35 (a, b) shows the pin configuration, block diagram of LM 380. A copper lead frame used with the central three pins (3, 4, 5, 10, 11 and 12) on either side of the DIP package forms a heat sink. Thus there is no need to use separate heat sink.

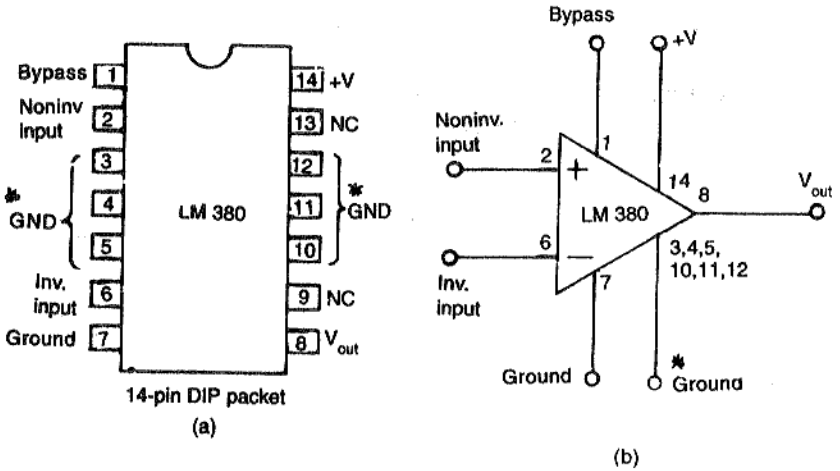


Fig. 4.35 (a) Pin configuration (b) block diagram

The use of LM380 as an audio power amplifier is shown in Fig. 4.36 (a). The IC can be used in both inverting and non-inverting configuration. In Fig. 4.36 (a), it is being used in non-inverting mode The inverting terminal (pin 6) can be either shorted to ground, left open or returned to ground through a resistor or capacitor. The capacitor C_2 is used to cancel the effects of inductance in the power supply leads. A lag compensating RC network must be connected from the output (pin 8) to ground to avoid oscillation.

The gain of LM380 is internally fixed at 50 but it is possible to get the gain increased upto 300, using positive feedback as shown in Fig. 4.36 (b). LM384 has the same connection diagram as that of LM380 except that it is designed to deliver 5W of power. Table 4.1 gives a list of monolithic audio power amplifiers with their output power ratings.

Table 4.1 Typical monolithic audio power amplifiers

Output power (W)	*IC Type*
1	MC1454
2	LM377 (dual)
4	LM378 (dual)
5	µA706
6	LM379 (dual)
8	TDA2002

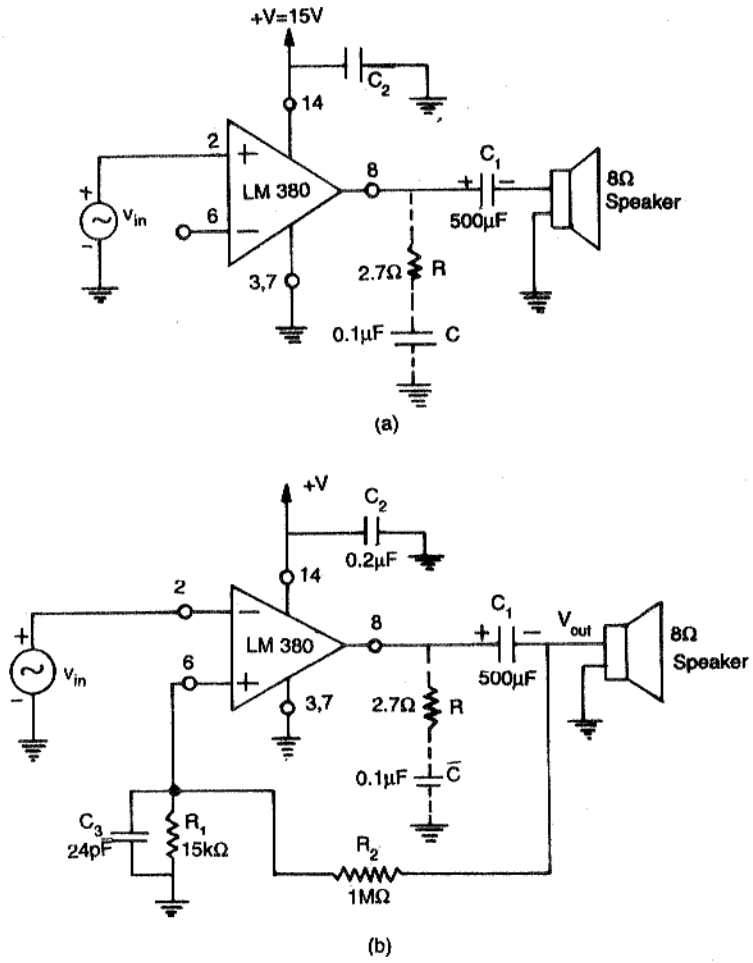


Fig. 4.36 (a) Audio power amplifier using LM380, (b) Use of positive feedback to increase gain

There are also available hybrid power amplifiers which supply more output power than is possible using monolithic power ICs. Some examples are: the Intersil's ICH 8510/8520/8530 and the Burr-Brown's

3573. The 3573 is desigred to deliver 100W peak or 40W continuous output power and can be used to drive dc and ac motors, electronic valves and push-pull solenoids.

4.14 OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

In Sec. 4.5, we have discussed the use of 741 op-amp as a voltage to current converter. A voltage to current converter is an amplifier which produces an output current proportional to an input voltage. The constant of proportionality is the transconductance of the amplifier and therefore such amplifiers are also known as transconductance amplifier. Due to wide applications, specially designed single chip transconductance amplifiers are available, called, operational transconductance amplifier (OTA). The symbolic representation of an OTA is shown in Fig. 4.37 (a). An OTA is a voltage-input, current-output device such that

$$I_o = g_m V_{in} = g_m (V_1 - V_2) \qquad (4.107)$$

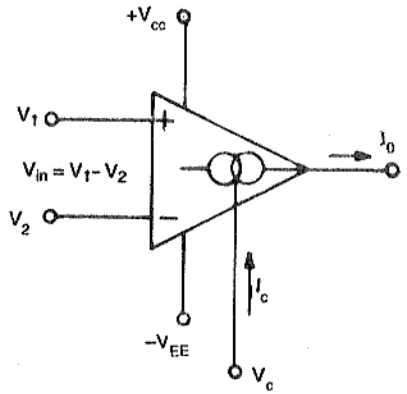


Fig. 4.37 (a) Symbol for OTA

where g_m is the transconductance, or gain of the OTA. The unique feature of an OTA is that it is possible to vary g_m over a wide range by means of an external control current. OTAs are used to implement programmable amplifiers and integrators in audio processing and electronic music synthesis. They are also used as current switches in sample-and-hold applications. Another important application of OTA using VLSI technique is in Neural networks. Popular OTAs are the CA3080 (RCA), the LMI 3600/700 (National Semiconductor) and the NE 5517 (Signetics).

The simplified internal circuit diagram of an OTA is shown in Fig. 4.37 (b). Transistors Q_1 and Q_2 form a differential pair. Current mirror $Q_3 - Q_4$ accepts the control current I_c which can be adjusted by an external resistance R_{ext} and control voltage V_c. Due to current mirror

$Q_3 - Q_4$, we get $I_1 = I_c$. The current I_1 is divided at the emitters of Q_1 and Q_2. Thus

$$I_1 + I_2 = I_4$$

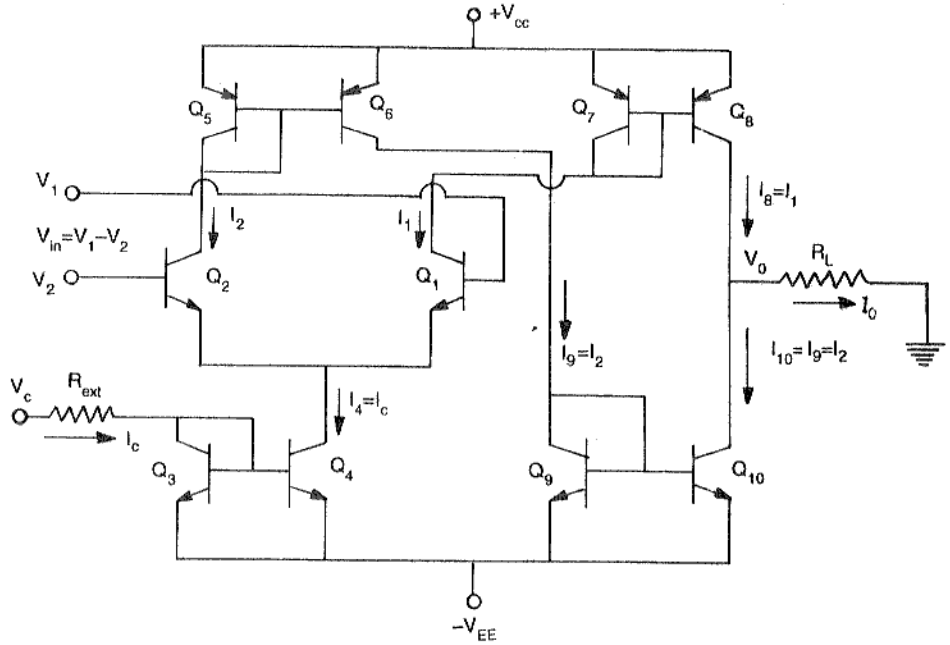


Fig. 4.37 (b) Simplified internal diagram of OTA

Current mirror $Q_5 - Q_6$ duplicates I_2 to yield $I_9 = I_2$. The current I_2 is in turn duplicated by current mirror $Q_9 - Q_{10}$ to produce $I_{10} = I_9 = I_2$. Similarly, current mirror $Q_7 - Q_8$ duplicates I_1 to yield $I_8 = I_1$. By KCL, we have,

$$I_o = I_8 - I_{10} = I_1 - I_2 \qquad (4.108)$$

Hence, the voltage gain A_v can be written as

$$A_v = \frac{V_o}{V_{in}} = \frac{I_o R_L}{V_{in}} = g_m R_L \qquad (4.109)$$

The transconductance g_m can be calculated as

$$I_1 = I_s \, e^{V_1/V_T} \qquad (4.110)$$

and

$$I_2 = I_s \, e^{V_2/V_T} \qquad (4.111)$$

where, I_s = reverse saturation current of transistor Q_1, Q_2 assumed to be equal and, V_T = volts equivalent of temperature

Now $$I_c = I_1 + I_2 = I_s\left[e^{V_1/V_T} + e^{V_2/V_T}\right] \qquad (4.112)$$

or, $$I_s = \frac{I_c}{e^{V_1/V_T} + e^{V_2/V_T}} \quad (4.113)$$

So, $$I_1 = \frac{I_c\, e^{V_1/V_T}}{e^{V_1/V_T} + e^{V_2/V_T}} \quad (4.114)$$

and $$I_2 = \frac{I_c\, e^{V_2/V_T}}{e^{V_1/V_T} + e^{V_2/V_T}} \quad (4.115)$$

Hence $$I_1 - I_2 = I_c \frac{e^{V_1/V_T} - e^{V_2/V_T}}{e^{V_1/V_T} + e^{V_2/V_T}} \quad (4.116)$$

Multiplying both the numerator and denominator by $e^{-\frac{V_1+V_2}{2}}$; Eq. (4.116) can be expressed in terms of voltage difference $(V_1 - V_2)$ as,

$$I_o = I_1 - I_2 = I_c \frac{e^{\frac{V_1-V_2}{2V_T}} - e^{-\frac{V_1-V_2}{2V_T}}}{e^{\frac{V_1-V_2}{2V_T}} + e^{-\frac{V_1+V_2}{2V_T}}} \quad (4.117)$$

$$= I_c \tanh\left(\frac{V_1 - V_2}{2V_T}\right) \quad (4.118)$$

A plot of output current I_o as a function of $(V_1 - V_2)$ is shown in Fig. 4.38. A transconductance amplifier basically computes a tan-hyperbolic. It operates linearly for a very small range of inputs and smoothly transits to saturation. The transconductance is given by

$$g_m = \left|\frac{\partial I_o}{\partial V_{in}}\right| = \frac{I_c}{2V_T} \quad (4.119)$$

$$\left(\text{with the assumption that for small } V_1 - V_2 ; \tanh\left(\frac{V_1 - V_2}{2V_T}\right) \approx \frac{V_1 - V_2}{2V_T}\right)$$

Then the voltage gain A_v is,

$$A_v = g_m R_L = \frac{I_c R_L}{2V_T} \quad (4.120)$$

Thus the voltage gain of the OTA circuit can be externally controlled by the control current I_c.

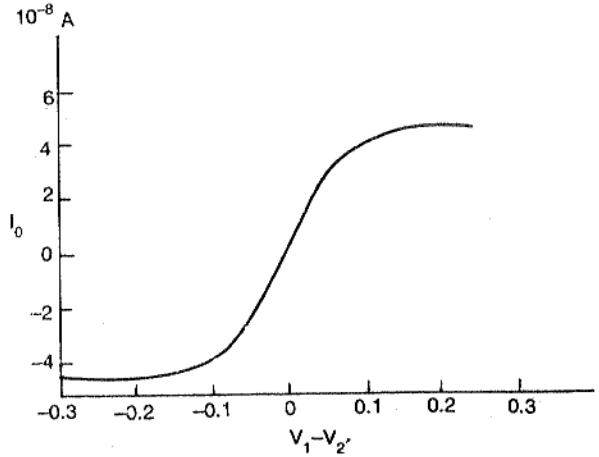


Fig. 4.38 Transfer characteristics of OTA

Figure 4.39 shows the schematic of widely used CA3080 OTA. Its transconductance or gain (g_m) is controlled by the current I_c driven into pin 5. At room temperature

$$g_m = \frac{I_c}{2V_T} = \frac{I_c}{2 \times 26\ \text{mV}}$$

where $V_T = 26$ mV at room temperature

or, $$g_m = \frac{19.2}{V} I_c \quad (4.121)$$

where V stands for volt as unit.
(The unit of transconductance g_m is Siemens)
This relationship holds linearly for 0.1 μA < I_c < 400 μA.

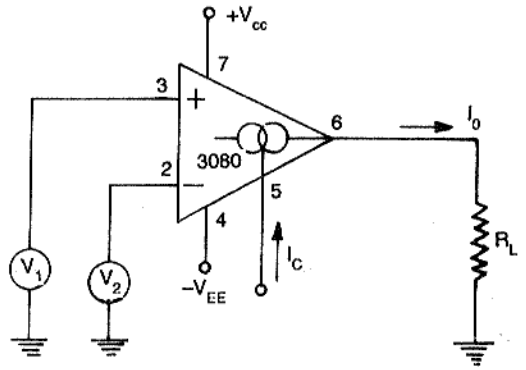


Fig. 4.39 Schematic of CA3080 OTA

From Eq. (4.107), we get

$$I_o = \left(\frac{19.2}{V} I_c\right) V_{in} \tag{4.122}$$

For CA3080, Eq. (4.122) is linear for $I_o < 400\ \mu A$ and $V_{in} < 20$ mV. If input voltage V_{in} becomes greater than 20 mV, Eq. (4.122) will no longer remain linear. So input voltage should be restricted to less than 20 mV. Another limitation is that since input signals are fed directly into the bases of the first stage, input impedance are of the order of 10 kΩ to 30 kΩ. To avoid loading, op-amp voltage followers should be used to buffer input signals.

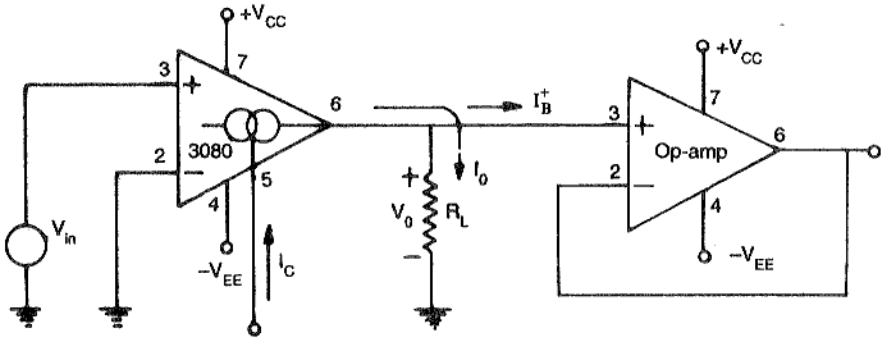


Fig. 4.40 Basic OTA voltage amplifier circuit

A basic OTA voltage amplifier is shown in Fig. 4.40. At room temperature, the output current is

$$I_o = \left(\frac{19.2}{V} I_c\right) V_{in}$$

If we assume that the entire I_o flows into the load resistor R_L, (i.e., $I_B^+ << I_o$), then

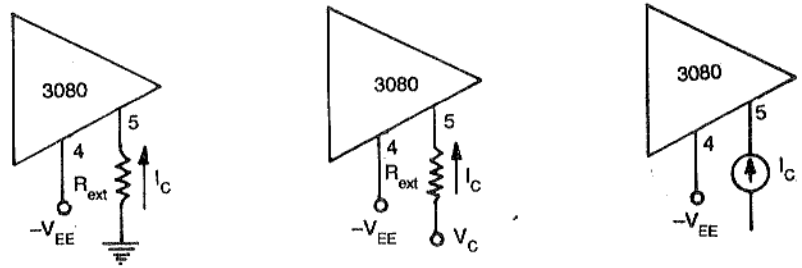
$$V_o = I_o R_L = \left(\frac{19.2\, I_c}{V}\right) V_{in} R_L \tag{4.123}$$

The output voltage depends upon the input voltage and the load resistor R_L. The voltage gain can be adjusted by varying R_L. However, we must use a voltage follower to avoid loading and select an op-amp for which bias-current (I_B^+) is much smaller than I_o. The control current I_c also affects the output. Figure 4.41 shows the various ways to set I_c. A fixed current I_c is obtained by connecting a resistance R_{ext} between pin 5 and ground as in Fig. 4.41 (a). The control current I_c can be written as,

$$I_c = \frac{|-V_{EE}| - 0.6\ V}{R_{ext}} \tag{4.124}$$

Here, 0.6 V is the forward voltage drop of the diode connected transistor Q_3 in Fig. 4.37 (b). In Fig. 4.41 (b), I_c is controlled by control voltage V_c and I_c is given by

$$I_c = \frac{V_c + |-V_{EE}| - 0.6\ V}{R_{ext}} \tag{4.125}$$



(a) Grounded (b) Control voltage (c) Current source

Fig. 4.41 Circuits for setting control current I_c

The control current I_c can be set directly with a current source as in Fig. 4.41 (c). This current source could be made with an FET, a BJT, an op-amp, an IC current source chip or another 3080.

An OTA can be viewed as a programmable resistor whose resistance is set by control current I_c. Since

$$I_o = \frac{19.2}{V} I_c V_{in}$$

The resistor $$R = \frac{V_{in}}{I_o} = \frac{V}{19.2\, I_c} = \frac{10.3\ mV}{I_c} \tag{4.126}$$

Figure 4.42 shows an electronically tuned resistor using two OTAs. The "resistance" expression for the circuit can be derived as follows:

For U_2,

$$I_{c2} = \frac{|-V_{EE}| - 0.6\ V}{R_{ext}} \approx \frac{|-V_{EE}|}{R_{ext}} \tag{4.127}$$

$$I_{o2} = \left(\frac{19.2}{V}\right) I_{c2} V_c = \frac{19.2}{V} \frac{|-V_{EE}|}{R_{ext}} V_c \tag{4.128}$$

For U_1,

$$I_{c1} = I_{o2}$$

and

$$I_o = \frac{19.2}{V} I_{c1} V_{in}$$

$$= \left(\frac{19.2}{V}\right)\left[\left(\frac{19.2}{V}\right)\frac{|-V_{EE}|}{R_{ext}}V_c\right]V_{in}$$

$$= \left[\left(\frac{19.2}{V}\right)^2\frac{|-V_{EE}|}{R_{ext}}\right]V_c V_{in} \qquad (4.129)$$

$$R = \frac{V_{in}}{I_o} = \frac{R_{ext}}{(369/V^2)|-V_{EE}|V_c} \qquad (4.130)$$

Thus the circuit of Fig. 4.42 can be considered as a voltage controlled resistance whose value is set in accordance with Eq. (4.130). However, V_{in} must be restricted to be less than 20 mV and I_o should be less than 400 μA.

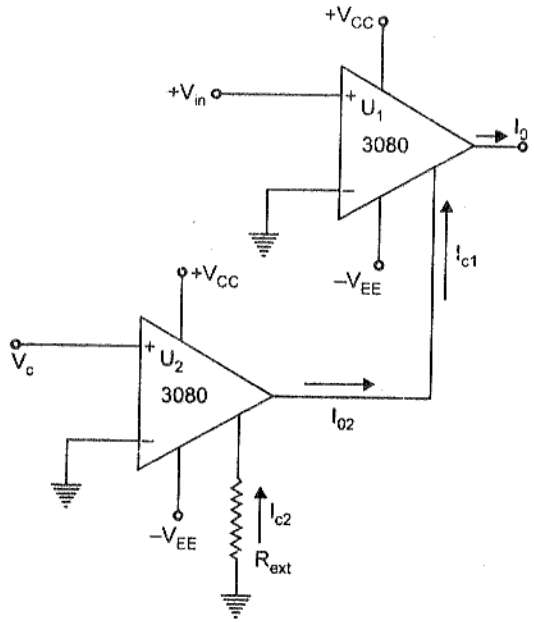


Fig. 4.42 Electronically tunable 'resistor' using two OTAs

The application of operational transconductance amplifier on sample-and-hold circuit is shown in Fig. 4.43. The control terminal is biased ***on*** ($= +V_{cc}$) and ***off*** ($= -V_{EE}$) to sample and hold an input signal across a holding capacitor. In the sample mode, the control voltage V_c is high, that is at $+V_{cc}$, and the output of the transconductance amplifier charges the holding capacitor C_H to a voltage equal to V_{in}. In the hold mode, I_c is reduced to zero, and the output of the OTA is at virtually open circuit so that the sampled input voltage is held on C_H. The

decay of the voltage across C_H during the hold mode depends upon the output impedance of the OTA and the input resistance of the buffer stage.

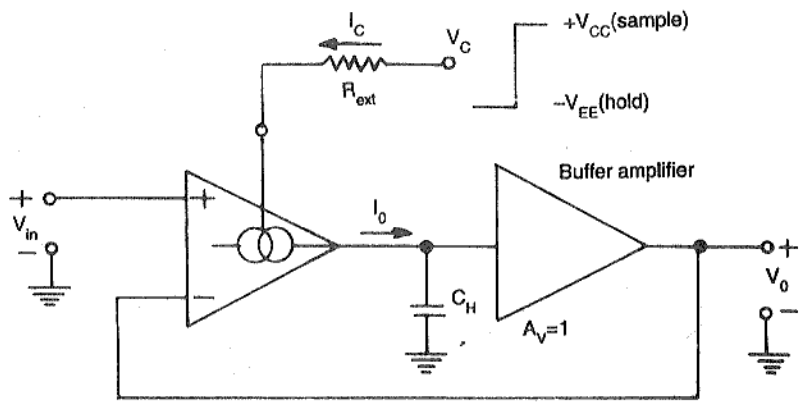


Fig. 4.43 Sample and hold circuit using OTA

There are a few basic limitations of OTAs. One is the severe restrictions on voltage and current magnitudes as already discussed. Another limitation is that as the control current I_c is varied to adjust gain or resistance, several other parameters of the amplifier are also affected. These include offset voltage, input bias current and slew-rate etc. To minimize these effects, input, output buffers and frequency compensating techniques may have to be used. Temperature also alters the performance of the OTA. The proportionality constant 19.2/V is valid only for room temperature. It may be noticed that the OTA performance is inversely proportional to temperature.

Summary

1. An op-amp can be used to perform mathematical operations such as scale changer, addition and subtraction.
2. An instrumentation amplifier is useful for amplifying low level signals which are obtained by sensing with a transducer in the measurement of physical quantities like temperature, water flow etc.
3. Op-amps can be used for amplifying both ac and dc inputs. A capacitively coupled amplifier is used for amplifying ac signals only.
4. The *V*-to-*I* converters are useful in low voltage dc and ac voltmeters, LED and zener diode testers.
5. The *I*-to-*V* converters are used for testing photo devices.
6. A diode in the feedback loop of an op-amp behaves as a precision diode as its cut-in voltage gets divided by the open-loop gain of op-amp.

7. A precision diode may be used for half-wave rectification, full wave rectification, peak-value detector, clipper and clamper.
8. A sample and hold circuit samples an input signal and holds on to its last sampled value until the input is sampled again. This circuit is used in analog to digital interfacing and pulse modulating systems.
9. Op-amp may be used to perform functions such as ln, log, antilog, multiply or divide signals.
10. The op-amp integrator and differentiator are useful for signal wave shaping.
11. Integrators are preferred over differentiators for analog computers as the gain of integrator decreases with increasing frequency and hence signal to noise ratio of integrator is higher than that of differentiator.
12. Monolithic audio power amplifiers with built in heat sink are available.
13. The operational transconductance amplifier (OTA) outputs a current proportional to its input voltage. OTAs are used to build programmable gain voltage amplifiers, voltage controlled resistances, neural networks etc.

Review Questions

4.1. Show with the help of circuit diagram an op-amp used as (i) scale changer, (ii) phase shifter, (iii) inverting adder and (iv) non-inverting adder. Draw an op-amp circuit whose output is $V_1 + V_2 - V_3 - V_4$.
4.2. What is an instrumentation amplifier? Draw a system whose gain is controlled by an adjustable resistance.
4.3. Explain the difference between the dc and ac amplifiers.
4.4. Draw and explain the operation of an ac voltage follower having very high input resistance.
4.5. Draw the circuit of a voltage to current converter if the load is (i) floating and (ii) grounded. Is there any limitation on the size of the load when grounded.
4.6. Draw and explain the operation of a current to voltage converter. If 741C is used, what is the lowest value of current that may be measured.
4.7. What is a precision diode?
4.8. Draw the circuit of a full-wave rectifier and explain how it gives the average value.
4.9. Name the circuit that is used to detect the peak value of the non-sinusoidal waveforms. Explain the operation.
4.10. Draw a sample and hold circuit. Explain its operation and indicate its uses.

4.11. Draw the circuit of a clipper which will clip the input signal below a reference voltage.
4.12. Draw the circuit of a log amplifier using two op-amps and explain its operation.
4.13. Indicate how two analog voltages are multiplied using log-antilog amplifiers.
4.14. Explain how to get the square and square root of the given analog signal.
4.15. What are the limitations of an ordinary op-amp differentiator. Draw the circuit of a practical differentiator that will eliminate these limitations.
4.16. Draw the circuit of a lossy integrator showing initial conditions.
4.17. Explain the difference between the integrator and differentiator and give one application of each.
4.18. Show the symbolic representation of the building blocks used in analog computer.
4.19. Explain why integrators are preferred over differentiators in analog computer.
4.20. Show the feedback arrangement to increase the gain of an audio power amplifier.
4.21. Discuss the application of OTA as programmable voltage amplifier and voltage controlled resistor.

PROBLEMS

4.1. (i) Find V_o in the circuit shown in Fig. P.4.1 if $R_f = 10$ kΩ, $R_1 = 2$ kΩ and $R_2 = 5$ kΩ.
(ii) Find R_1 and R_2 in Fig. P.4.1 if V_o is the average of V_1 and V_2 and $R_f = 10$ kΩ.

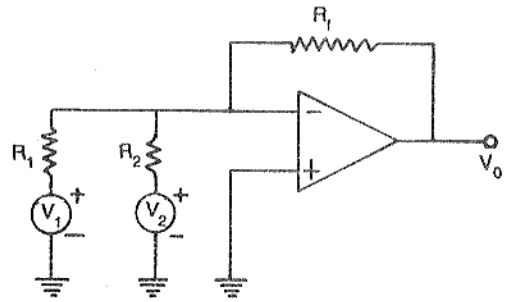


Fig. P. 4.1

4.2. Calculate V_o for the circuit of Fig. P.4.2. for $V_1 = 5$V, $V_2 = 2$V.
4.3. (i) In Fig. 4.2 (a), $V_1 = 0.1$ V, $V_2 = 0.2$ V, $V_3 = -0.3$ V, $R_1 = 4$ kΩ, $R_2 = 3$ kΩ, $R_3 = 1$ kΩ, $R_f = 4.7$ kΩ. Find output voltage V_o.
(ii) The circuit of Fig. 4.2 (b) is to be used as an averaging amplifier with the following specifications: $V_1 = V_2 = 1.5$V, $V_3 = 3$V, $R_1 = R_2 = R_3 = R = 1.5$ kΩ, and $V_o = 5$V. Determine the value of R_f.

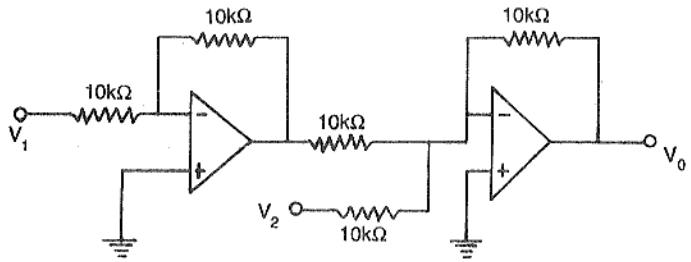


Fig. P. 4.2

4.4. In the circuit of Fig. P.4.4, it can be shown that

$$V_0 = a_1 V_1 + a_2 V_2 + a_3 V_3$$

Find the values of a_1, a_2 and a_3. Also find the value of V_0 if (i) R_4 is short circuited (ii) R_4 removed (iii) R_1 is short circuited.

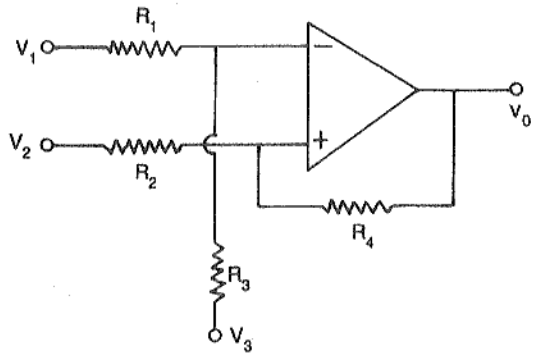


Fig. P. 4.4

4.5. Figure P. 4.5. shows a diff-amp with double ended output. Show that $V_0 = \frac{R_2}{R_1}(V_1 - V_2)$ where $V_0 = V_4 - V_3$.

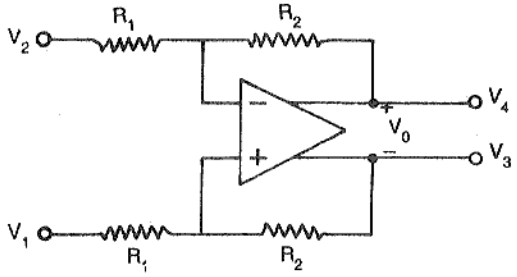


Fig. P. 4.5

4.6. For the instrumentation amplifier shown in Fig. P. 4.6. verify that,

$$V_0 = \left(1 + \frac{R_2}{R_1} + \frac{2R_2}{R}\right)(V_2 - V_1)$$

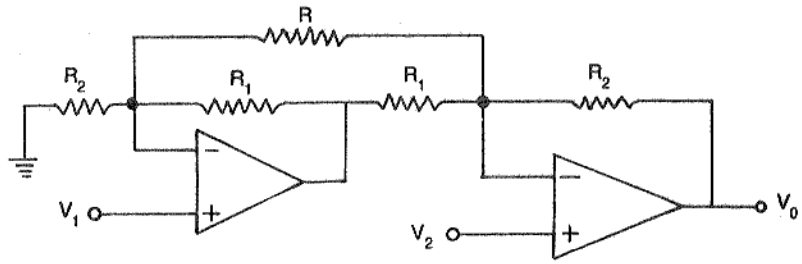


Fig. P. 4.6

4.7. In a peak detector of the type shown in Fig. 4.13 (a), $C = 0.01$ μF, $v_i = 2$ V pp square wave at 1 kHz. Draw the approximate output voltage waveform. Assume R_f for the diode = 100 Ω.

4.8. In the circuit shown in Fig. P.4.8. input is a sweep voltage $v_i = \alpha t$. Show that the output.

$$v_0 = -\alpha R' C - \alpha \frac{R'}{R} t$$

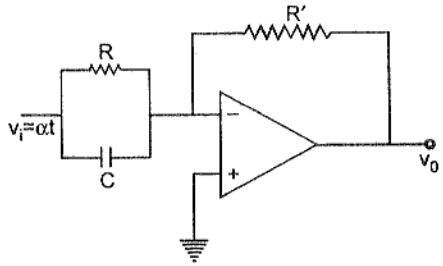


Fig. P. 4.8

4.9. The input v_i to a differentiator of Fig. 4.21 (a) is shown in Fig. P.4.9. Find the output v_0 if $R_f = 2$ kΩ and $C_1 = 0.1$ μF.

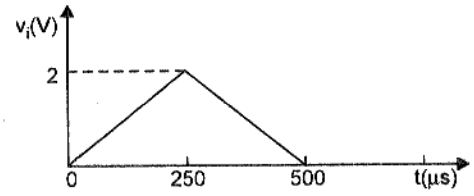


Fig. P. 4.9

4.10. In the integrator of Fig. 4.23, find the output v_0, if $R_1 = 10$ kΩ, $C_f = 0.02$ μF, $v_0(0) = 0$, and the input voltage is,

$$v_i = 4 \cos 10^4 t + 1$$

4.11. Find the gain in dB of the lossy integrator of Fig. 4.25 (a) if R_f = 10 kΩ, R_1 = 1 kΩ, C_f = 0.01 μF, for (a) ω = 0, (b) ω = 10,000 rad/s.

4.12. Find R_f and R_1 in Fig. 4.25 (a) so that the peak gain is 20 dB and the gain is 3 dB down from its peak when f = 10,000 Hz. Use a capacitor of 1 *nF*.

4.13. Prove that the circuit shown in Fig. P. 4.13 is a non-inverting integrator with $v_o = \frac{2}{RC}\int v_i\, dt$.

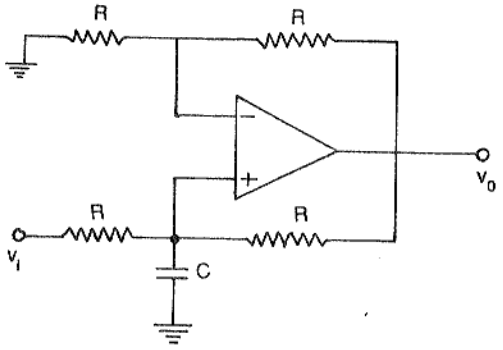


Fig. P. 4.13

4.14. An op-amp is used as an adder-integrator for two inputs V_1 and V_2. Two supply voltages + 10V and – 10V are available to allow for an initial output voltage which may be anywhere between – 5V and + 5V. Indicate the system using ganged switches so that in position 1, the initial condition is set and in position 2, the integration takes place.

4.15. Find the transfer function v_o/v_i of the circuit shown in Fig. P.4.15.

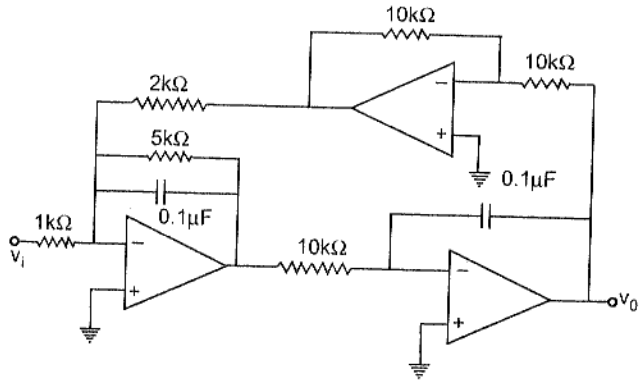
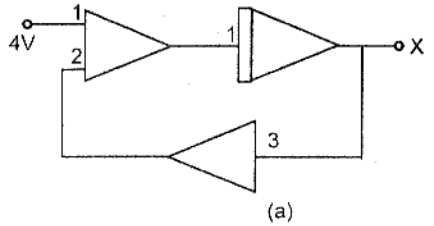
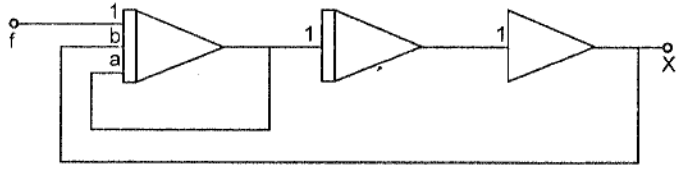


Fig. P. 4.15

4.16. Find the differential equation satisfied by the output X in the circuit of Fig. P. 4.16 (a, b).



(a)



(b)

Fig. P. 4.16

4.17. Set up a computer simulation to solve the differential equation,

$$\frac{d^2v}{dt^2} + 2v - 5\sin\omega t = 0$$

where, $v(0) = -1$ and $\dot{v}(0) = 0$

Simulate also the input sinewave.

Experiment 4.1

To demonstrate the operation of an inverting summing amplifier using 741 op-amp.

Procedure

1. Connect the circuit as shown in Fig. E. 4.1. (a).
2. Since it is usually not possible to have two signal generators for one experiment, op-amp 1 is used as a voltage follower to give two signals v_2 and v_1 shown in Fig. E. 4.1. (a). In this case, the two input signals v_1 and v_2 will be equal. Set the signal generator to give peak-to-peak voltage of 1 V at 100 Hz.
3. Measure the output voltage v_o using a CRO. The output should be

$$v_o = -\frac{R_f}{R_2}v_2 - \frac{R_f}{R_1}v_1$$

4. Observe the waveforms v_1, v_2 and v_o.

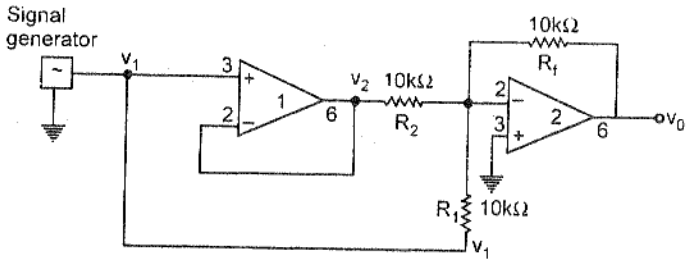


Fig. E. 4.1 (a) An inverting summing amplifier

5. Note the phase of the output voltage v_o with respect to input voltage.
6. If it is desired to add unequal voltages, use op-amp 1 as a non-inverting amplifier as shown in Fig. E. 4.1 (b). For the values chosen, the gain of the non-inverting amplifier will be 2.

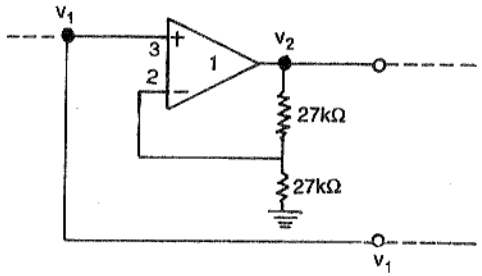


Fig. E. 4.1 (b) Op-amp '1' connected as non-inverting amplifier

7. Set the signal generator to give 1 V pp sine wave at 100 Hz.
8. Repeat step 3, 4 and 5.

Experiment 4.2

To demonstrate the operation of a Practical Differentiator

Design Aspects

Practical Differentiator

In Fig. E. 4.2. the resistor R_1 reduces the high frequency noise and capacitor C_f helps in suppressing oscillations. The circuit will provide reasonably accurate differentiation upto a frequency f_a, where,

$$f_a = \frac{1}{2\pi R_f C_1} \text{ Hz} \qquad \text{[See Eq. (4.71)]}$$

The values of R_1 and C_f should be chosen so that $f_b = 10\, f_a$ where,

$$f_b = \frac{1}{2\pi R_1 C_1} \qquad \text{[See Eq. (4.74)]}$$

and $$R_1 C_1 = R_f C_f$$

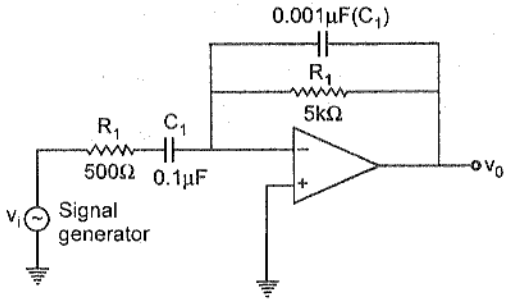


Fig. E. 4.2 A practical differentiator

For the given component values the highest frequency f_a or f_{max} up to which circuit will provide accurate differentiation is,

$$f_a = \frac{1}{2\pi R_f C_1} = \frac{1}{2\pi \times 5 \times 10^3 \times .01 \times 10^{-6}}$$

$$= 3.18 \text{ kHz}$$

Thus, if we give an input signal of frequency 3 kHZ, i.e.
If $v_i(t) = 1 \sin 2\pi\ 3000\, t$

$$\text{Then, } v_o = -\, R_f\, C_1 \frac{dv_i}{dt}$$

$$= -\, 5 \times 10^3 \times .01 \times 10^{-6}\ \frac{d\,(1 \sin 2\pi\ 3000\, t)}{dt}$$

$$= -\, 0.94 \cos 2\pi\ 3000t$$

The output waveform is also sinusoidal but it lags input by 90°. Note that the input frequency has not changed, but the amplitude has. The output amplitude of a differentiator is directly proportional to the input frequency, thus, if input frequency is changed to 1.5 kHZ, the output amplitude will be half the present value.

Procedure

(i) Connect the differentiator circuit shown in Fig. E. 4.2. Adjust the signal generator to produce a 5 volt peak sine wave at 100 Hz.
(ii) Observe input v_i and output v_o simultaneously on the oscilloscope. Measure and record the peak value of v_o and the phase angle of v_o with respect to v_i.
(iii) Repeat step (ii) while increasing the frequency of the input signal. Find the maximum frequency at which the circuit performs differentiation. Compare it with the calculated value of f_a.

Computer Program 4.2

The circuit of a practical differentiator shown in Fig. E. 4.2 has been redrawn in Fig. C. 4.2 (a) where various terminals have been numbered for writing the PSPICE program. The program listing is shown in Fig. C. 4.2 (b) and the output waveforms for a sinusoidal input of 3 kHZ is shown in Fig. C. 4.2 (c). It may be noted that the output is plotted after several cycles of the input has passed through to achieve steady state results.

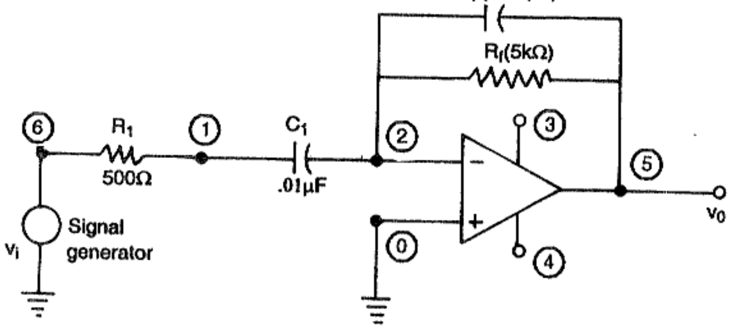


Fig. C 4.2 (a) Practical differentiator redrawn for PSPICE program

Fig. C 4.2 (b) Program Listing

```
*Practical Differentiator-sine wave input
* * * * Circuit Description
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
* * *
   R1  6  1  .5K
   C1  1  2  .01μF
   RF  2  5  5K
   CF  2  5  .001μF
*  Op-amp analysis
   X1  0  2  3  4  5  μA741
   .LIB  EVAL.LIB
*  Power supplies
   VCC  3  0  DC  15V
   VEE  0  4  DC  15V
*  Input signal source
   Vi  6  0  sin  (0  1V 3 kHz)
*  Output
   .TRAN  6US  6600US  6000US  .001MS
   .PROBE
   .END
```

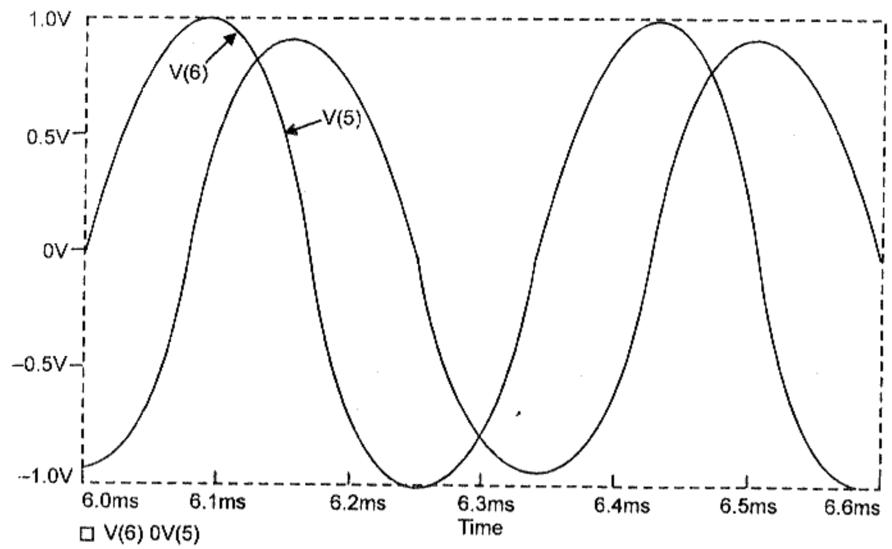



Fig. C 4.2 (c) Input and output waveforms of a practical differentiator

Experiment 4.3

To demonstrate the operation of a Lossy Integrator

Design Aspects

Fig. E. 4.3 (a) shows a lossy integrator designed in Example 4.4.

The resistor R_f (100 kΩ) is connected across the 0.01 μF capacitor to prevent the amplifier from saturation due to the presence of any dc offset in the input.

Choose $R_f C_f$ = period of the signal to be integrated = $1/f_a$ and R_f = 10 R_1.

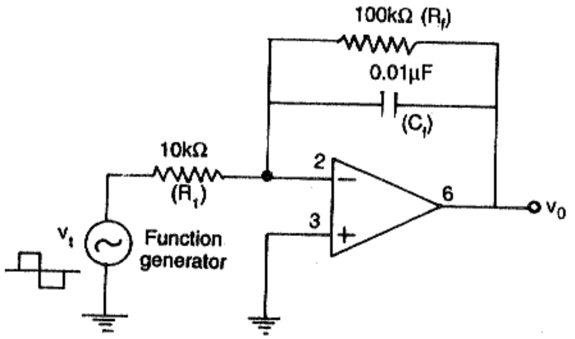


Fig. E. 4.3 (a) A Lossy integrator

For $f < f_a$, the circuit behaves as an inverting amplifier and output

$$v_o = -\frac{R_f}{R_1} v_i$$

For $f > f_a$ the circuit is an integrator and output

$$v_o = -\frac{1}{R_1 C_f} \int v_i \, dt$$

Procedure

(i) Connect the integrator circuit shown in Fig. E. 4.3 (a). Set the function generator to produce a square wave of 1 V peak-to-peak amplitude at 500 Hz. View simultaneously output v_o and input v_i.

(ii) Slowly adjust the input frequency until the output is a good triangular waveform. Measure the amplitude and frequency of the input and output waveforms.

(iii) Verify the following relationship between R_1C_f and input frequency f for good integration

$$f > f_a = \frac{1}{R_1 C_f}$$

(iv) Now set the function generator to a sine wave of 1 V peak-to-peak and frequency 500 Hz. Adjust the frequency of the input until the output is a negative going cosine wave. Measure the frequency and amplitude of the input and output waveforms.

Computer Program 4.3

The circuit diagram of the Lossy Integrator designed in Example 4.4 has been redrawn in Fig. C. 4.3 (a) with various nodes numbered for writing the PSPICE program. The program listing is shown in Fig. C. 4.3 (b). The response of the circuit for sine wave, step input and square wave input have been shown in Fig. C. 4.3 (c).

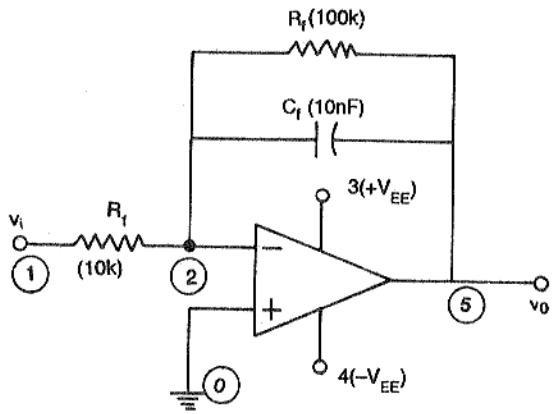
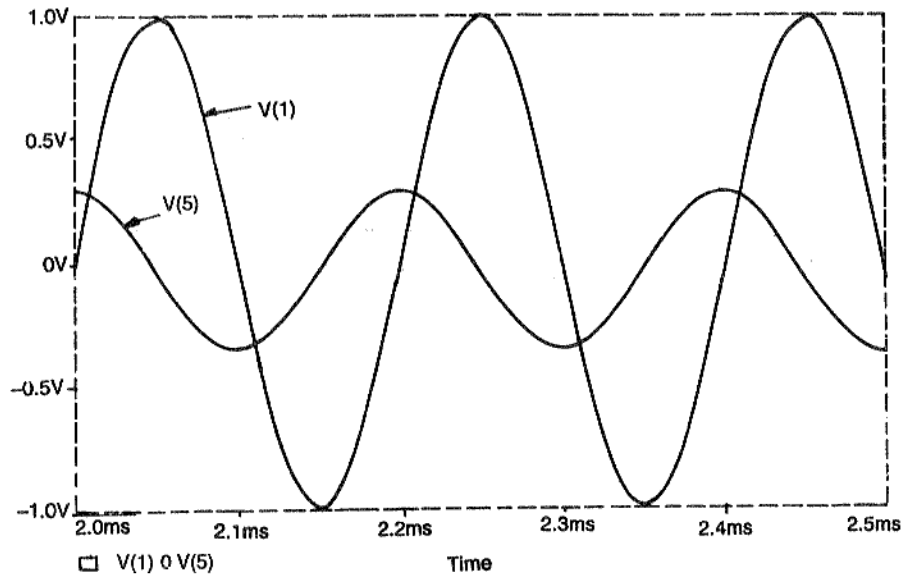


Fig. C 4.3 (a) Circuit for Program 4.3

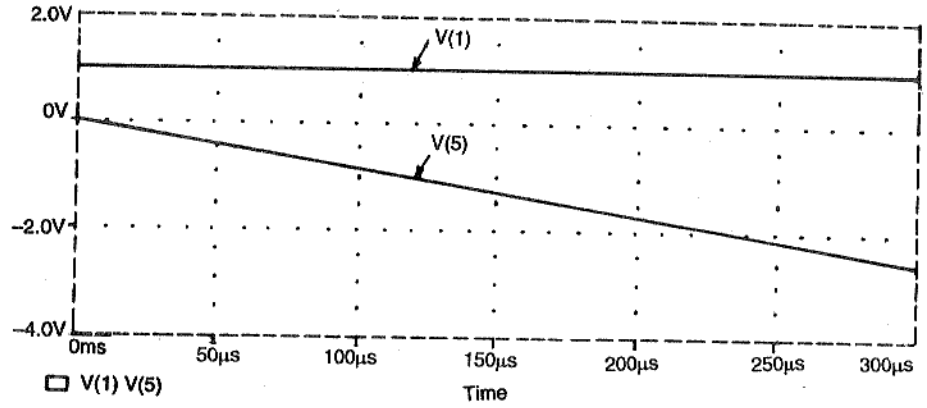
Fig. C. 4.3 (b): Program Listing

```
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*  A Lossy Integrator
   R1   1   2   10K
   RF   2   5   100K
   CF   2   5   10NF
*  Op-amp analysis
   X1   0   2   3   4   5   UA741
   .LIB EVAL.LIB
*  Power supplies
   VCC  3   0   DC   15V
   VEE  0   4   DC   15V
*  Sine wave input
   Vi   1   0   sin  (0   1V 5Khz)
*  Output for sinewave input
   .TRAN  .5MS  2.5MS  2MS  .001MS
*  Square Wave Input
*  Vi   1   0   PULSE (−1V 1V 0MS 0MS 0MS .IMS .2MS)
*  Output for square wave input
*  .TRAN  .2US  5MS  4MS  .001MS
*  Step Input
   * Vi 1 0 PULSE (0V 1V  0MS 0MS 0MS 1MS 1MS)
   * Output for step input
   * .TRAN  .2US  .3MS  0MS  .001MS
   .PROBE
   .END
```

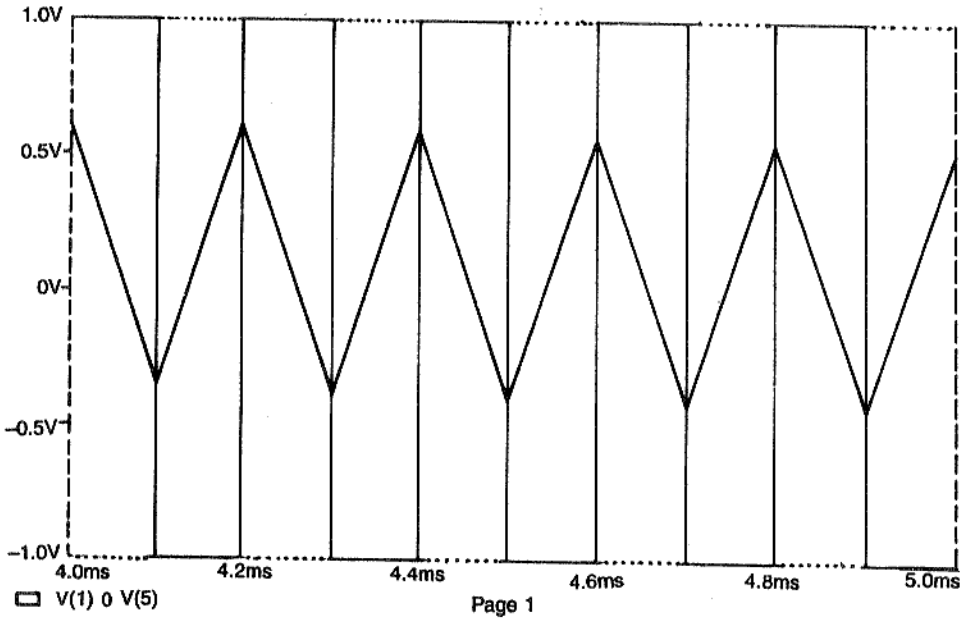


(i)

Fig. C 4.3 (c)



(ii)



(iii)

Fig. C 4.3 (c) Response to (i) Sine wave input
(ii) Step input
(iii) Square wave input

5

Comparators and Waveform Generators

5.1 INTRODUCTION

An operational amplifier in the open-loop configuration operates in a non-linear manner. There are a number of applications of op-amp in this mode, such as, comparators, detectors, limiters and digital interfacing devices namely converters. In this chapter, we shall discuss comparator and its applications.

5.2 COMPARATOR

A comparator is a circuit which compares a signal voltage applied at one input of an op-amp with a known reference voltage at the other input. It is basically an open-loop op-amp with output $\pm V_{sat}$ ($= V_{CC}$) as shown in the ideal transfer characteristics of Fig. 5.1 (a). However, a commercial op-amp has the transfer characteristics of Fig. 5.1 (b).

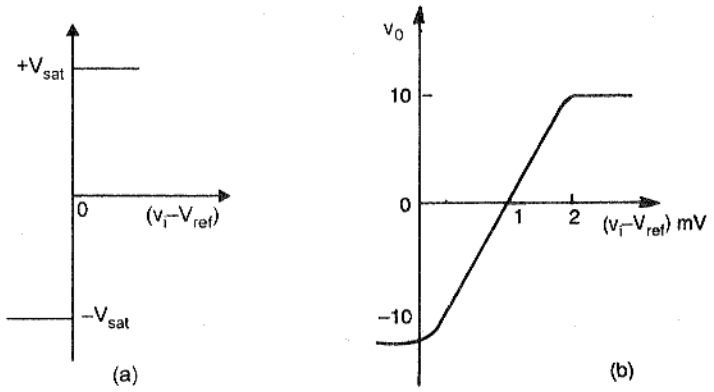


Fig. 5.1 The transfer characteristics (a) ideal comparator (b) practical comparator