

of op-amp has been explained. Various compensating techniques have also been discussed. Interpretation of important parameters in the data sheet is also featured in this Chapter.

A number of linear and nonlinear applications of operational amplifier such as adder, subtractor, integrator, differentiator, instrumentation amplifier, log/antilog amplifiers, multiplier, divider, analog computation techniques, clipper/clamper, sample and hold circuit are presented in Chapter 4. The various comparators—square, triangular and sine wave generators are discussed in Chapter 5. Chapter 6 deals with voltage regulator chips—fixed regulator, variable voltage regulator and switched mode power supply.

Active filters—low pass, high pass, band pass, band reject and state variable filters are discussed in Chapter 7. Switched capacitor filter and its realization are also described. Chapter 8 is devoted to 555-timer and its various applications. The phase locked loop-565, an important linear IC which is very useful in communications has been discussed in Chapter 9 with its detailed applications. In Chapter 10, the various analog to digital (A/D) and digital to analog (D/A) techniques are presented.

We wish to acknowledge a large number of students and colleagues who have contributed to this book. Thanks to Mr. Manav Sen of Solid State Physics Laboratory and Dr. B. Kumar of Delhi Institute of Technology for their valuable suggestions.

Our family members deserve very special thanks for their continued support, encouragement and patience throughout this project.

D. ROY CHOUDHURY  
SHAIL B. JAIN

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# Integrated Circuit Fabrication

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## 1.1 INTRODUCTION

We are going through a period of micro-electronic revolution. For a common person, the role of electronics is limited to audio-visual gadgets like radio and television, but the truth is, today the growth of any industry like communication, control, instrumentation or computer, is dependent upon electronics to a great extent. And integrated circuits are electronics.

The integrated circuit or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon. Most of the components used in ICs are not similar to conventional components in appearance although they perform similar electrical functions. In this chapter, we describe the basic processes used in the fabrication of integrated circuits. Both bipolar and MOS fabrication are treated. These circuits naturally offer a number of distinct advantages over those made by interconnecting discrete components. These may be listed as follows:

1. Miniaturization and hence increased equipment density
2. Cost reduction due to batch processing
3. Increased system reliability due to elimination of soldered joints
4. Improved functional performance (as it is possible to fabricate even complex circuits for better characteristics)
5. Matched devices
6. Increased operating speeds (due to the absence of parasitic capacitance effect)
7. Reduction in power consumption.

## 1.2 CLASSIFICATION

Integrated circuits offer a wide range of applications and could be broadly classified as:

Digital ICs

Linear ICs

Based upon the above requirements, two distinctly different IC technology namely, Monolithic technology and Hybrid technology have been developed.

In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. The monolithic circuit is ideal for applications where identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds. This technology is more adaptable to small quantity custom circuits. Based upon the active devices used, ICs can be classified as bipolar (using BJT) and unipolar (using FET). Bipolar and unipolar ICs may further be classified depending upon the isolation technique or type of FET used as in Fig. 1.1.

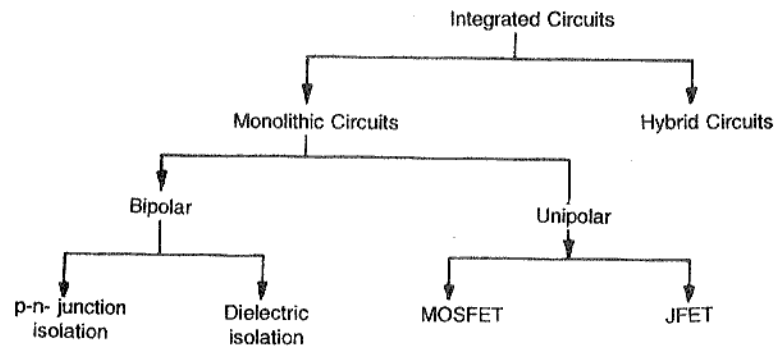


Fig. 1.1 Classification of ICs

## 1.3 IC CHIP SIZE AND CIRCUIT COMPLEXITY

UP until the 1950s, the electronic device technology was dominated by the vacuum tube. The present day electronics is the result of the invention of the transistor in 1947. The invention of the transistor by William B. Shockley, Walter H. Brattain and John Bardeen of Bell Telephone Laboratories was followed by the development of the Integrated circuit (IC). The concept of IC was introduced at the beginning of 1960 by both Texas Instruments and Fairchild Semiconductors. Since that time, the size and complexity of ICs have increased rapidly as shown by the brief chronology.

Invention of transistor (Ge)		1947
Development of Silicon transistor		1955-1959
Silicon Planar Technology	Junction transistor diode	1959
First ICs, Small Scale Integration (SSI)	3 to 30 gates/chip approx. or 100 transistors/chip (Logic gates, Flip-flops)	1960-65
Medium Scale Integration (MSI)	30 to 300 gates/chip or 100 to 1000 transistors/chip (Counters, Multiplexers, Adders)	1965-1970
Large Scale Integration (LSI)	300 to 3000 gates/chip or 1000-20,000 transistors/chip (8 bit microprocessors, ROM, RAM)	1970-1980
Very Large Scale Integration (VLSI)	More than 3000 gates/chip or 20,000-1,00,00,00 transistors/chip (16 and 32 bit microprocessors)	1980-1990
Ultra Large Scale Integration (ULSI)	$10^6 - 10^7$ transistors/chip (Special processors, Virtual reality machines, Smart sensors)	1990-2000
Giant-Scale Integration (GSI)	$> 10^7$ transistors/chip	

Over the years, the device density has increased together with some increase in the chip area. Figure 1.2 (a, b, c) show small (SSI), medium (MSI) and large (LSI or VLSI) IC chip size. The chip areas range from  $1 \text{ mm}^2$  (1600 mil<sup>2</sup>)\* for the SSI chip to  $1 \text{ cm}^2$  (160,000 mil<sup>2</sup>) for the LSI chip.

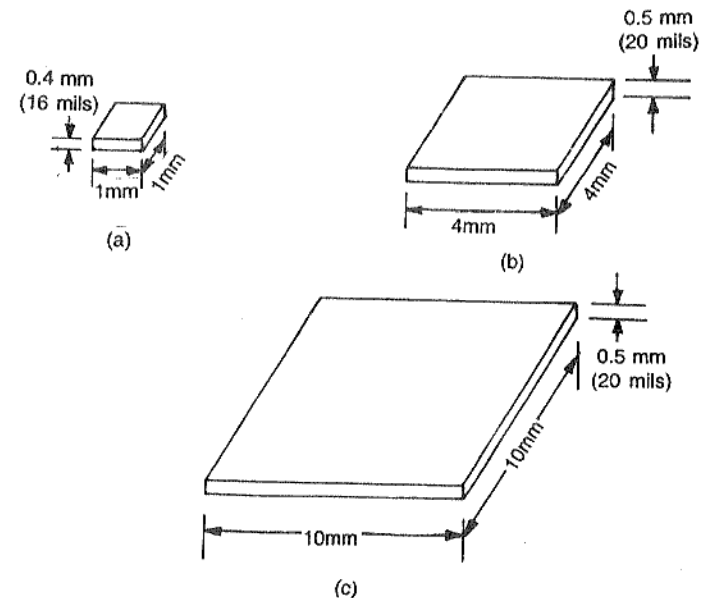


Fig. 1.2 Integrated circuit chips (a) SSI chip (b) MSI chip (c) LSI or VLSI chip

\* mil = 0.001 in = 25.4  $\mu\text{m}$  = 0.0254 mm

## 1.4 FUNDAMENTALS OF MONOLITHIC IC TECHNOLOGY

A monolithic circuit, literally speaking, means a circuit fabricated from a single stone or a single crystal. The origin of the word 'monolithic' is from the Greek word *monos* meaning 'single' and *lithos* meaning 'stone'. So monolithic integrated circuits are, in fact, made in a single piece of single crystal silicon.

The most significant advantage of integrated circuit of reducing the cost of production of electronic circuits due to batch production can be easily visualized by a simple example. A standard 10 cm diameter wafer can be divided into approximately 8000 rectangular chips of sides 1 mm. Each IC chip may contain as few as tens of components to several thousand components. And if 10 such wafers are processed in one batch, we can make 80,000 ICs simultaneously. Many chips so produced will be faulty due to imperfection in the manufacturing process. Even if the yield (percentage of fault free chips/wafer) is only 20 percent, it can be seen that 16,000 good chips are produced in a single batch.

The fabrication of discrete devices such as transistor, diode or an integrated circuit in general can be done by the same technology. The various processes usually take place through a single plane and therefore, the technology is referred to as planar technology. A simple circuit of Fig. 1.3 when fabricated by silicon planar technology will have the cross-sectional view shown in Fig. 1.4.

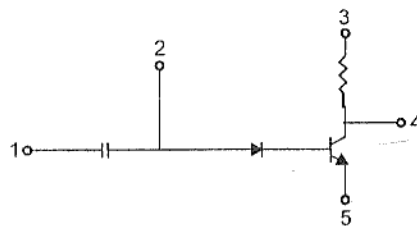


Fig. 1.3 A typical circuit

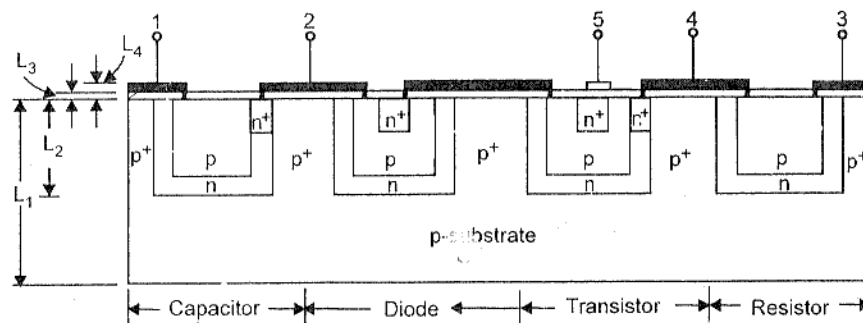


Fig. 1.4 Complete cross-sectional view of the circuit in Fig. 1.3 when transformed into monolithic form

An IC in general, consists of four distinct layers, as follows:

- Layer No. 1** (~ 400  $\mu\text{m}$ ) is a *p*-type silicon substrate upon which the integrated circuit is fabricated.
- Layer No. 2** (~ 5–25  $\mu\text{m}$ ) is a thin *n*-type material grown as a single crystal extension of the substrate using epitaxial deposition technique. All active and passive components are fabricated within this layer using selective diffusion of impurities.
- Layer No. 3** (0.02–2 $\mu\text{m}$ ) is a very thin  $\text{SiO}_2$  layer for preventing diffusion of impurities wherever not required using photolithographic technique.
- Layer No. 4** (~ 1 $\mu\text{m}$ ) is an aluminium-layer used for obtaining interconnection between components.

It may be pointed out that the drawings showing the cross-sectional view in this chapter are never scale drawings, but are distorted for the particular emphasis required.

## 1.5 BASIC PLANAR PROCESSES

The basic processes used to fabricate ICs using silicon planar technology can be categorised as follows:

1. Silicon wafer (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation technique
8. Metallization
9. Assembly processing and packaging

We shall now describe these processes in detail

### 1.5.1 Silicon Wafer Preparation

The following steps are used in the preparation of Si-wafers

1. Crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. Wafer polishing and etching
5. Wafer cleaning

The starting material for crystal growth is highly purified (99.99999) polycrystalline silicon. The Czochralski crystal growth process is the most often used for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant

is put in a quartz crucible and is then placed in a furnace. The material is then heated to a temperature in excess of the silicon melting point of  $1420^{\circ}\text{C}$ . A small single crystal rod of silicon called a seed crystal is then dipped into the silicon-melt and slowly pulled out as shown in Fig. 1.5. As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal. During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross-section. The diameter of the ingot is controlled by the pulling rate and the melt temperature. Ingot diameter of about 10 to 15 cm is common and ingot length is generally of the order of 100 cm.

Next the top and bottom portions of the ingot are cut off and the ingot surface is ground to produce an exact diameter ( $D = 10, 12.5, 15$  cm). The ingot is also ground flat slightly along the length to get a reference plane. The ingot is then sliced using a stainless

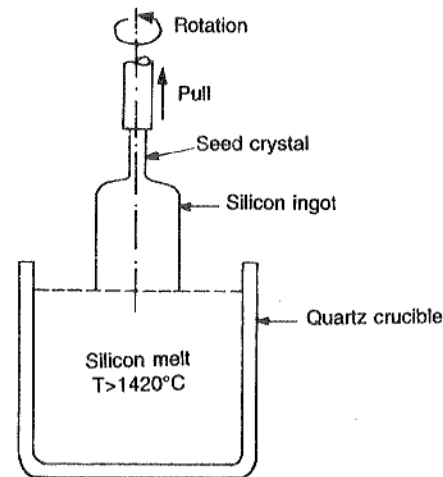


Fig. 1.5 Czochralski crystal growth

steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circular wafers or slices as shown in Fig. 1.6. The orientation flat portion serves as a useful reference plane for the various processes described later. The silicon wafers so obtained have very rough surface due to slicing operation. These wafers undergo a number of polishing steps to produce a flat surface. Then one side of the wafer is given a final mirror-smooth highly polished finish, whereas the other side is simply lapped on an abrasive lapping machine to obtain an acceptable degree of flatness. Finally, the wafers are thoroughly rinsed and dried. A raw cut slice of thickness 23–40 mils produces wafers of 16–32 mils thickness after all the polishing steps.

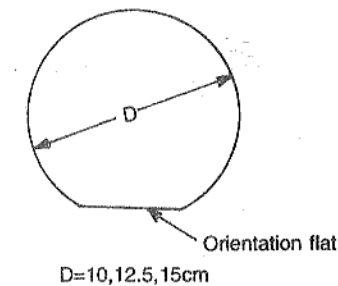


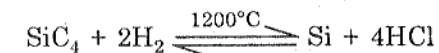
Fig. 1.6 Silicon wafer,  $D = 10, 12.5, 15$  cm showing flat orientation

These silicon wafers will contain several hundred rectangular chips, each one containing a complete integrated circuit. After all the IC fabrication processes are complete, these wafers are sawed into 100 to 8000 rectangular chips having side of 10 to 1 mm. Each chip is a single IC and may contain hundreds of components. The wafer thickness therefore is so chosen that it is possible to separate chips without breaking and at the same time, it gives sufficient mechanical strength to the IC chip.

### 1.5.2 Epitaxial Growth

The word epitaxy is derived from Greek word *epi* meaning 'upon' and the past tense of the word *teinon* meaning 'arranged'. So, one could describe epitaxy as, arranging atoms in single crystal fashion upon a single crystal substrate, so that the resulting layer is an extension of the substrate crystal structure.

The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.



Mostly, epitaxial films with specific impurity concentration are required. This is accomplished by introducing phosphine ( $\text{PH}_3$ ) for the *n*-type and bi-borane ( $\text{B}_2\text{H}_6$ ) for *p*-type doping into the silicon-tetrachloride hydrogen gas stream.

The process is carried out in a reaction chamber consisting of a long cylindrical quartz tube encircled by an RF induction coil. Figure 1.7 shows the diagrammatic representation of the system used. The silicon wafers are placed on a rectangular graphite rod called a boat. This boat is then placed in the reaction chamber where the graphite is heated inductively to a temperature  $1200^{\circ}\text{C}$ . The various gases required for the growth of desired epitaxial layers are introduced into the system through a control console.

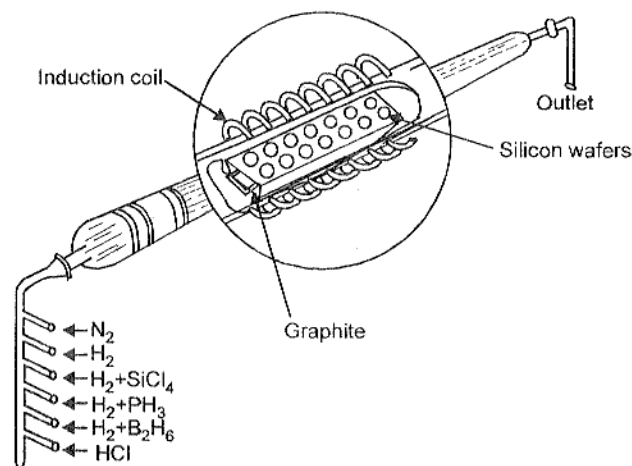


Fig. 1.7 A diagrammatic representation of a system for growing silicon epitaxial films

### 1.5.3 Oxidation

$\text{SiO}_2$  has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1.  $\text{SiO}_2$  is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid. Thus it stands against any contamination.
2. By selective etching of  $\text{SiO}_2$ , diffusion of impurities through carefully defined windows in the  $\text{SiO}_2$  can be accomplished to fabricate various components.

The silicon wafers are stacked up in a quartz boat and then inserted into quartz furnace tube. The Si-wafers are raised to a high temperature in the range of 950 to 1115°C and at the same time, exposed to a gas containing  $\text{O}_2$  or  $\text{H}_2\text{O}$  or both. The chemical reaction is



This oxidation process is called thermal oxidation because high temperature is used to grow the oxide layer. The thickness of the film is governed by time, temperature and the moisture content. The thickness of oxide layer is usually in the order of 0.02 to 2  $\mu\text{m}$ .

### 1.5.4 Photolithography

With the help of photolithography, it has become possible to produce microscopically small circuit and device patterns on Si-wafers. As many as 10,000 transistors can be fabricated on a 1 cm  $\times$  1 cm chip. The

conventional photolithographic process uses ultraviolet light exposure and device dimension or line width as small as 2  $\mu\text{m}$  can be obtained. However, with the advent of latest technology using X-ray or electron beam lithographic techniques, it has become possible to produce device dimension down to submicron range ( $< 1 \mu\text{m}$ ).

Photolithography involves two processes, namely:

- Making of a photographic mask
- Photo etching

The making of a photographic mask involves the following sequence of operations—first the preparation of initial artwork and secondly, its reduction. The initial layout or artwork of an IC is normally done at a scale several hundred times larger than the final dimensions of the finished monolithic circuit. This is because, for a tiny chip, larger the artwork, more accurate is the final mask. For example, it is often required to make an opening of width about 1 mil (25  $\mu\text{m}$ ). Obviously, this cannot be managed by any draftsman even with his thinnest of sketch pens. So the drawings are made magnified and often by a factor of 500. With this magnification, it is easy to see that a width of one mil is magnified to a width of 500 mils, that is, about 1.2 cm. Therefore, for a finished monolithic chip of area 50 mil  $\times$  50 mil, the artwork will be made on an area of about 60 cm  $\times$  60 cm.

This initial layout is then decomposed into several mask layers, each corresponding to a process step in the fabrication schedule, e.g., a mask for base diffusion, another for collector diffusion, another for metallization and so on.

For photographic purpose, artwork should not contain any line drawings but must be of alternate clear and opaque regions. This is accomplished by the use of clear Mylar coated with a sheet of red photographically opaque mylar (trade name-Rubylith). The red layer can be easily peeled off thus exposing clear areas with a knife edge from the regions where impurities have to be diffused. The artwork is usually produced on a precision drafting machine, known as coordinatograph. The coordinatograph has a cutting head that can be positioned accurately and moved along two perpendicular axes. The coordinatograph outlines the pattern cutting through the red mylar without damaging the clear layer underneath.

This rubylith pattern of individual mask is photographed and then reduced in steps by a factor of 5 or 10 several times to finally obtain the exact image size. The final image also must be repeated many times in a matrix array, so that many ICs will be produced in one process. The photo repeating is done with a step and repeat camera. This is an imaging device with a photographic plate on a movable platform. Between exposure, the plate is moved in equal steps so that successive images form in an array. When the exposed plate is developed, it becomes a master mask. The masks, actually used in IC processing are made by contact printing from the master. These working masks wear out with use and are replaced as required.

Photo-etching is used for the removal of  $\text{SiO}_2$  from desired regions so that the desired impurities can be diffused. The wafer is coated with a film of photosensitive emulsion (Kodak Photoresist KPR). The thickness of the film is in the range of 5000–10000 Å as shown in Fig. 1.8 (a). The mask negative of the desired pattern (as prepared by steps described earlier) is placed over the photoresist coated wafer as shown in Fig. 1.8 (b). This is now exposed to ultraviolet light, so that KPR becomes polymerized beneath the transparent regions of the mask. The mask is then removed and the wafer is developed using a chemical (trichloroethylene) which dissolves the unexposed/unpolymerized regions on the photoresist and leaves the pattern as shown in Fig. 1.8 (c). The polymerised photoresist is next fixed or cured, so that it becomes immune to certain chemicals called etchants used in subsequent processing steps. The chip is immersed in the etching solution of hydrofluoric acid, which removes the  $\text{SiO}_2$  from the areas which are not protected by KPR as shown in Fig. 1.8 (d) After diffusion of impurities, the photoresist is removed with a chemical solvent (hot  $\text{H}_2\text{SO}_4$ ) and mechanical abrasion.

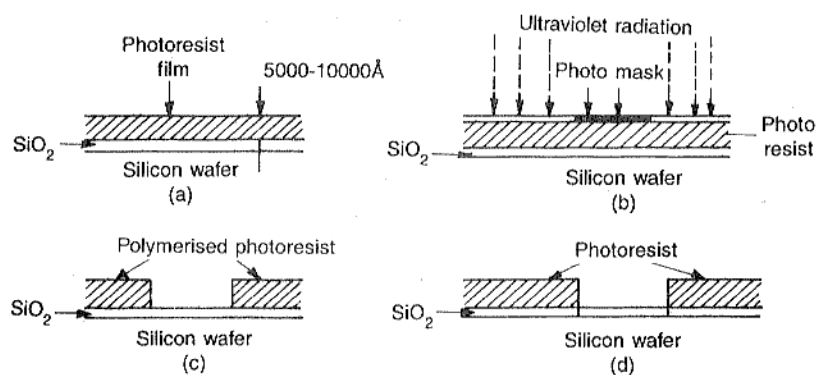


Fig. 1.8 Various steps for photo-etching

The etching process described is a wet etching process and the chemical reagents used are in liquid form. A new process used these days is a dry etching process called plasma etching. A major advantage of the dry etching process is that it is possible to achieve smaller line openings ( $\leq 1 \mu\text{m}$ ) compared to wet process. Complete description of the plasma etching process is beyond the scope of this book.

### X-Ray and Electron Beam Lithography

With conventional ultraviolet (UV) photolithography process in which the UV wavelengths used are in the range 0.3 to 0.4  $\mu\text{m}$ , the minimum device dimensions or line widths are limited by diffraction effects to around five wavelengths or about 2  $\mu\text{m}$ . This is what puts an upper limit on the IC device density using UV photolithography.

With the advent of X-ray and electron beam lithography techniques, it has become possible to produce device dimensions down to submicron range ( $< 1 \mu\text{m}$ ). This is due to much shorter wavelengths involved. With these techniques, MOSFET with gate length as small as 0.25  $\mu\text{m}$  have been made. The cost of X-ray or electron beam equipment is very high and the exposure times very much longer than with UV photolithography. So this becomes a very expensive process and is used only when very small device dimensions ( $\leq 1 \mu\text{m}$ ) are needed.

### 1.5.5 Diffusion

Another important process in the fabrication of monolithic ICs is the diffusion of impurities in the Silicon chip. This uses a high temperature furnace having a flat temperature profile over a useful length (about 20" length). A quartz boat containing about 20 cleaned wafers is pushed into the hot zone with temperature maintained at about a 1000°C. Impurities to be diffused are rarely used in their elemental forms. Normally, compounds such as  $\text{B}_2\text{O}_3$  (Boron oxide),  $\text{BCl}_3$  (Boron chloride) are used for Boron and  $\text{P}_2\text{O}_5$  (Phosphorous pentoxide) and  $\text{POCl}_3$  (Phosphorous oxychloride) are used as sources of Phosphorous. A carrier gas, such as dry oxygen or nitrogen is normally used for sweeping the impurity to the high temperature zone. The depth of diffusion depends upon the time of diffusion which normally extends to 2 hours.

The diffusion of impurities normally takes place both laterally as well as vertically. Therefore, the actual junction profiles will be curved as shown in Fig. 1.9. However, for the sake of simplicity, lateral diffusion will be omitted in all the drawings.

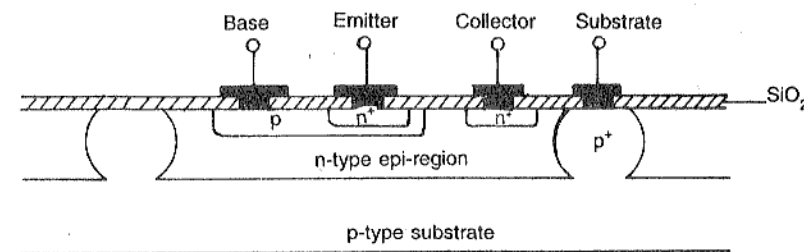


Fig. 1.9 The cross-section of an *npn* transistor showing curved junction profiles as a result of lateral diffusion

### 1.5.6 Ion Implantation

Ion implantation is the other technique used to introduce impurities into a silicon wafer. In this process, silicon wafers are placed in a vacuum chamber and are scanned by a beam of high-energy dopant ions (borons for *p*-type and phosphorus for *n*-type) as shown in Fig. 1.10. These ions are accelerated by energies between 20 kV to 250 kV.



As the ions strike the silicon wafers, they penetrate some small distance into the wafer. The depth of penetration of any particular type of ion increases with increasing accelerating voltage. Ion implantation technique has two important advantages.

1. It is performed at low temperatures. Therefore, previously diffused regions have a lesser tendency for lateral spreading.
2. In diffusion process, temperature has to be controlled over a large area inside the oven, whereas in ion implantation technique, accelerating potential and the beam current are electrically controlled from outside.

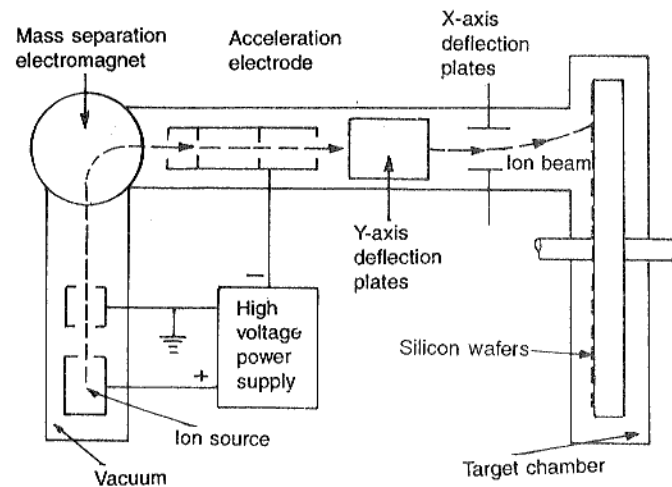


Fig. 1.10 Ion implantation system

### 1.5.7 Isolation Techniques

Since a number of components are fabricated on the same IC chip, it becomes necessary to provide electrical isolation between different components and interconnections. Various types of isolation techniques have been developed. However, we shall discuss here only two commonly used techniques namely:

- pn* junction isolation
- Dielectric isolation

#### *p-n* Junction Isolation

In this isolation technique,  $p^+$  type impurities are selectively diffused into the  $n$ -type epitaxial layer so as to reach  $p$ -type substrate as shown in Fig. 1.11 (a). This produces islands surrounded by  $p$ -type moats. It can be seen that these regions are separated by two back-to-back  $p-n$  junction diodes. If the  $p$ -type substrate material is held at the most negative potential in the circuit, the diodes will be reverse

biased providing electric isolation between these islands. The different components are fabricated in these isolation islands. The concentration of the acceptor atoms in the region between isolation islands is usually kept much higher ( $p^+$ ) than the  $p$ -type substrate. This prevents the depletion region of the reverse biased diode from penetrating more into  $p^+$  region and possibly connecting the isolation islands.

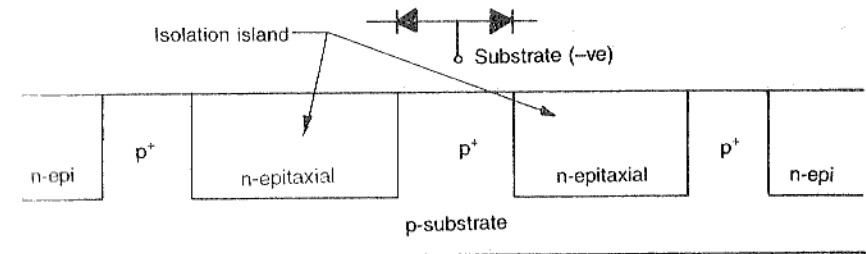


Fig. 1.11 (a) *p-n* junction isolation

There is, however, one undesirable by-product of this isolation process. It is the presence of a transition capacitance at the isolating  $pn$  junctions, resulting in an inevitable capacitor coupling between the components and the substrate. These parasitic capacitances limit the performance of the circuit at high frequencies. But being economical, this technique is commonly used for general purpose ICs.

#### Dielectric Isolation

Here a layer of solid dielectric such as silicon dioxide or ruby completely surrounds each component, thereby producing isolation, both electrical and physical. This isolating dielectric layer is thick enough so that its associated capacitance is negligible. Also, it is possible to fabricate both  $pnp$  and  $npn$  transistor within the same silicon substrate. Since this method requires additional fabrication steps, it becomes more expensive. The technique is mostly used for fabricating professional grade ICs required for specialised applications viz, aerospace and military, where higher cost is justified by superior performance. Figure 1.11 (b) shows such a structure.

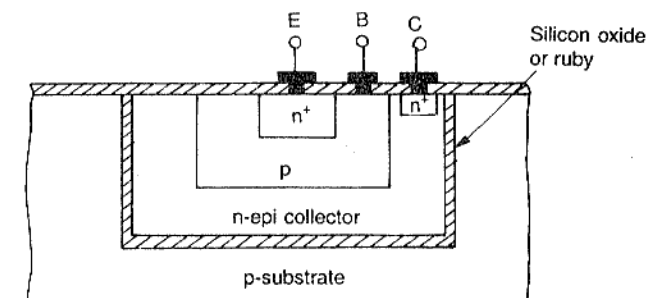


Fig. 1.11 (b) Dielectric isolation

### 1.5.8 Metallization

The purpose of this process is to produce a thin metal film layer that will serve to make interconnections of the various components on the chip. Aluminium is usually used for the metallization of most ICs as it offers several advantages.

1. It is relatively a good conductor.
2. It is easy to deposit aluminium films using vacuum deposition.
3. Aluminium makes good mechanical bonds with silicon.
4. Aluminium forms low resistance, non-rectifying (i.e. ohmic) contact with *p*-type silicon and the heavily doped *n*-type silicon.

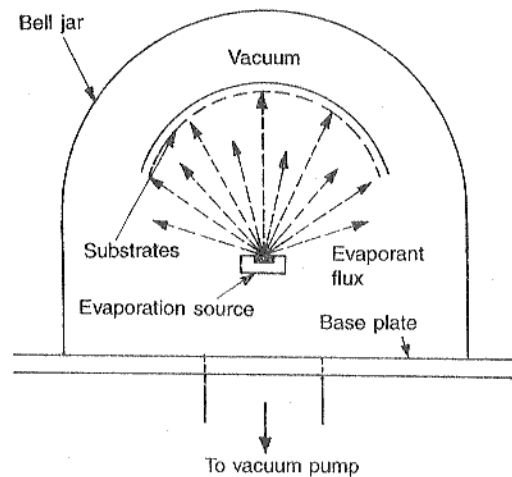


Fig. 1.12 Vacuum evaporation for metallization

The film thickness of about  $1\ \mu\text{m}$  and conduction width of about 2 to  $25\ \mu\text{m}$  are commonly used. The process takes place in a vacuum evaporation chamber as shown in Fig. 1.12. The pressure in the chamber is reduced to the range of about  $10^{-6}$  to  $10^{-7}$  torr (1 atmosphere = 760 torr = 760 mm Hg). The material to be evaporated is placed in a resistance heated tungsten coil or basket. A very high power density electron beam is focussed at the surface of the material to be evaporated. This heats up the material to very high temperature and it starts vaporizing. These vapors travel in straight line paths. The evaporated molecules hit the substrate and condense there to form a thin film coating.

After the thin film metallization is done, the film is patterned to produce the required interconnections and bonding pad configuration. This is done by photolithographic process and aluminium is etched away from unwanted places by using etchants like phosphoric acid ( $\text{H}_3\text{PO}_4$ ).

### 1.5.9 Assembly Processing and Packaging

Each of the wafer processed contains several hundred chips, each being a complete circuit. So these chips must be separated and individually packaged. A common method called scribing and cleaving used for separation makes use of a diamond tipped tool to cut lines into the surface of the wafer along the rectangular grid separating the individual chips. Then the wafer is fractured along the scribe lines and the individual chips are physically separated. Each chip is then mounted on a ceramic wafer and attached to a suitable package.

There are three different package configurations available.

1. TO-5 glass metal package
2. Ceramic flat package
3. Dual-in-line (ceramic or plastic type)

TO-5 packages are available in 8, 10 or 12 leads, whereas the flat or dual-in-line package is commonly available in 8, 14 or 16 leads, but

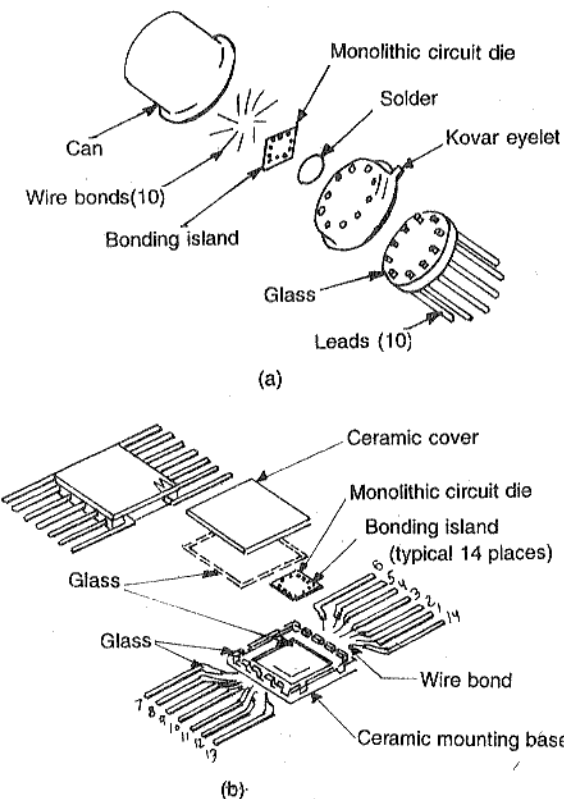


Fig. 1.13 Exploded view of (a) lead TO-5 package (b) 14-lead version of the flat package, showing the various components as well as the completed flat package

even 24 or 36 or 42 leads are also available for special circuits. Ceramic packages, whether of flat type or dual-in-line are costly due to fabrication process, but have the advantage of best hermetic sealing. Most of the general purpose ICs are dual-in-line plastic packages due to economy. Figure 1.13 (a, b) shows the exploded view of TO-5 and flat package.

### 1.6 FABRICATION OF A TYPICAL CIRCUIT

We shall here show the various steps utilized in converting the circuit of Fig. 1.3 into the monolithic IC of Fig. 1.4.

#### Step-1: Wafer Preparation

Refer Fig. 1.14 (a). The starting material called the substrate is a *p*-type silicon wafer prepared as discussed in Sec. 1.5.1. The wafers are usually of 10 cm diameter and 0.4 mm (~ 400  $\mu\text{m}$ ) thickness. The resistivity is approximately 10  $\Omega\text{-cm}$  corresponding to concentration of acceptor atom,  $N_A = 1.4 \times 10^{15}$  atoms/cm<sup>3</sup>.

#### Step-2: Epitaxial Growth

An *n*-type epitaxial film (5–25  $\mu\text{m}$ ) is grown on the *p*-type substrate as shown in Fig. 1.14 (b). The ultimately becomes the collector region of the transistor, or an element of the diode and diffused capacitor associated with the circuit. So in general it can be said that all active and passive components are fabricated within this layer. The resistivity of *n*-epitaxial layer is of the order of 0.1 to 0.5  $\Omega\text{-cm}$ .

#### Step 3: Oxidation

Refer Fig. 1.14 (c) A  $\text{SiO}_2$  layer of thickness of the order of 0.02 to 2  $\mu\text{m}$  is grown on the *n*-epitaxial layer.

#### Step 4: Isolation Diffusion

In the circuit of Fig. 1.3 four components have to be fabricated, so we require four islands which are isolated. For this,  $\text{SiO}_2$  is removed from five different places using photolithographic technique. Refer Fig. 1.14 (d). The wafer is next subjected to heavy *p*-type diffusion for a long time interval so that *p*-type impurities penetrate the *n*-type epitaxial layer and reach the *p*-type substrate. The area under the  $\text{SiO}_2$  are *n*-type islands that are completely surrounded by *p*-type moats. As long as the *pn* junctions between the isolation islands are held at reverse bias, that is, the *p*-type substrate is held at a negative potential with respect to the *n*-type isolation islands, these regions are electrically isolated from each other by two back-to-back diodes, providing the desired isolation.

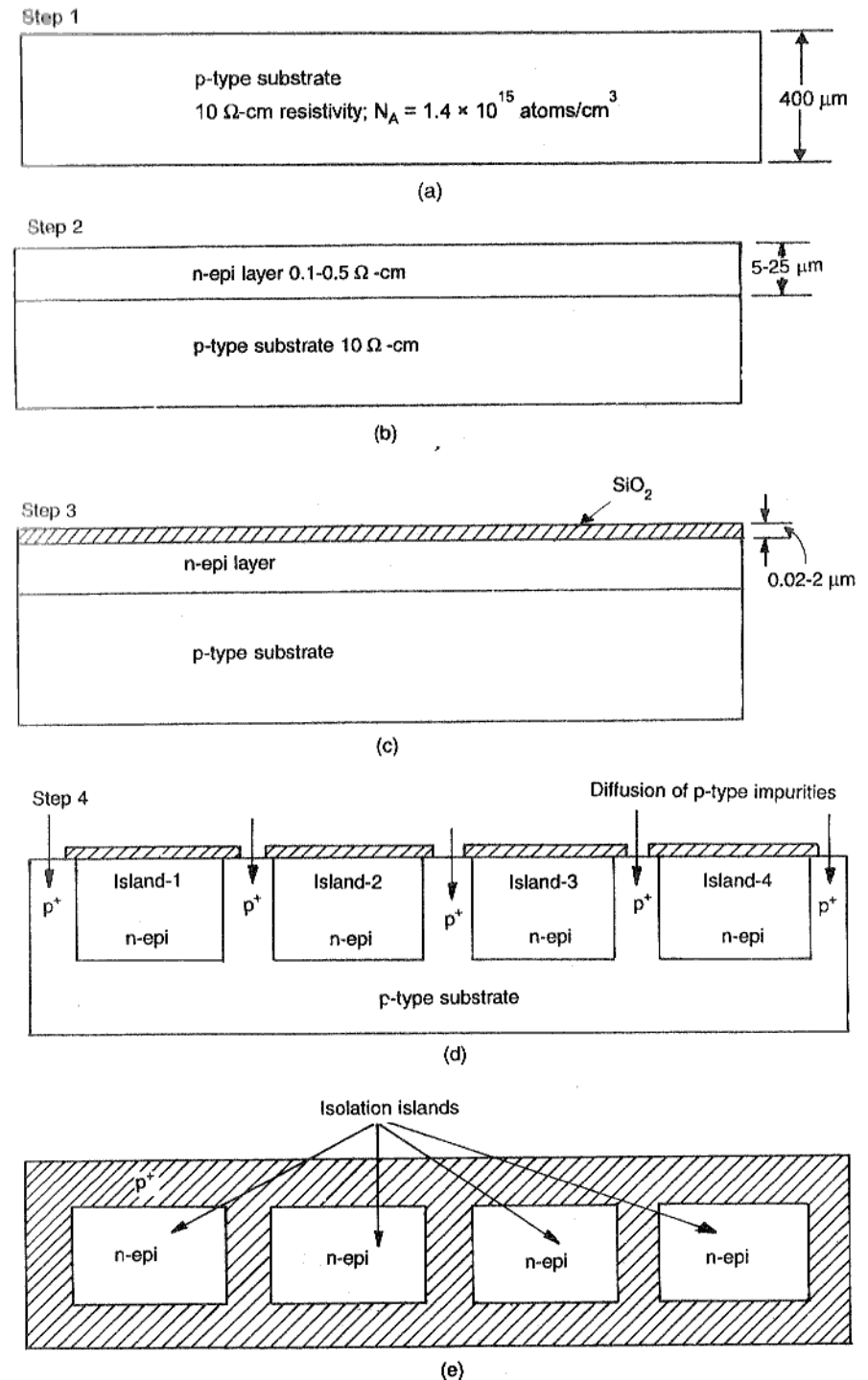


Fig. 1.14 (a-e) Steps in the fabrication of the circuit shown in Fig. 1.3

The concentration of acceptor atoms ( $N_A \approx 5 \times 10^{20} \text{ cm}^{-3}$ ) in the region between isolation islands is generally kept higher than  $p$ -type substrate for which  $N_A = 1.4 \times 10^{15} \text{ atoms/cm}^3$ . This ensures that the depletion region of the reverse biased diode will not extend into  $p^+$  region to the extent of electrically connecting the two isolation islands. There will, however, be a significant amount of barrier or transition capacitance present as a by product of the isolation diffusion. The top view of the isolation islands is depicted in Fig. 1.14 (e).

### Step 5: Base Diffusion

Refer to Fig. 1.14 (f). A new layer of  $\text{SiO}_2$  is grown over the entire wafer and a new pattern of openings is formed using photolithographic technique. Now,  $p$ -type impurities, such as boron, are diffused through the openings into the islands of  $n$ -type epitaxial silicon. The depth of this diffusion must be controlled so that it does not penetrate through  $n$ -layer into the substrate. This diffusion is utilized to form base region, of the transistor, resistor, the anode of the diode and junction capacitor.

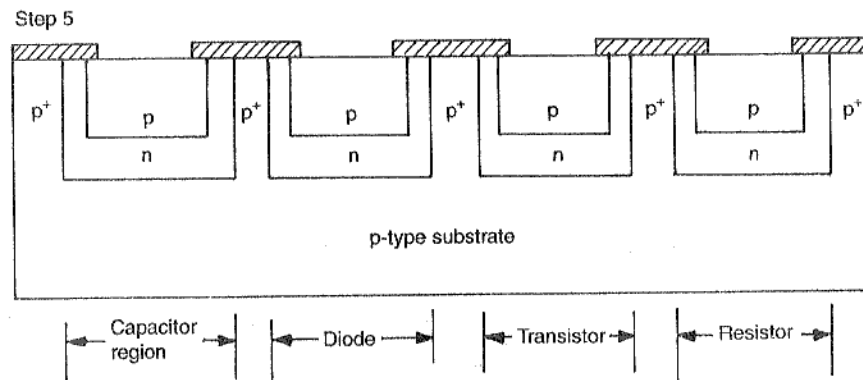


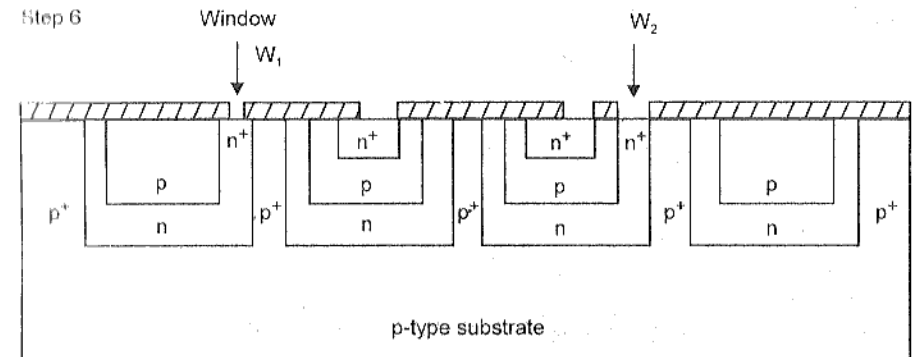
Fig. 1.14 (f)

### Step 6: Emitter Diffusion

Refer to Fig. 1.14 (g). A new layer of  $\text{SiO}_2$  is again grown over the entire wafer and selectively etched to open a new set of windows and  $n$ -type impurity (phosphorus) is diffused through them. This forms transistor emitter and cathode region of diode.

Windows ( $W_1$ ,  $W_2$  etc.) are also etched into  $n$ -region where contact is to be made to the  $n$ -type layer. Heavy concentration of phosphorus ( $n^+$ ) is diffused into these regions simultaneously with the emitter diffusion. The reason for using heavily doped  $n$ -regions can be explained as follows:

Aluminium, normally used for making interconnections, is a  $p$ -type impurity in silicon, and can produce an unwanted rectifying contact with the lightly doped  $n$ -material. However, heavy concentration of phosphorus ( $\sim 2 \times 10^{20} \text{ cm}^{-3}$ ) doping causes a high degree of damage to the Si-lattice at the surface, thus effectively making it semi-metallic. This  $n^+$  layer thus makes a good ohmic contact with the Al-layer. The top view corresponding to Fig. 1.14 (g) is shown in Fig. 1.14 (h).



(g)

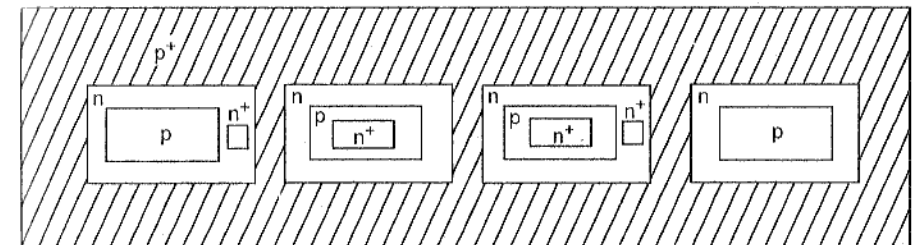


Fig. 1.14 (g-h)

### Step 7: Aluminium Metallization

Now the IC chip is complete with all the active and passive devices and only interconnections between the various components have to be made in accordance with the circuit in Fig. 1.3. The chip is further subjected to the process of the formation of a new  $\text{SiO}_2$  layer and masked etching to open a new set of windows at the points where contacts have to be made.

Now, a thin even coating of aluminium is vacuum-deposited over the entire surface of the wafer. The interconnection pattern between the components is then formed by photo resist techniques. The undesired aluminium areas are etched away leaving a pattern of interconnections between transistor, resistor, diode and capacitor as shown by the cross-sectional and top view in Fig. 1.14 (i) and Fig. 1.14 (j) respectively.

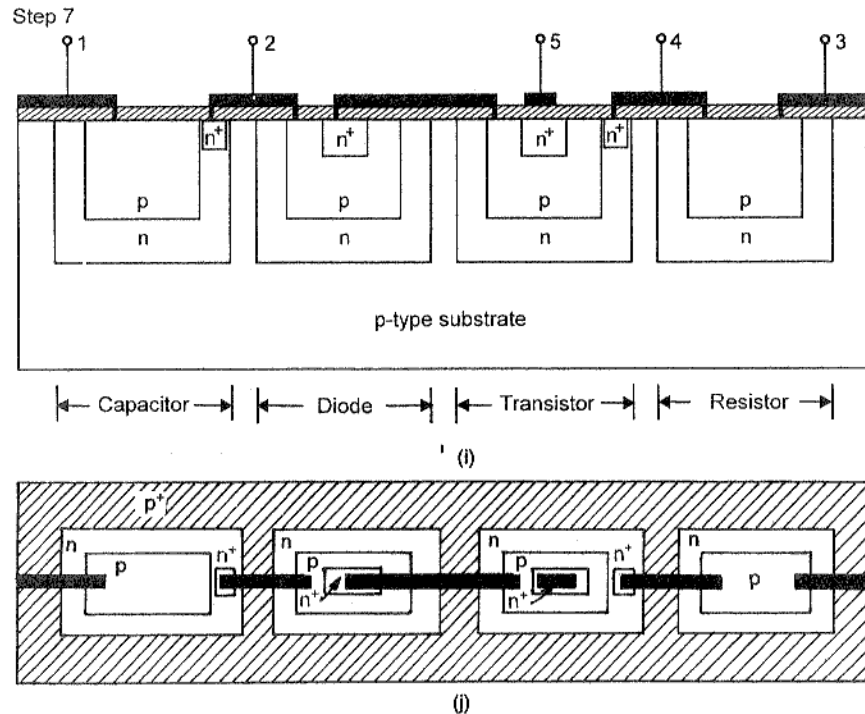


Fig. 1.14 (i, j)

## 1.7 ACTIVE AND PASSIVE COMPONENTS OF ICs

Now the reader is familiar with the basic technology involved in the fabrication of ICs. More light will be thrown on the various devices which constitute a monolithic circuit. These include:

1. Transistors
2. Diodes
3. Resistors
4. Capacitors
5. Inductors.

### 1.7.1 Monolithic Transistors

Figure 1.15 (a) shows the cross-sectional view of an IC transistor. Let us compare it with the conventional discrete transistor also fabricated using planar technology and shown in Fig. 1.15 (b).

The most striking feature in the two structures is that in the IC transistor, collector contact is on the top whereas in the discrete transistor it is at the bottom. In IC transistor, collector contact has to be taken from the top because collector is isolated from the substrate and the next isolation island by reverse-biased diodes. This structural

difference makes an integrated transistor poorer than discrete transistor in two ways:

- (i) Collector contact being at the top increases the collector current path, thereby increasing the collector series resistance and hence  $V_{CE(sat)}$  of the device.
- (ii) In the integrated transistor, additional parasitic capacitance appears between collector and substrate is held at negative potential. However, these shortcomings of the integrated transistors can be overlooked on account of a number of advantages inherent in integrated technology. In this, circuit performance is highly improved as matched transistors can be obtained for example to be used in difference amplifiers. Integrated transistors spaced within 30 mils can have  $V_{BE}$  matching better than 5 mV and  $h_{FE}$  match of  $\pm 10$  percent.

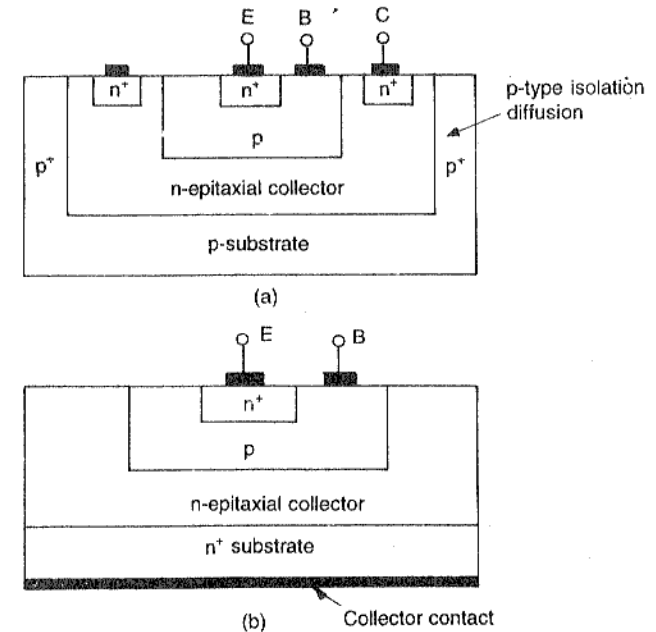


Fig. 1.15 Cross-section of (a) Monolithic integrated circuit transistor, (b) a discrete planar epitaxial transistor

### Use of 'Buried $n^+$ Layer' to reduce Collector Series Resistance

The higher collector series resistance of an integrated transistor can be easily reduced by a process known as 'buried layer' shown in Fig. 1.16. In this, a heavily doped  $n^+$  region is sandwiched between the  $n$ -type epitaxial collector and  $p$ -type substrate. This buried  $n^+$  region provides a low resistivity current path from the active collector region ( $n$ -type layer) to the collector contact ( $n^+$  contact layer). In effect, the  $n^+$  layer shunts the  $n$ -layer of the collector region with respect to the flow of the current thus effectively reducing the collector resistance.

### *pnp Transistor*

*pnp* transistors in integrated circuits are fabricated in one of the following three ways:

- Vertical or substrate *pnp*
- Lateral *pnp*
- Triple diffused *pnp*

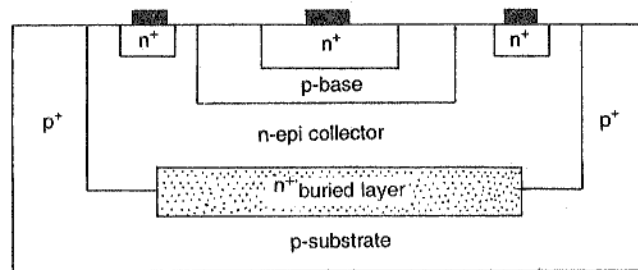


Fig. 1.16 Use of "buried  $n^+$  layer" to reduce collector series resistance

### *Vertical pnp Transistor*

The  $p$ -type substrate itself is used as  $p$ -collector,  $n$ -epitaxial layer for the base and the next  $p$ -diffusion (base in  $npn$  structure) as the emitter region. This type of *pnp* transistor has the limitation that collector has to be held at a fixed negative potential, as substrate is to be held at the most negative potential in the circuit for providing good isolation.

### *Lateral pnp-Transistor*

This is the most common form of an integrated *pnp* transistor which can be fabricated simultaneously with the *npn* transistor and requires no additional masking or diffusion step. The  $n$ -type epi layer is used as the base of the *pnp* transistor. During the  $p$ -type base diffusion for the *npn* transistor, two adjacent  $p$ -regions are diffused to form emitter and collector regions of the lateral *pnp* transistor as shown in Fig. 1.17.

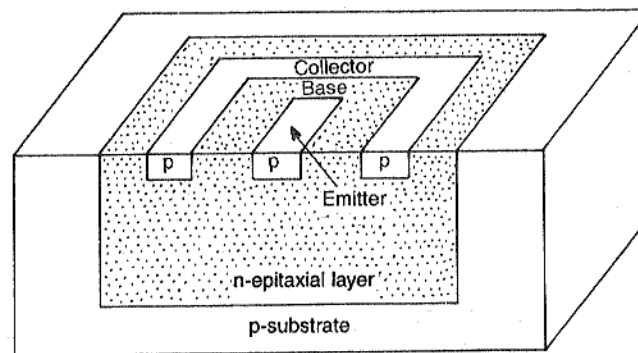


Fig. 1.17 A *pnp* lateral transistor

### *Triple Diffused pnp Transistor*

If to a standard *npn* transistor, an extra  $p$ -type diffusion is added after the  $n$ -diffusion, it is quite possible to obtain a *pnp* transistor and is known as triple diffused *pnp* transistor. However the usefulness of such a structure is limited due to additional fabrication steps required and serious design considerations.

### *Comparison of npn and pnp IC Transistors*

In general, *npn* transistors are preferred in integrated circuits compared to *pnp* transistors due to a variety of reasons.

1. A vertical *pnp* transistor has the disadvantage that its collector has to be held at a fixed negative voltage.
2. Lateral *pnp* transistor has inferior characteristic as the base width is usually larger controlled by lateral diffusion of  $p$ -type impurities and photographic limitations during mask making and alignment. Therefore, *pnp* transistor normally gives current gain as low as 1.5 to 30 compared to 50 to 300 for the *npn* transistor. With improved technology, however, it has now been possible to increase the gain to 100.
3. We know that collector region is heated during base and emitter diffusions, so the diffusion coefficient of the collector impurities should be as small as possible to avoid the movement of the collector junction. Since  $n$ -type impurities have smaller diffusion constant than  $p$ -type impurities, the  $n$ -type collector moves very little while  $p$ -type moves appreciably. This makes the *npn* transistor superior in performance with relatively easier process control.

### *Multi-emitter Transistor*

In many applications such as transistor-transistor logic (TTL), we need multiemitter transistor of the type shown in Fig. 1.18 (a). The cross-sectional view of such a transistor is shown in Fig. 1.18 (b) where  $n^+$  emitter is diffused at three places in the  $p$ -type base. Thus it is possible to save chip area and enhance component density of an IC.

### *The Schottky Transistor*

In digital circuits, many times it is desired that the switching should be very fast. This can be achieved if the transistor is prevented from entering into saturation. Figure 1.19 (a) shows such an arrangement where a Schottky diode (Sec. 1.7.2) is used as a clamp between the base and collector.

If base current is increased to saturate the transistor, the voltage at the collector drops thereby making diode D conduct. As soon as diode D conducts, the base to collector voltage drops to about 0.4 V

which is less than the cut-in voltage for Si-base to collector junction ( $\approx 0.5$  V), so that the transistor does not enter into saturation.

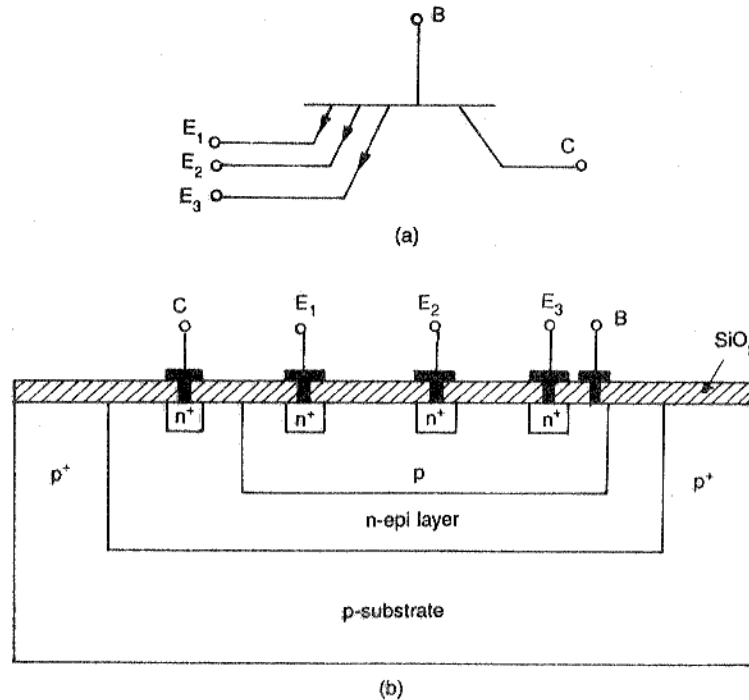


Fig. 1.18 (a) Multi-emitter transistor, (b) Cross-sectional view of a multi-emitter transistor

Figure 1.19 (b, c) shows the cross-sectional view of a Schottky transistor, and its symbol. A Schottky diode is formed between base and collector by allowing Al-metallization for the base lead to make contact with the n-type collector region. This is discussed in detail in Sec. 1.7.2.

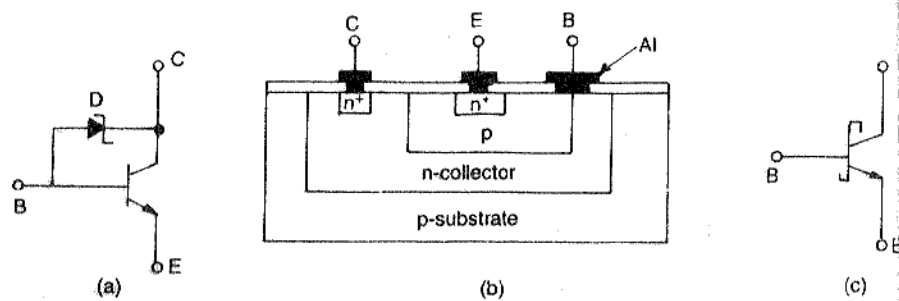


Fig. 1.19 (a) A transistor with a Schottky-barrier diode clamped between base and collector to prevent saturation, (b) Cross-section of a Schottky-barrier transistor, (c) Symbolic representation

### 1.7.2 Monolithic Diodes

Diodes find extensive use in integrated circuits, especially in digital applications. Figure 1.20 shows five different possible connections by which a transistor could be utilized as a diode. These configurations have slightly different characteristics as depicted in Table. 1.1 and the choice of the diode depends upon the application and circuit performance desired.

Table 1.1 Summary of typical values for various diode connections

Characteristic	(a) $V_{CB} = 0$	(b) $V_{CE} = 0$	(c) $V_{EB} = 0$	(d) $I_C = 0$	(e) $I_E = 0$
Breakdown voltage in volts	7	7	55	7	55
Storage time, n sec	9	100	53	56	85
Forward voltage in volts	.85	.92	.94	.96	.95

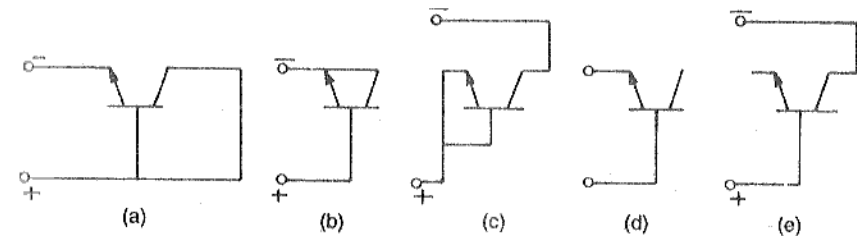


Fig. 1.20 Cross-section of various diode structures

It can be seen that diode 'a' is most useful for getting high speed diode to be used in digital integrated circuit due to its lowest storage time and lowest forward voltage drop. Diodes 'b' and 'd' can be utilized as a stored charge device as this feature gives a high speed turn-off of the transistor. Diode 'c' and 'e' have the advantage of highest breakdown voltage.

#### Schottky Barrier Diode

Metal to semiconductor junctions can be ohmic as well as rectifying. The ohmic contact is used when a lead is to be attached to a semiconductor device. And a rectifying contact called a metal semiconductor diode, (also called Schottky barrier diode) has characteristics very similar to an ordinary *pn* diode.

As already mentioned aluminium is a  $p$ -type impurity in silicon. So when it is used to make a contact with  $n$ -type Si, it is essential that contact is ohmic and no  $pn$  junction is formed. This is done by making  $n^+$  diffusions in the  $n$  regions near the surface where Al is deposited. On the other hand, if Al is deposited directly upon the  $n$ -type Si, a metal semiconductor diode is formed. It is found that such a metal semiconductor diode has essentially the same type of V-I characteristics as an ordinary  $pn$  junction, though the physical mechanism is very different and complicated.

Figure 1.21 (a) shows two contacts, where contact 1 is a Schottky barrier and contact 2 is an ohmic contact. The symbolic representation of a schottky diode is shown in Fig. 1.21 (b). The contact potential between the semiconductor and the metal creates a barrier to the flow of conduction electrons from semiconductor to metal. Forward biasing the junction lowers this barrier and permits electron flow from semiconductor to metal where electrons are abundant. Note that the majority carrier electrons carry current in a Schottky diode. On the other hand, in a  $pn$  junction diode, current is due to minority carriers and such a diode shows a substantial time delay from *on* to *off*, as the minority carriers stored in the junction have to be totally removed. In this sense, Schottky diode exhibit negligible storage time, since electrons from the  $n$ -type Si enter the Al almost right at the contact surface, where they mix with the free electrons and are not stored.

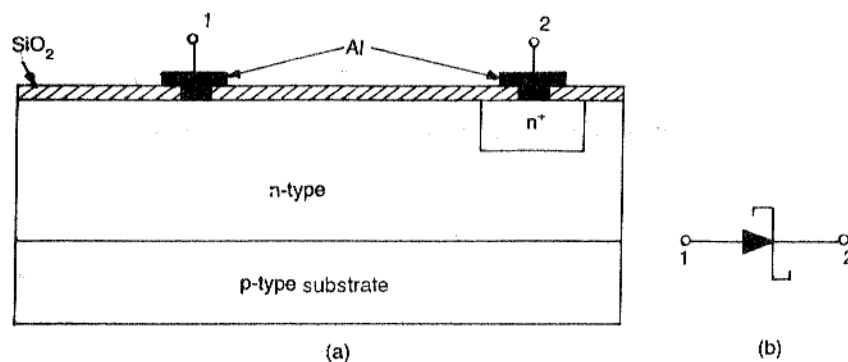


Fig. 1.21 (a) A Schottky diode, (b) Symbol for metal semiconductor diode

Another significant advantage of this type of diode is that it has less forward voltage ( $V_f \approx 0.3V$ ) when compared to that of  $pn$  diode ( $V_f = 0.6V$ ). Thus it can be used for more ideal clamping, or as detectors in high frequency and microwave ICs.

### 1.7.3 Integrated Resistors

The basic technique for obtaining a resistor in integrated circuit is by utilising the bulk resistance of a defined volume of semiconductor region. Four different methods are available for fabricating integrated resistors, namely:

- Diffused Resistor
- Epitaxial Resistor
- Pinched Resistor
- Thin Film Resistor

#### Diffused Resistor

In this method, resistor is formed in one of the isolated regions of epitaxial layer during base or emitter diffusion common to bipolar transistor fabrication. As no extra fabricating steps are required, this type of resistor is very economical. However, a severe limitation is the small range of resistances possible.

The value of the resistance depends upon the surface geometry. That is, length, width and upon the diffused impurity profile. In this context, a very useful quantity sheet resistance is defined as diffused layers are very thin.

#### Sheet Resistance $R_s$

Consider the square  $L \times L$  of a material of resistivity  $\rho$ , thickness  $t$ , and cross-sectional area  $A = L \times t$  shown in Fig. 1.22 (a). The resistance of this sheet of material can be written as

$$R_s = \frac{\rho L}{L \times t} = \frac{\rho}{t} \text{ (ohms per square)}$$

This quantity  $R_s$  is independent of the size of the square and mainly depends upon the diffusion characteristic of the material. Now consider Fig. 1.22 (b, c) which shows a base resistor and the emitter resistor. The resistance for these resistors can be expressed in terms of the sheet resistance  $R_s$  and the surface dimensions  $L$  and  $W$ .

$$\text{Now} \quad R = \rho \frac{L}{W \times t}$$

$$\text{or,} \quad R = R_s \frac{L}{W}$$

where the ratio  $L/W$  is called the aspect ratio of the surface geometry and is, therefore, the effective number of square contained in the resistor. The base resistor in the range of  $20 \Omega$  to  $300 \text{ k}\Omega$  can be easily fabricated due to medium resistivity ( $200 \Omega/\text{square}$ )  $p$ -type base region. However, the sheet resistance of the emitter diffusion is of the order of  $5 \Omega/\text{sq}$ . only. So emitter resistors are usually in the range of  $10$  to  $1 \text{ k}\Omega$ .



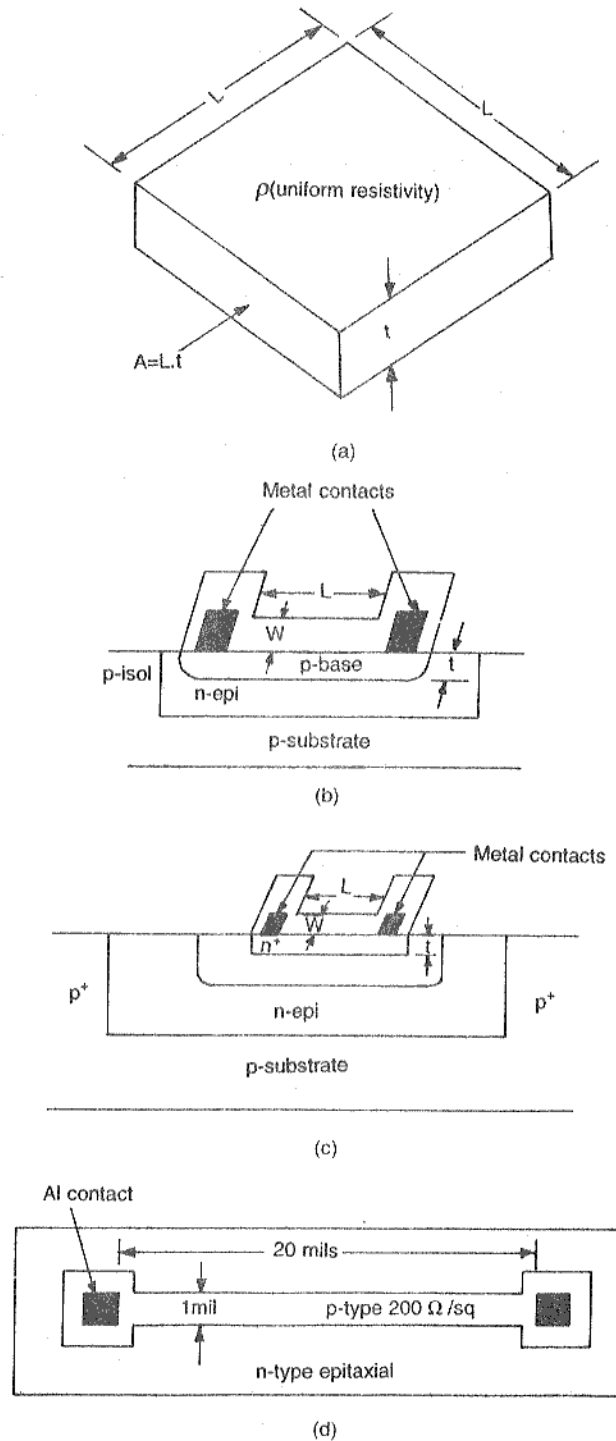


Fig. 1.22 (a) Sheet resistance (b) Base resistor (c) Emitter resistor (d) Top view showing dimensions for a 4000 Ω diffused resistor

**Example**

Design a 4 kΩ diffused resistor.

The sheet resistance of p-type diffusion is 200 ohm/sq.

$$\text{Then } \frac{L}{W} = \frac{R}{R_s} = \frac{4 \times 10^3}{200} = \frac{20}{1}$$

So a 4 kΩ resistor can be fabricated by using a pattern of 20 mils long by 1 mil wide as shown by the top view in Fig. 1.22 (d).

**Epitaxial Resistor**

Large value of resistance than possible by base or emitter resistor can be achieved by using n-epitaxial collector region as shown in Fig. 1.23 (a). Sheet resistance of epitaxial layer in the order of 1 to 10 kΩ/square can be obtained.

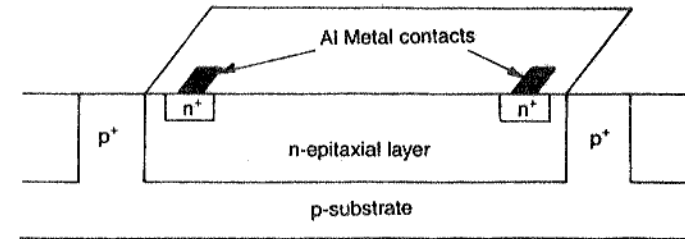


Fig. 1.23 (a) Epitaxial resistor

**Pinched Resistor**

The sheet resistivity of a semiconductor region can be increased by reducing its effective cross-sectional area. In a pinched resistor, this technique is used to achieve a high value of sheet resistance from the ordinary base diffused resistor.

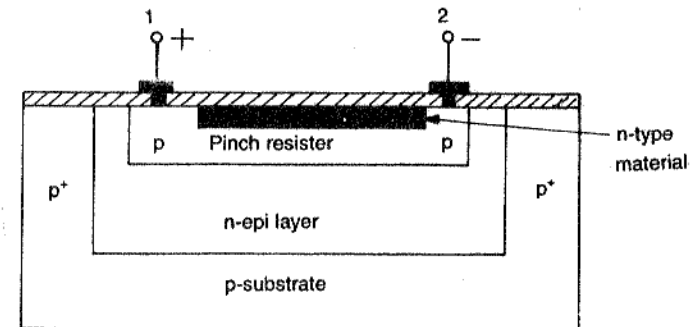


Fig. 1.23 (b) Cross-sectional view of a pinch resistor

A pinched base diffused resistor is shown in Fig. 1.23 (b). It can give resistances of the order of mega-ohm in a reasonably small area. In this structure, no current can flow through the  $n$ -type material (dark region) due to the diode at contact 2 in the reverse direction. Only a small reverse saturation current can flow through  $n$ -material. So, by creating this  $n$ -type region the effective cross-sectional area for the conduction path has been reduced and thus resistance between 1 and 2 increases.

#### Thin Film Resistor

Vapour thin film deposition techniques as discussed in Sec. 1.5.8 can also be used for the fabrication of IC resistors. In this, a very thin metallic film usually of Nichrome (NiCr) of thickness less than  $1\ \mu\text{m}$  is vapour deposited on the  $\text{SiO}_2$  layer. Using masked etching, desired geometry of this thin film is achieved to obtain suitable values of resistors. The ohmic contacts are made using Al metallization and usual masked etching techniques. Nichrome resistors are available with typical sheet resistance values of 40 to 400  $\Omega/\text{square}$  depending upon film thickness, so that resistance in the range of 20 to 50  $\text{k}\Omega$  can be easily obtained. Figure 1.23 (c) shows the cross-sectional view of such a resistor. These thin film resistors have three distinct advantages over the diffused resistors.

1. Thin film resistors have lesser and smaller parasitic components and hence their high frequency behaviour is better.
2. The values of thin-film resistors can be easily adjusted even after fabrication by cutting a part of the resistor with a laser beam (Laser trimming).
3. Thin film resistors have low temperature coefficient, thereby making them more stable.

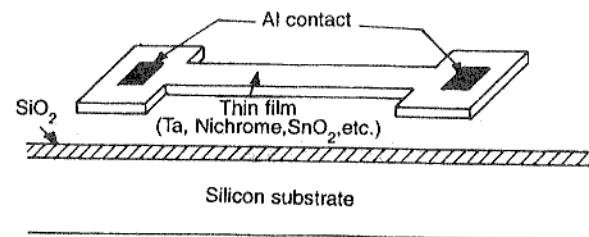


Fig. 1.23 (c) Cross-section of a thin film resistor

Higher values of thin film resistors have been obtained by depositing Tantalum over  $\text{SiO}_2$  layer. The main disadvantage of thin film resistors is the additional process steps required in their fabrication.

#### 1.7.4 Integrated Capacitors

Two commonly used methods for obtaining integrated capacitors are as follows:

- (1) Junction capacitor
- (2) MOS and thin film capacitor

##### Junction Capacitor

It is possible to use the junction capacitance of a reverse biased diode as an element in monolithic ICs. Figure 1.24 shows the cross-sectional view of a junction monolithic capacitor and its equivalent circuit. It can be seen that there are two junctions in this type of diffused capacitor. Junction  $J_2$ , if reverse biased, will produce the desired capacitance. However, a parasitic capacitance  $C_1$  is inevitable due to the junction  $J_1$  between  $n$ -type epitaxial layer and the substrate. Also a series resistance results due to the bulk resistance of the  $n$ -region. In the equivalent circuit, two diodes are the idealized diodes of the two junctions. The substrate must be held at the most negative point in the circuit, to minimize  $C_1$ . The value of the capacitance  $C_2$  will depend upon the area of the junction, impurity concentration of the  $n$ -type epitaxial layer and the voltage across the junction. It can be seen that the capacitor  $C_2$  is polarised and is obtained only when the junction  $J_2$  is reverse biased.

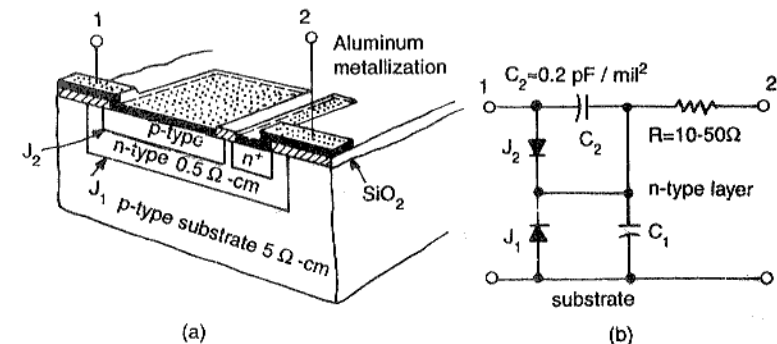


Fig. 1.24 (a) Junction-type IC capacitor, (b) Equivalent circuit

##### MOS and Thin Film Capacitor

A commonly used capacitor is the metal-oxide semiconductor capacitor for which the cross-sectional view and equivalent circuit is shown in Fig. 1.25. It is basically a parallel plate capacitor with  $\text{SiO}_2$  as the dielectric. The heavily doped  $n^+$  region formed during the emitter diffusion forms the lower plate and the thin film of aluminium metallization forms the upper plate of the capacitor with  $\text{SiO}_2$  as the

dielectric. As shown in the equivalent circuit, the parasitic effects consist of a small series resistance  $R$  due to  $n^+$  region, a collector substrate junction  $J_1$ , and its associated capacitance  $C_1$ .

This type of capacitor has the advantage of being nonpolar, that is, it does not matter which of the plates is positive or negative. Nor is it a function of the voltage applied, thus giving more circuit flexibility. Silicon Nitride ( $\text{Si}_3\text{N}_4$ ) can also be used as dielectric layer. Silicon Nitride offers a higher value of capacitance because of higher dielectric constant value, but requires extra processing steps.

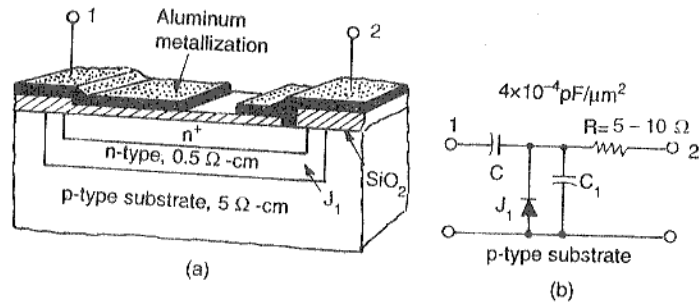


Fig. 1.25 (a) Structure and (b) equivalent circuit of a MOS capacitor

Thin film capacitor structures which use thin dielectric film layer between two metal layers are also in use. Although such a capacitor structure is almost free from substrate parasitics, it requires a number of additional masking and deposition steps beyond the basic MOS structure. In such a structure, either aluminium or tantalum is used as capacitor plates and aluminium oxide ( $\text{Al}_2\text{O}_3$ ) or tantalum oxide ( $\text{Ta}_2\text{O}_5$ ) as the dielectric material.  $\text{Ta}_2\text{O}_5$  is particularly preferred for large value capacitors. One basic serious disadvantage of thin film capacitor is that they fail when the voltage rating exceeds due to breakdown of the dielectric. This is a destructive and irreversible failure mechanism and may require over-voltage protection.

### 1.7.5 Integrated Inductors

Inductors, transformers and chokes are the missing link in the chain of IC components. IC devices are essentially two dimensional as the depth dimension is usually very small ( $\sim 1$  to  $10 \mu\text{m}$ ) compared to the lateral dimensions. IC inductors can be made in the form of a flat metallic thin film spirals by successive deposition of conduction patterns. Very small values of inductance of the order of nano-henry with low quality factor can be only obtained. For any reasonable inductance value, a three dimensional coil structure is needed to obtain a large number of turns.

Most circuit designers go to great lengths to avoid the use of inductors or otherwise simulate them by using RC active networks. In

applications such as RF and IF circuits, where inductors cannot be avoided, inductors external to the IC-package are used. However, in thin-film hybrid microwave integrated circuit (MIC), thin film inductor spirals are used giving upto 250 nH.

## 1.8 FABRICATION OF FET

Unipolar monolithic ICs use JFET or MOSFET as an active device. The fabrication technique of JFET, MOSFET and CMOS is discussed.

### 1.8.1 JFET Fabrication

The structure of an  $n$ -channel JFET is shown in Fig. 1.26. The basic processes used are the same as in BJT fabrication. The epitaxial layer which formed the collector of the BJT is used as the  $n$ -channel of the JFET. The  $p^+$  gate is formed in the  $n$ -channel by the process of diffusion or ion-implantation. The  $n^+$  regions have been formed under the drain and source contact regions to provide good ohmic contact.

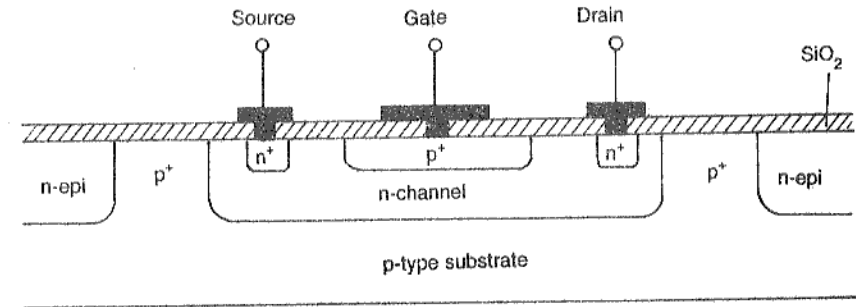


Fig. 1.26  $n$ -channel JFET structure

### 1.8.2 MOSFET Fabrication

Two types of MOSFET devices are available, such as, enhancement type and depletion type. The cross-sectional view of  $n$ -channel aluminium gate enhancement MOSFET is shown in Fig. 1.27. In this structure, the metallic gate G is separated from the semiconductor channel by the insulating  $\text{SiO}_2$  layer. The insulating layer of silicon dioxide gives an extremely high input resistance ( $10^{10}$  to  $10^{15} \Omega$ ) for the MOSFET.

The value of  $V_T$ , the threshold voltage for MOSFET fabricated by this technique is typically 3 to 6V and power supply voltage of 12V is used for the drain supply. This large voltage is not compatible with the 5V supply used in digital ICs. A number of techniques have been developed to lower the magnitude of  $V_T$  which leads to improved device performance.

### Use of Silicon Nitride ( $\text{Si}_3\text{N}_4$ )

It has been found that  $\text{Si}_3\text{N}_4$  has superior masking properties compared to  $\text{SiO}_2$ . The  $\text{Si}_3\text{N}_4$  is sandwiched between two  $\text{SiO}_2$  layers and provides the necessary barrier to prevent impurities penetrating through the  $\text{SiO}_2$  layer. The dielectric constant of  $\text{Si}_3\text{N}_4$  is 7.5 whereas that of  $\text{SiO}_2$  is 4. This increased overall dielectric constant reduces  $V_T$ .

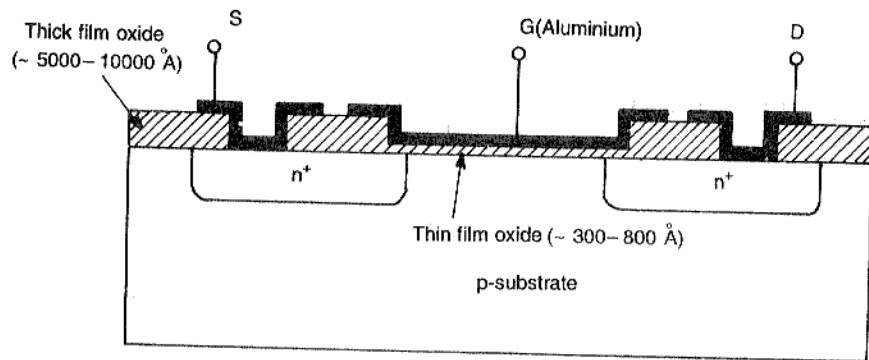


Fig. 1.27 n-channel MOSFET

### Polysilicon Gate

Polycrystalline silicon when doped with phosphorus is conductive and is used as the gate electrode instead of aluminium. This reduces  $V_T$  to about 1 to 2V. Such devices are called silicon gate MOS transistors. The fabrication of NMOS enhancement device using these improved techniques is shown in Fig. 1.28.

The  $\text{Si}_3\text{N}_4$  is first coated on the entire surface of a  $p$ -type wafer. With the help of a mask, sufficient area is defined to include the source, gate and drain. The  $\text{Si}_3\text{N}_4$  is next etched away from the surface outside the transistor region. Now  $p^+$  impurities are ion-implanted in the exposed  $p$ -substrate. These  $p^+$  regions serve to isolate the various devices. Next a thick  $\text{SiO}_2$  layer called field oxide is grown over the  $p^+$  regions. The  $\text{Si}_3\text{N}_4$  region, however, remains unaffected by the oxidation. The structure now is as shown in Fig. 1.28 (a).

The  $\text{Si}_3\text{N}_4$  is now removed by selective etching and then  $\text{SiO}_2$  layer (800 to 1000Å) is thermally grown over the transistor area as shown in Fig. 1.28 (b).

Polycrystalline silicon commonly known as polysilicon is now deposited over the entire wafer. The polysilicon gate is now formed by selective removal of polysilicon as shown in Fig. 1.28 (c).

The  $n^+$  source and drain regions are formed by ion implantation. The field oxide and the polysilicon gate prevent the penetration of dopants below these regions. The thin oxide layer, however, allows the penetration of dopants and thus drain and source regions are formed.

After this, the entire wafer is covered with a protective isolating layer usually of  $\text{SiO}_2$ . The contact areas (including the body) are next defined using photolithographic process. Finally aluminium is evaporated over the entire wafer and another mask is used to pattern the circuit connections. The final cross-section is shown in Fig. 1.28 (d).

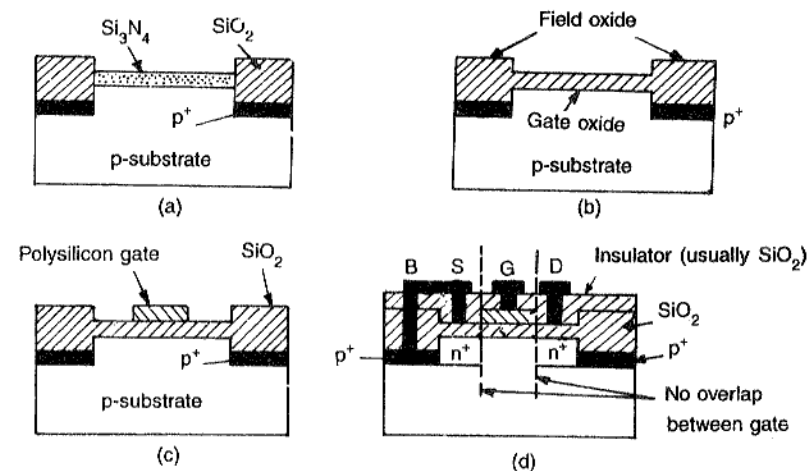


Fig. 1.28 Fabrication of polysilicon gate enhancement NMOS (a) Thick oxide growth and  $p^+$  implantation, (b) Selective etching of  $\text{Si}_3\text{N}_4$  and thin oxide growth, (c) Deposition of polysilicon gate, (d) Final cross-sectional view showing metallization and interconnection between substrate and source

There are two important points to be noticed in this structure.

1. The polysilicon-gate provides self alignment of the gate with the source and drain. In a conventional metal gate structure of Fig. 1.27, the gate electrode is normally designed to overlap the edges of the source and drain region by about  $5 \mu\text{m}$  to avoid any masking errors. This, however, results in small overlap capacitance  $C_{gs}$  between gate  $G$  and source  $S$  and  $C_{gd}$  between gate  $G$  and drain  $D$ . These capacitances are of the order of 1 to 3 pF and lower the speed of operation and increase the power consumption. The silicon gate due to self aligning property eliminates these capacitances.
2. Another advantage of this structure is that no isolation island is required. This is because drain terminal in an NMOS device is held positive with respect to the source which is tied to the substrate. This cuts off the drain to substrate diode and the source to substrate diode formed due to  $p^+$  region and the current flows only along the channel between  $D$  and  $S$ . In BJT the isolation diffusion occupies an extremely large percentage of chip area. With MOSFET, it is possible to get a packaging density twenty times more than that of BJT IC.

### 1.8.3 Complementary MOSFET (CMOS) Fabrication

It is possible to fabricate NMOS and PMOS enhancement devices on the same silicon chip. These devices are called complementary MOSFETs (abbreviated as CMOS, COS/MOS). The CMOS circuit of Fig. 1.29 (a) when implemented with polysilicon gate FETs has the cross-sectional view as shown in Fig. 1.29 (b). An  $n$ -type 'well' or 'tub' is diffused in the  $p$ -type substrate. The PMOS transistor ( $Q_2$ ) is fabricated within this well. The  $n$ -type region forms the substrate or body  $B_2$  for the the PMOS transistor. There are two additional steps required in the fabrication of PMOS transistor ( $Q_2$ ) compared to NMOS transistor ( $Q_1$ ), such as, the formation of  $n$ -region and ion implantation of  $p$ -type source and drain regions. The rest of the processes are the same as discussed for NMOS fabrication.

It can be seen that  $B_1$  is tied to  $S_1$  and is connected to the lowest voltage (GND) whereas  $B_2$  is tied to  $S_2$  and held at supply voltage  $V_{DD}$ . Since  $B_1$  is  $p$ -type and  $B_2$  is  $n$ -type, both the source substrate diodes ( $B_1$ - $S_1$  and  $B_2$ - $S_2$ ) are reverse biased and thus cut off. Thus isolation between NMOS and PMOS transistor is automatically achieved.

The circuit of Fig. 1.29 (a) is a CMOS inverter where  $G_1$  is tied to  $G_2$  and  $D_1$  is connected to  $D_2$ . However, we have not shown these connections in the cross-sectional view of Fig. 1.29 (b).

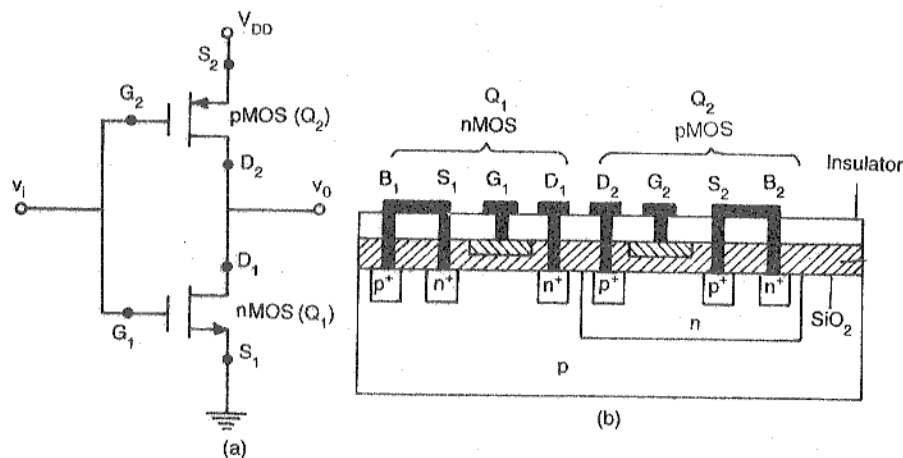


Fig. 1.29 (a) CMOS inverter, (b) Cross-section of CMOS IC

## 1.9 THIN AND THICK FILM TECHNOLOGY

Film ICs are classified as thick film and thin film circuits. Film technology at present can produce only passive components. The use of the term 'Thin Film' has been made in this chapter often, wherever

isolation or interconnections have to be made in integrated circuits. Thin film elements like resistors and capacitors have been discussed earlier also.

Conventional film circuits, both thick and thin, are made by depositing film capacitors and resistors on a passive substrate such as glass or ceramic and subsequently adding pre-fabricated active components to the film structure. Care has to be taken that the film elements and their interconnections are compatible with the rest of the integrated circuit.

Combining films and semiconductor technology, a circuit designer has greater degree of freedom, a wider range of component values and better electrical performance than either technology can provide separately.

Thin films are defined as the ones with thickness varying from 50 Å to 20,000 Å, whereas thick-films vary from 125000 Å (0.5 mil) to 625,000 Å (2.5 mils). However, a more fundamental difference between thin film and thick film is not the ultimate thickness, but the technology or the processes used for forming the film. Thick film ICs are made by the process of screen printing, usually silk screening techniques, whereas, the materials used to make thin film are generally deposited on to substrates in a vacuum chamber. Nevertheless, thick film technology produces cheap and rugged resistors, capacitors and conducting patterns. The processing equipment for thick film circuits is relatively inexpensive and easy to use. Thin film technology provides greater precision in manufacturing but is more costly than thick film technology.

### 1.9.1 Deposition of Thin Film

Various methods in use for deposition of thin film are:

1. Vacuum Evaporation
2. Sputtering
3. Gas plating
4. Electroplating
5. Electroless plating
6. Silk screening

The methods listed above have been used with varying degree of success. In this text however, we limit ourselves to discuss cathode sputtering and plating techniques only.

#### Vacuum Evaporation

The system used for depositing film using this method has been already discussed in sec. 1.5.8 where the technique has been used for depositing thin aluminium film for taking out contacts from the IC.

### Cathode Sputtering

The system used for cathode sputtering is almost identical to that used for vacuum evaporation. The process however is much slower than evaporation, depositing a micron-thick film in minutes to hours, compared to seconds to minutes for evaporation. However, sputtering is superior to vacuum evaporation in the quality of the film produced but sputtering equipment is more costly than most evaporation systems. The process of cathode sputtering is performed at a low pressure (about  $10^{-12}$  torr). The source material (material to be sputtered) is subjected to intense bombardment by the ions of a heavy inert gas such as argon. These gas ions are usually accelerated by making the source material as the cathode of a dc glow discharge. As atoms are ejected from the surface of the cathode, they diffuse away from it through a low pressure gas, depositing as a thin film on a nearby substrate. This sounds crude, but the high energy of the particles landing on the substrate actually results in a very uniform film with good crystal structure and adhesion. The principal parts of a sputtering system are shown in the Fig. 1.30. A potential typically 2 to 5 kV, is applied between the cathode (Source material) and anode, and produces a glow discharge that fills the entire interelectrode space, except for a thin region close to the cathode.

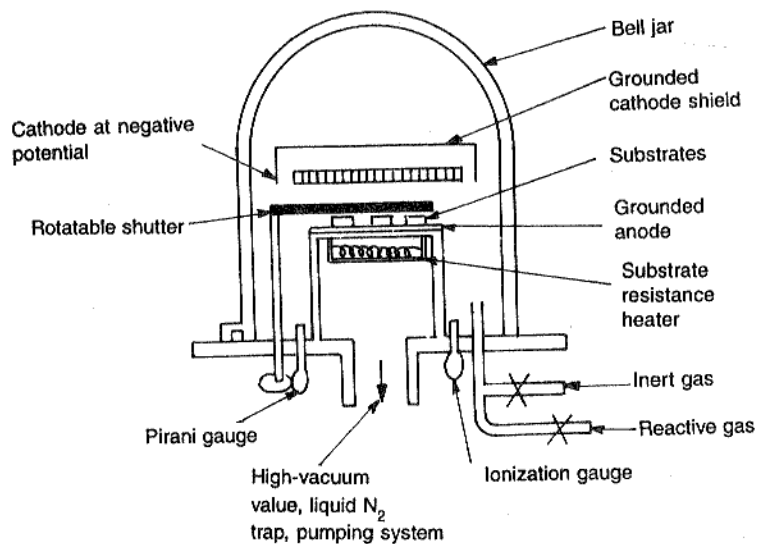


Fig. 1.30 The principal parts of sputtering system

### Plating Technique

The two types of plating technique used are (i) Electroplating (ii) Electroless plating.

Electroplating uses for typical process of coating an object with one or more layers of different metals. Cathode and anode, in this case substrate and metal, are immersed in an electrolytic solution. When dc is passed through the solution, the positive metal ions migrate from the anode and deposit on the cathode. This method is suitable for making conduction films of gold or copper.

In electroless deposition of thin films, a metal ion in solution is reduced to the free metal and deposited as a metallic coating without the use of an electric current. This process can be used to deposit metals on any substrate such as glass, ceramic, plastic, etc., and films to considerable thickness can be deposited.

### 1.9.2 Thick Film Technology

The basic thick film process are:

- (i) Screen printing,
- (ii) Ceramic firing.

The process of screen printing patterns is an ancient one. The Egyptians used this technique thousands of years ago to decorate pottery and the walls of buildings and tombs. The same process is used today for production of thick film circuits, though considerably more complicated than simply forcing the ink through the screen as did the equipment used by the Egyptians. The screens used are woven from stainless steel wires to mesh size 320 and mounted on aluminium frame so as to keep the screen under uniform tension. The screen is next coated with a photo-sensitive emulsion which polymerizes on exposure to light. A mask (negative) of the desired pattern is made and kept on it. After exposure to light, it is developed. The screen becomes clear wherever thick film is to be deposited and blocked by the photoresist elsewhere. The screen is now placed on a substrate and carefully aligned components are deposited on the substrate through screening process. The screening process is carried out by a squeegee driven across the patterned screen at a constant rate. The squeegee forces an ink in the paste form through the openings on the screen. Different types of inks are used for depositing resistors conductors.

The desired physical and electrical properties from the thick films so deposited are now developed by thermal processing usually referred to as firing. It uses a furnace or kiln where temperature varies from  $500^{\circ}\text{C}$  to  $1000^{\circ}\text{C}$  in four to eight separately controlled zones. During the firing process, the organic binders of the thick film paste vaporizes and the remaining material fuses with the substrate, thereby, becoming a part of the ceramic structure. However, the structure and dimensions of most thick films are not compatible with monolithic circuits, therefore their use is limited to hybrid structures only.

### 1.9.3 Surface Mount Technology (SMT)

SMT is one of the advanced achievement in the area of semiconductor technology. This technology improves the product in terms of function, size and quality. It is difficult to automate production line with the use of conventional components. However, with surface mount devices, automation of manufacturing process as well as interconnection methodology can be achieved. The compact size of microcassette recorder, calculators, wrist watches and radios is the result of clever electronic component packing and assembly as a surface mount technology.

Surface mount technology utilizes micro-miniature leaded or leadless components called SMDs which are directly soldered to the specified areas on the PCB/surface without holes. The compact size of SMD components greatly reduce the area in a PCB, thus increasing packaging density. In this technology, both the components as well as conductive paths are installed on the same side of PCB, whereas, in conventional mounting technology, the components are mounted on one side and conductive paths are on the other side of PCB.

### 1.10. TECHNOLOGY TRENDS

The technology of semiconductor is advancing at a rapid rate. For high speed and low noise applications, bipolar technology is used. The heat dissipation in bipolar circuits is large and requires elaborate cooling arrangement. The MOS technology is becoming popular, because, high component density can be achieved. Originally, PMOS devices were used but now NMOS technology is predominant due to high-speed performance. The CMOS technology is now leading NMOS because of extremely low power consumption. The feature size of CMOS is also decreasing rapidly. In 1990s, the minimum feature size for CMOS was 0.5 micron ( $\mu\text{m}$ ), which reduced to 0.12  $\mu\text{m}$  in the year 2002 and it is predicted that 0.07  $\mu\text{m}$  will be available for production by 2004.

The assembly of the chip is also improving drastically : 120 to 250-pin package are already available. It is predicted that 1000-pin package will be available. The electron-beam photolithographic techniques have been outdated and X-rays are in use exclusively. By 2003-04 new techniques EUV and Scalpel will also be used along with X-ray. The interconnections will also undergo change from aluminium to copper and optical interconnections may soon arrive.

The design styles and design tools are also undergoing rapid evolution. The design tools are sometimes referred to as computer-aided-design (CAD) tools and automatic testing is employed. The programs SPICE for circuit analysis and SUPREME for device

fabrication are the two widely used CAD tools. These tools are not used to design ICs but provide necessary information to evaluate a given design. No commercial IC is fabricated without such analysis.

### Summary

1. An IC is a miniature, low cost electronic circuit fabricated on a single crystal chip of silicon.
2. An IC offers increased reliability, improved performance, high speed and lower power consumption.
3. ICs may be Linear or Digital.
4. Important IC technologies used are Monolithic technology and Hybrid technology.
5. The basic processes used in the silicon planar technology are (i) Substrate preparation (ii) Epitaxial Growth (iii)  $\text{SiO}_2$  growth (iv) Photolithography (v) Diffusion (vi) Metallization
6. Order of magnitude for some important quantities:
  - (i) Substrate thickness  $\sim 400\text{--}800 \mu\text{m}$  (16-32 mils)
  - (ii) Epitaxial thickness  $\sim 5\text{--}20 \mu\text{m}$
  - (iii) Oxide thickness  $\sim 0.02\text{--}2 \mu\text{m}$
  - (iv) Al metallization  $\sim 1 \mu\text{m}$
  - (v) Base width (thickness)  $\sim 0.7 \mu\text{m}$
  - (vi) Diffusion time = about 2 hours
  - (vii) Diffusion temperature =  $1000^\circ\text{C}$
  - (viii) Surface area for transistor  $\approx 25$  mils
  - (ix) Wafer diameter = 10; 12.5; 15 cm
  - (x) Chip size : 1  $\text{mm}^2$  (SSI); 16  $\text{mm}^2$  (MSI); 1  $\text{cm}^2$  (LSI)
  - (xi) Concentration of acceptor atoms in the p-type substrate  $N_A = 1.4 \times 10^{15}$  atoms/ $\text{cm}^3$
  - (xii) Concentration of acceptor atoms in isolation islands  $N_A = 5 \times 10^{20}/\text{cm}$
  - (xiii) Sheet resistance for
    - (a) epitaxial collector region is 1 to 10 k  $\Omega/\text{sq}$ .
    - (b) p-type base region is 200  $\Omega/\text{sq}$ .
    - (c) n-type emitter region is 5  $\Omega/\text{sq}$ .
7. The various components in an IC are provided electrical isolation by fabricating each component in an isolation island. Isolation techniques used are *pn* junction isolation and dielectric isolation.
8. ICs are available in three packages:
  - (i) TO-5 glass metal package
  - (ii) ceramic flat package
  - (iii) Dual-in-line package

9. Buried layer is a heavily doped  $n^+$  layer sandwiched between the  $p$ -type substrate and  $n$ -type epitaxial collector to reduce the collector series resistance of the IC transistor.
10. Aluminium used for making interconnections is a  $p$ -type impurity in silicon. The formation of a rectifying  $pn$  junction is avoided by making  $n^+$  diffusions in the  $n$ -regions from where contact is to be made using aluminium. Such contacts are called ohmic.
11. The  $npn$  transistors are preferred over  $pnp$  transistors in ICs.
12. A Schottky barrier diode is clamped between base and collector of a transistor to avoid saturation.
13. It has not been possible to fabricate high-Q-inductors in monolithic ICs. Inductors have to be simulated by RC networks.
14. MOSFET occupies very small area and consumes less power. A polysilicon gate MOSFET has advantage over aluminium gate as (i) it lowers  $V_T$ , (ii) it reduces capacitances due to self-aligning property.
15. Thin and Thick film technology is used to make passive components like resistors and capacitors. Films with thickness greater than 0.5 mil are usually made by thick film technology.

### Review Questions

- 1.1. List the advantages of integrated circuit over discrete component circuit.
- 1.2. Classify ICs on the basis of application, device used and chip complexity.
- 1.3. Name the technology used for the fabrication of transistors or ICs.
- 1.4. List the basic processes used in the silicon planar technology.
- 1.5. Explain how silicon wafers are prepared.
- 1.6. Explain the word "Epitaxy".
- 1.7. Describe the Epitaxial growth process.
- 1.8. Explain the importance of  $\text{SiO}_2$  layer. How thick is this layer?
- 1.9. Explain briefly the photolithography process.
- 1.10. Describe the diffusion process.
- 1.11. What is ion implantation? Give its advantages.
- 1.12. Explain the need for making isolation islands.
- 1.13. Explain the various isolation techniques used in ICs.
- 1.14. To what voltage is the substrate connected and why?
- 1.15. Name the different types of IC packages.
- 1.16. Draw the cross-section of a discrete transistor and an IC transistor and hence compare their performance.
- 1.17. What is meant by parasitic capacitance?
- 1.18. Discuss the various ways for fabricating  $pnp$  transistor.

- 1.19. Compare the performance of  $pnp$  and  $nnp$  transistor.
- 1.20. Explain why "buried layer" is used.
- 1.21. Show the cross-sectional structure of a multi-emitter transistor.
- 1.22. What is a Schottky transistor? Draw the cross-sectional view and explain its operation.
- 1.23. Give the various ways for making diodes in ICs.
- 1.24. Explain the operation of a Schottky-barrier diode.
- 1.25. What is an ohmic contact?
- 1.26. Give the advantages of Schottky barrier diode over  $pn$  junction diode.
- 1.27. Discuss the various methods used for fabricating IC resistors and compare their performance.
- 1.28. Define sheet resistance  $R_s$ .
- 1.29. Sketch the cross-section of a junction capacitor and draw its equivalent circuit.
- 1.30. Sketch a MOS capacitor and explain the difference in junction capacitor and MOS capacitor.
- 1.31. What is a thin film capacitor?
- 1.32. Explain why inductors are difficult to fabricate in ICs.
- 1.33. Draw the cross-section of an  $n$ -channel MOSFET.
- 1.34. Discuss the various ways for reducing  $V_T$  of a MOSFET.
- 1.35. What is the effect of using a polysilicon gate?
- 1.36. Discuss the self-aligning property of a polysilicon gate MOSFET.
- 1.37. Sketch the cross-section of a CMOS transistor.
- 1.38. Discuss the difference between thin films and thick films.
- 1.39. List the various methods used for depositing thin films.
- 1.40. Discuss cathode sputtering.
- 1.41. Describe thick film technology.



## 2

# Operational Amplifier

## 2.1 INTRODUCTION

Linear integrated circuits are being used in a number of electronic applications such as in fields like audio and radio communication, medical electronics, instrumentation control, etc. An important linear IC is operational amplifier which will be discussed in this chapter.

The operational amplifier (commonly referred to as op-amp) is a multi-terminal device which internally is quite complex. Fortunately, for the ordinary user, it is not necessary to know about the op-amp's internal make-up. The manufacturers have done their job so well that op-amp's performance can be completely described by its terminal characteristics and those of external components that are connected to it. However, for the designer's interest, the electronics of op-amp is described where the various stages of op-amp are discussed. Then some of the FET op-amps are described. The dc and ac characteristics with compensating techniques and the various applications of op-amp are taken up later.

## 2.2 BASIC INFORMATION OF OP-AMP

### Circuit Symbol

The circuit schematic of an op-amp is a triangle as shown in Fig. 2.1. It has two input terminals and one output terminal. The terminal

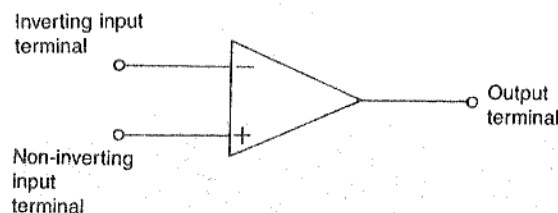


Fig. 2.1 Op-amp circuit symbol

with a (-) sign is called inverting input terminal and the terminal with (+) sign is called the non-inverting input terminal.

### Packages

There are three popular packages available:

1. The metal can (TO) package
2. The dual-in-line package (DIP)
3. The flat package or flat pack

Op-amp packages may contain single, two (dual) or four (quad) op-amps. Typical packages have 8 terminals (the can and the DIP or MINI DIP), 10 terminals (flatpacks and some cans) and 14 terminals (the DIP and the flat pack). The widely used very popular type, for example  $\mu A741$  is a single op-amp and is available as an 8-pin can, an 8-pin DIP, a 10-pin flatpack or a 14-pin DIP. The  $\mu A747$  is a dual 741 and comes in either a 10-pin can or a 14-pin DIP. Figure 2.2 shows the various IC packages along with the top view of connection diagram.

### OP-AMP Terminals

Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals. The significance of other terminals varies with the type of the op-amp.

Refer to the top view of a metal can package ( $\mu A741$ ) in Fig. 2.2 (a). The metal can has eight pins with pin number 8 identified by a tab. The other pins are numbered counter-clockwise from pin 8, beginning with pin 1. Pin 2 is called the inverting input terminal and pin 3 is the non-inverting input terminal, pin 6 is the output terminal and pins 7 and 4 are the power supply terminals labelled as  $V^+$  and  $V^-$  respectively. Terminals 1 and 5 are used for dc offset. The pin 8 marked NC indicates 'No Connection'. In case of DIP package of 741 as in Fig. 2.2 (b, c), the top pin on the left of the notch locates pin 1, and the flat pack of Fig. 2.2 (d) has a dot on it for identification. The other pins are numbered counter-clockwise from pin 1. The pin numbers have been illustrated only for some popular op-amps and the user should consult the manufacturer's data sheet before connecting a given op-amp into a circuit.

### Power Supply Connections

The  $V^+$  and  $V^-$  power supply terminals are connected to two dc voltage sources. The  $V^+$  pin is connected to the positive terminal of one source and the  $V^-$  pin is connected to the negative terminal of the other source as illustrated in Fig. 2.3 (a) where the two sources are 15 V batteries each. These are typical values, but in general, the power supply voltage may range from about  $\pm 5$  V to  $\pm 22$  V. The common

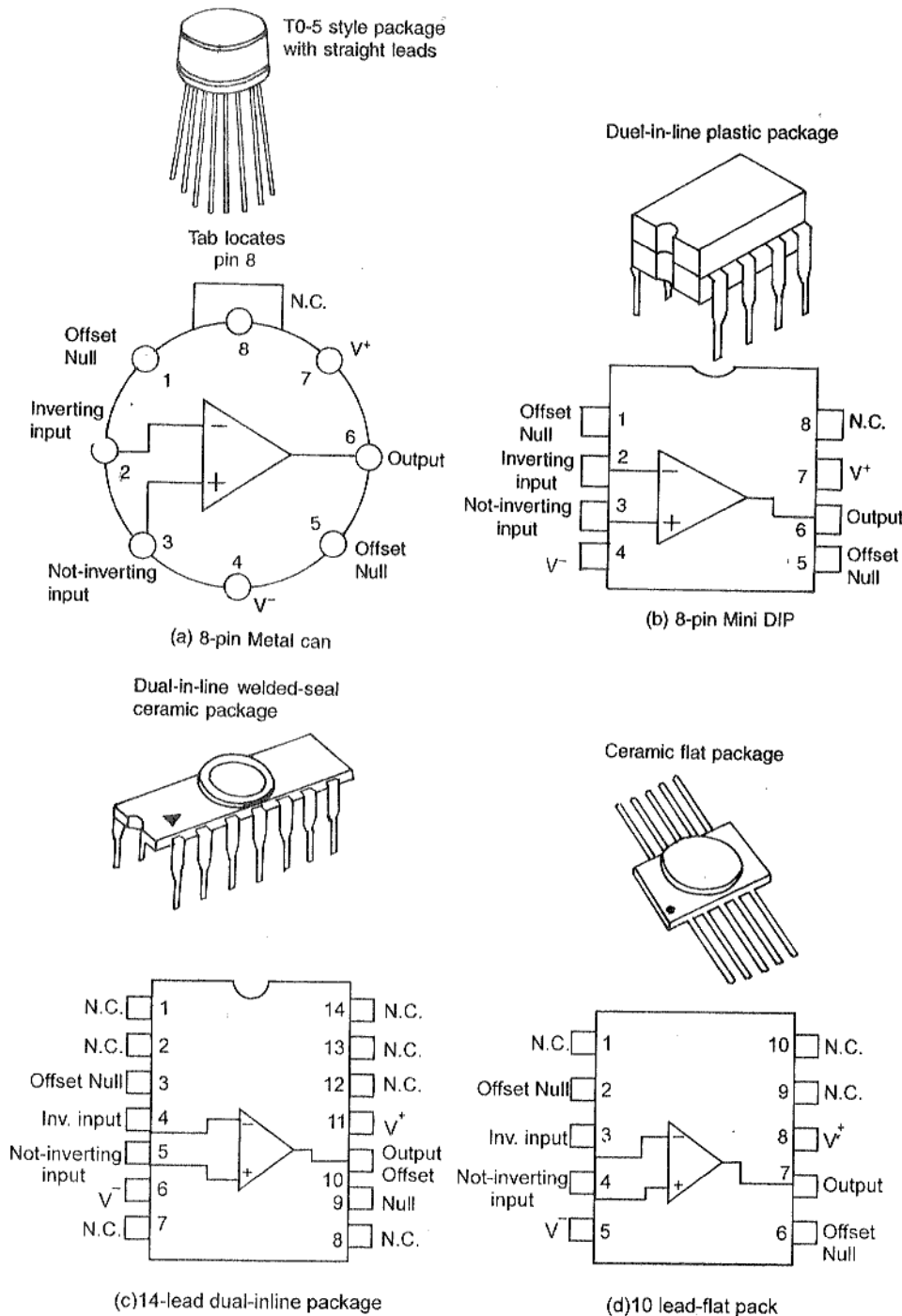


Fig. 2.2 (a, b, c, d) Various IC packages of  $\mu A741$  op-amp along with connection diagrams (top view)

terminal of the  $V^+$  and  $V^-$  sources is connected to a reference point or ground. Some op-amps have a ground terminal, but most do not. The ground is simply a convenient point on the circuit bread-board to which the op-amp is connected through the power supplies. The equivalent representation of Fig. 2.3 (a) is given in Fig. 2.3 (b). The common point of the two supplies must be grounded, otherwise twice the supply

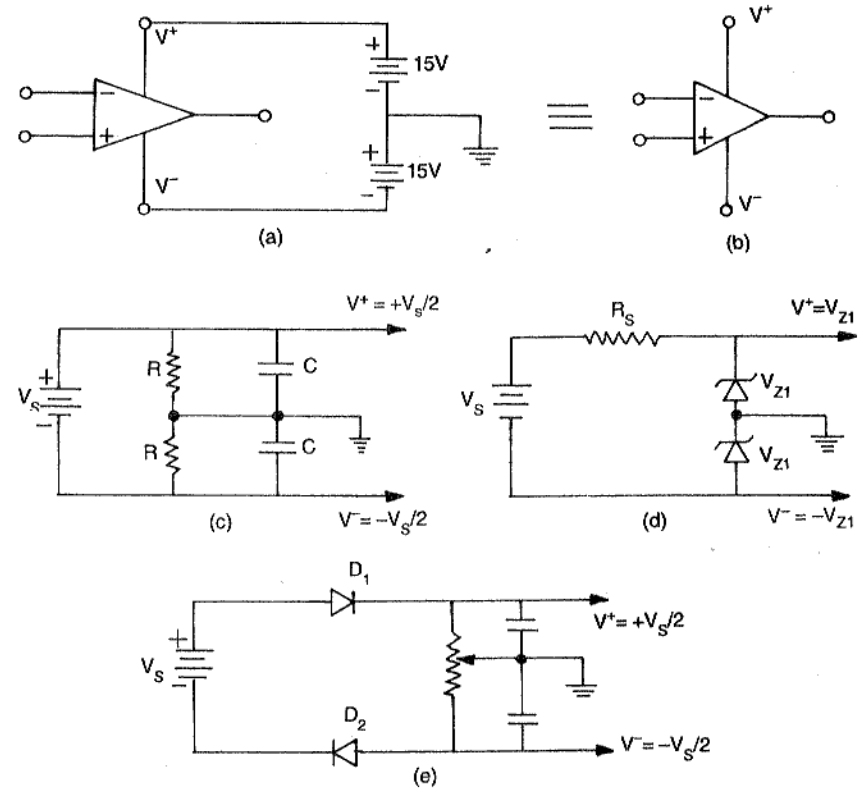


Fig. 2.3 (a) Power supply connections (b) Circuit symbol showing power supply terminals (c, d, e) Different circuits for obtaining positive and negative supply voltages for op-amp

voltage will get applied and it may damage the op-amp. Instead of using two power supplies, one can use a single power supply to obtain  $V^+$  and  $V^-$  as shown in circuits of Fig. 2.3 (c, d, e). In Fig. 2.3 (c), resistor  $R$  should be greater than 10 k $\Omega$  so that it does not draw more current from the supply  $V_s$ . The two capacitors provide decoupling of the power supply and range in value from 0.01 to 10  $\mu F$ . In the circuit of Fig. 2.3 (d), zener diodes are used to give symmetrical supply voltages. The value of the resistor  $R_s$  is chosen such that it supplies sufficient current for the zener diodes to operate in the avalanche mode. In Fig. 2.3 (e), potentiometer is used to get equal values of  $V^+$  and  $V^-$ . Diodes  $D_1$  and  $D_2$  protect the IC if the positive and negative

leads of the supply voltage  $V_s$  are accidentally reversed. These diodes can also be connected in the circuits of Fig. 2.3 (c) and 2.3 (d).

### Manufacturer's Designation for Linear ICs

Each manufacturer uses a specific code and assigns a specific type number to the ICs produced. For example, 741 an internally compensated op-amp originally manufactured by Fairchild is sold as  $\mu A741$ . Here  $\mu A$  represents the identifying initials used by Fairchild. The codes used by some of the well-known manufacturers of linear ICs are:

(1) Fairchild	$\mu A, \mu AF$
(2) National Semiconductor	LM, LH, LF, TBA
(3) Motorola	MC, MFC
(4) RCA	CA, CD
(5) Texas Instruments	SN
(6) Signetics	N/S, NE/SE
(7) Burr-Brown	BB

A number of manufacturers also produce popular ICs of the other manufacturers. For easy use, they usually retain the original type number of the IC alongwith their identifying initials. For example, Fairchild's original  $\mu A741$  is also manufactured by other manufacturers as follows:

(1) National Semiconductor	LM741
(3) Motorola	MC1741
(4) RCA	CA3741
(5) Texas Instruments	SN52741
(6) Signetics	N5741

It may be noted that the last three digits in each manufacturer's designation are 741. All these op-amps have the same specifications. Since a number of manufacturers produce the same IC, one can refer to such ICs by their type number only and delete manufacturer's identifying initials. For example,  $\mu A741$  or MC1741 may simple be referred as 741.

Some linear ICs are available in different classes such as A, C, E, S and SC. For example 741, 741 A, 741 C, 741 E, 741 S and 741 SC are different versions of the same op-amp. The main difference of these op-amps are:

741	Military grade op-amp (Operating temperature range $-55^\circ$ to $125^\circ C$ )
741C	Commercial grade op-amp (Operating temperate range $0^\circ$ to $70^\circ/75^\circ C$ )

741A	Improved version of 741	} Better electrical specifications
741E	Improved version of 741 C	
741S	Military grade op-amp with higher slew-rate	
741SC	Commercial grade op-amp with higher slew-rate	

### 2.3 THE IDEAL OPERATIONAL AMPLIFIER

The schematic symbol of an op-amp is shown in Fig. 2.4 (a). It has two input terminals and one output terminal. Other terminals have not been shown for simplicity. The  $-$  and  $+$  symbols at the input refer to inverting and non-inverting input terminals respectively, i.e if  $v_1 = 0$ , output  $v_o$  is  $180^\circ$  out of phase with input signal  $v_2$ . And, when  $v_2 = 0$ , output  $v_o$  will be in phase with the input signal applied at  $v_1$ . This op-amp is said to be ideal if it has the following characteristics.

Open loop voltage gain,	$A_{OL}$	=	$\infty$
Input impedance,	$R_i$	=	$\infty$
Output impedance	$R_o$	=	0
Bandwidth	$BW$	=	$\infty$
Zero offset, i.e. $v_o = 0$ when $v_1 = v_2 = 0$ .			

It can be seen that

- (i) an ideal op-amp draws no current at both the input terminals i.e.,  $i_1 = i_2 = 0$ . Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.
- (ii) Since gain is  $\infty$ , the voltage between the inverting and non-inverting terminals, i.e., differential input voltage  $v_d = (v_1 - v_2)$  is essentially zero for finite output voltage  $v_o$ .
- (iii) The output voltage  $v_o$  is independent of the current drawn from the output as  $R_o = 0$ . The output thus can drive an infinite number of other devices.

The above properties can never be realized in practice. However, the use of such an 'Ideal op-amp' model simplifies the mathematics involved in op-amp circuits. There are practical op-amps that can be made to approximate some of these characteristics.

A physical amplifier is not an ideal one. So, the equivalent circuit of an op-amp may be shown in Fig. 2.4 (b) where  $A_{OL} \neq \infty$ ,  $R_i \neq \infty$  and  $R_o \neq 0$ . It can be seen that op-amp is a voltage controlled voltage source and  $A_{OL} v_d$  is an equivalent *Thevenin* voltage source and  $R_o$  is the *Thevenin* equivalent resistance looking back into the output terminal of an op-amp. The equivalent circuit is useful in analyzing the basic operating principles of op-amp. For the circuit shown in Fig. 2.4 (b), the output voltage is

$$\begin{aligned} v_o &= A_{OL} v_d \\ &= A_{OL} (v_1 - v_2) \end{aligned} \quad (2.1)$$

The equation shows that the op-amp amplifies the difference between the two input voltages.

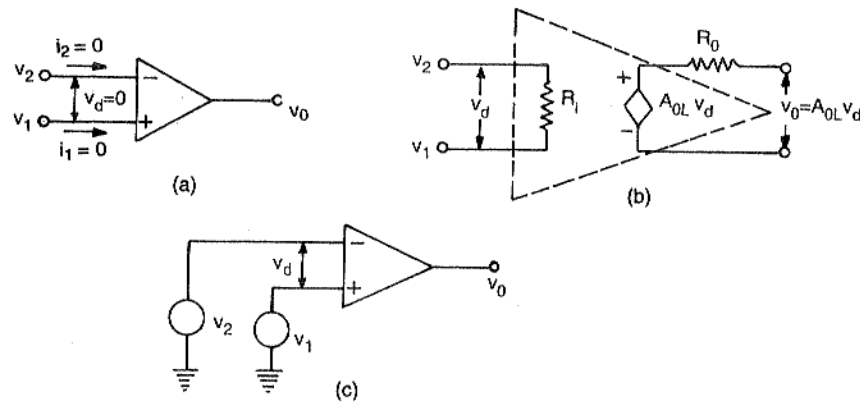


Fig. 2.4 (a) Ideal op-amp (b) Equivalent circuit of an op-amp (c) Open loop circuit

### 2.3.1 Open Loop Operation of Op-Amp

The simplest way to use an op-amp is in the open loop mode. Refer to Fig. 2.4 (c) where signals  $v_1$  and  $v_2$  are applied at non-inverting and inverting input terminals respectively. Since the gain is infinite, the output voltage  $v_o$  is either at its positive saturation voltage ( $+V_{sat}$ ) or negative saturation voltage ( $-V_{sat}$ ) as  $v_1 > v_2$  or  $v_2 > v_1$  respectively. The output assumes one of the two possible output states, that is,  $+V_{sat}$  or  $-V_{sat}$  and the amplifier acts as a switch only. This has a limited number of applications such as voltage comparator, zero crossing detector etc. which are discussed later.

### 2.3.2 Feedback in Ideal Op-Amp

The utility of an op-amp can be greatly increased by providing negative feedback. The output in this case is not driven into saturation and the circuit behaves in a linear manner.

#### Two Important Negative Feedback Circuits

There are two basic feedback connections used. In order to understand the operation of these circuits, we make two realistic simplifying assumptions discussed earlier also.

1. The current drawn by either of the input terminals (non-inverting and inverting) is negligible.
2. The differential input voltage  $v_d$  between non-inverting and inverting input terminals is essentially zero.

### 2.3.3 The Inverting Amplifier

This is perhaps the most widely used of all the op-amp circuits. The circuit is shown in Fig. 2.5 (a). The output voltage  $v_o$  is fed back to the inverting input terminal through the  $R_f - R_1$  network where  $R_f$  is the feedback resistor. Input signal  $v_i$  is applied to the inverting input terminal through  $R_1$  and non-inverting input terminal of op-amp is grounded.

**Analysis:** For simplicity, assume an ideal op-amp. As  $v_d = 0$ , node 'a' is at ground potential and the current  $i_1$  through  $R_1$  is

$$i_1 = \frac{v_i}{R_1} \quad (2.2)$$

Also since op-amp draws no current, all the current flowing through  $R_1$  must flow through  $R_f$ . The output voltage,

$$v_o = -i_1 R_f = -v_i \frac{R_f}{R_1} \quad (2.3)$$

Hence, the gain of the inverting amplifier (also referred as closed loop gain) is,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1} \quad (2.4)$$

Alternatively, the nodal equation at the node 'a' in Fig. 2.5 (a) is

$$\frac{v_a - v_i}{R_1} + \frac{v_a - v_o}{R_f} = 0$$

where  $v_a$  is the voltage at node 'a'. Since node 'a' is at virtual ground  $v_a = 0$ . Therefore, we get,

$$A_{CL} = \frac{v_o}{v_i} = -\frac{R_f}{R_1}$$

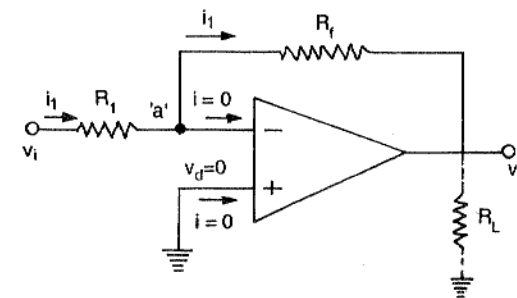


Fig. 2.5 (a) Inverting amplifier

The negative sign indicates a phase shift of  $180^\circ$  between  $v_i$  and  $v_o$ . Also since inverting input terminal is at virtual ground, the effective

input impedance is  $R_1$ . The value of  $R_1$  should be kept fairly large to avoid loading effect. This however, limits the gain that can be obtained from this circuit. A load resistor  $R_L$  is usually put at the output in actual practice otherwise, the input impedance of the measuring device such as oscilloscope or DVM acts as the load. The calculation of load and output currents is shown in the Example 2.2.

If, however, resistances  $R_1$  and  $R_f$  in Fig. 2.5 (a) are replaced by impedances  $Z_1$  and  $Z_f$  respectively, then the voltage gain,  $A_{CL}$  will be

$$A_{CL} = -\frac{Z_f}{Z_1} \quad (2.5)$$

This expression for the voltage gain will be used in op-amp application, such as integrator, differentiator etc.

### Example 2.1

Design an amplifier with a gain of  $-10$  and input resistance equal to  $10 \text{ k}\Omega$ .

### Solution

Since the gain of the amplifier is negative, an inverting amplifier has to be made.

In Fig. 2.5 (a) choose  $R_1 = 10 \text{ k}\Omega$

Then  $R_f = -A_{CL} R_1$  (from Eq. 2.4)  
 $= -(-10) \times 10 \text{ k}\Omega = 100 \text{ k}\Omega$

### Example 2.2

In Fig. 2.5 (b),  $R_1 = 10 \text{ k}\Omega$ ,  $R_f = 100 \text{ k}\Omega$ ,  $v_i = 1 \text{ V}$ . A load of  $25 \text{ k}\Omega$  is connected to the output terminal. Calculate (i)  $i_1$  (ii)  $v_o$  (iii)  $i_L$  and total current  $i_o$  into the output pin.

### Solution

$$(a) i_1 = \frac{v_i}{R_1} = \frac{1 \text{ V}}{10 \text{ k}\Omega} = 0.1 \text{ mA}$$

$$(b) v_o = -\frac{R_f}{R_1} v_i = -\frac{100 \text{ k}\Omega}{10 \text{ k}\Omega} 1 \text{ V} = -10 \text{ V}$$

$$(c) i_L = \frac{v_o}{R_L} = \frac{10 \text{ V}}{25 \text{ k}\Omega} = 0.4 \text{ mA}$$

The direction of  $i_L$  is shown in Fig. 2.5 (b).

(d)  $i_1$  as calculated above is  $0.1 \text{ mA}$ .

Therefore, total current  $i_o = i_1 + i_L = 0.1 \text{ mA} + 0.4 \text{ mA} = 0.5 \text{ mA}$ . In an inverting amplifier, for a +ive input, output will be -ive, therefore the direction of  $i_o$  is as shown in Fig. 2.5 (b).

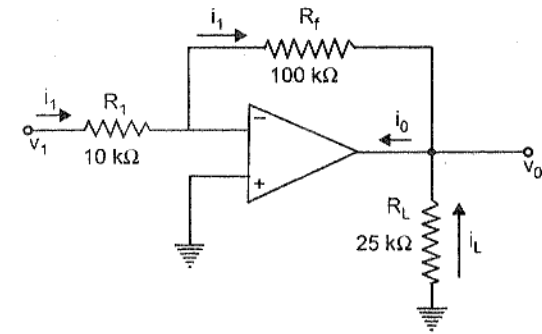


Fig. 2.5 (b) Circuit for Example 2.2

### Practical Inverting Amplifier

Equation (2.4) is valid only if the op-amp is an ideal one. For a practical op-amp, the expression for the closed loop voltage gain should be calculated using the low frequency model of Fig. 2.4 (b). The equivalent circuit of a practical inverting amplifier is shown in Fig. 2.6 (a). This circuit can be simplified by replacing the signal source  $v_i$  and resistors  $R_1$  and  $R_f$  by Thevenin's equivalent as shown in Fig. 2.6 (b) which is analysed to calculate the exact expression for closed loop gain,  $A_{CL}$  and input impedance  $R_{if}$ .

The input impedance  $R_i$  of an op-amp is usually much greater than  $R_1$ , so one may assume,  $v_{eq} \equiv v_i$  and  $R_{eq} \equiv R_1$ . From the output loop in Fig. 2.6 (b)

$$v_o = iR_o + A_{OL} v_d \quad (2.6)$$

$$\text{Also } v_d + iR_f + v_o = 0 \quad (2.7)$$

Putting the value of  $v_d$  from Eq. (2.6) to Eq. (2.7) and simplifying,

$$v_o(1 + A_{OL}) = i(R_o - A_{OL} R_f) \quad (2.8)$$

Also the KVL loop equation gives

$$v_i = i(R_1 + R_f) + v_o \quad (2.9)$$

Putting the value of  $i$  from Eq. (2.8) in Eq. (2.9) and solving for closed

loop gain  $A_{CL} = \frac{v_o}{v_i}$ , gives

$$A_{CL} = \frac{v_o}{v_i} = \frac{R_o - A_{OL} R_f}{R_o + R_f + R_1(1 + A_{OL})} \quad (2.10)$$

It can be seen from Eq. (2.10) that if  $A_{OL} \gg 1$  and  $A_{OL} R_1 \gg R_o + R_f$ ,

$$A_{CL} \cong -\frac{R_f}{R_1}$$

**Input Resistance  $R_{if}$**

In Fig. 2.6 (b), it can be seen that

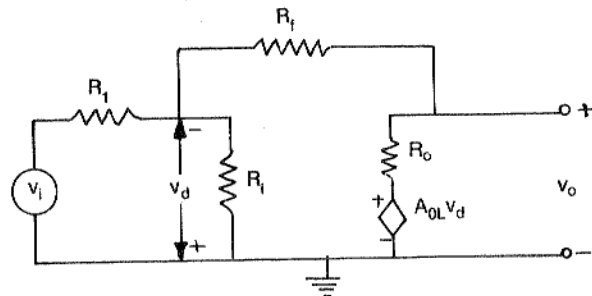
$$R_{if} = \frac{v_d}{i}$$

Writing the loop equation and solving for  $R_{if}$ ,

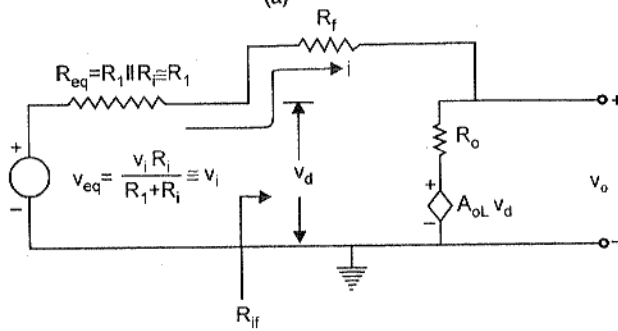
$$v_d + i(R_f + R_o) + A_{OL} v_d = 0$$

We obtain

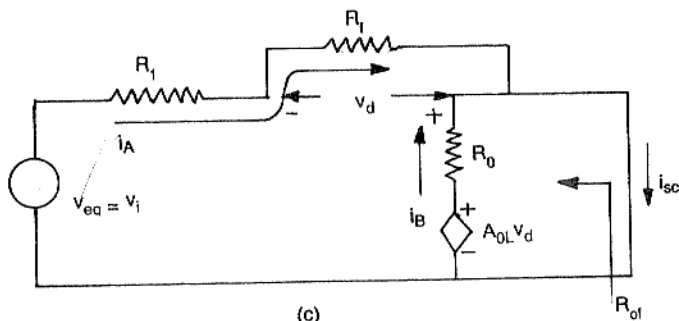
$$R_{if} = \frac{R_f + R_o}{1 + A_{OL}} \tag{2.11}$$



(a)



(b)



(c)

**Fig. 2.6** (a) Equivalent circuit of a practical op-amp inverting amplifier (b) Simplified circuit by using Thevenin's equivalent (c) Equivalent circuit for computing  $R_{of}$

**Output Resistance  $R_{of}$**

Output impedance  $R_{of}$  (without load resistance  $R_L$ ) is calculated from the open circuit output voltage  $v_{oc}$  and short circuit output current  $i_{sc}$ . Now consider the circuit shown in Fig. 2.6 (c). Under short circuit conditions at output,

$$i_A = \frac{v_i - 0}{R_1 + R_f} \tag{2.12}$$

and,

$$i_B = \frac{A_{OL} v_d}{R_o} \tag{2.13}$$

Since

$$v_d = -i_A R_f$$

So,

$$i_B = \frac{A_{OL} i_A R_f}{R_o}$$

Solving for  $i_{sc} = i_A + i_B$ , we obtain

$$i_{sc} = i_A + i_B = v_i \frac{(R_o - A_{OL} R_f)}{R_o (R_1 + R_f)} \tag{2.14}$$

Since

$$R_{of} = \frac{v_{oc}}{i_{sc}}$$

and

$$A_{CL} = \frac{v_{oc}}{v_i}$$

Therefore,

$$R_{of} = \frac{A_{CL} v_i}{v_i \left[ \frac{(R_o - A_{OL} R_f)}{R_o (R_1 + R_f)} \right]} \tag{2.15}$$

Putting the value of  $A_{CL}$  from Eq. (2.10), we obtain

$$R_{of} = \frac{R_o (R_1 + R_f)}{R_o + R_f + R_1 (1 + A_{OL})} \tag{2.16}$$

Eq. (2.16) may alternatively be written as

$$R_{of} = \frac{\frac{R_o (R_1 + R_f)}{R_o + R_1 + R_f}}{1 + \frac{R_1 A_{OL}}{R_o + R_1 + R_f}} \tag{2.17}$$

It may be seen that numerator consists of a term  $R_o \parallel (R_1 + R_f)$  and is therefore smaller than  $R_o$ . The output resistance  $R_{of}$  (with feedback) is, therefore always less than  $R_o$  and for  $A_{CL} \rightarrow \infty$ ,  $R_{of} \rightarrow 0$ .

### 2.3.4 The Non-Inverting Amplifier

If the signal is applied to the non-inverting input terminal and feedback is given as shown in Fig. 2.7 (a), the circuit amplifies without inverting the input signal. Such a circuit is called non-inverting amplifier. It may be noted that it is also a negative feed-back system as output is being fed back to the inverting input terminal.

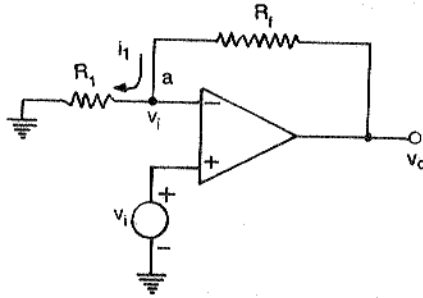


Fig. 2.7 (a) Non-inverting amplifier

As the differential voltage  $v_d$  at the input terminal of op-amp is zero, the voltage at node 'a' in Fig. 2.7 (a) is  $v_i$ , same as the input voltage applied to non-inverting input terminal. Now  $R_f$  and  $R_1$  forms a potential divider. Hence

$$v_i = \frac{v_o}{R_1 + R_f} R_1 \quad (2.18)$$

as no current flows into the op-amp.

$$\frac{v_o}{v_i} = \frac{R_1 + R_f}{R_1} = 1 + \frac{R_f}{R_1} \quad (2.19)$$

Thus, for non-inverting amplifier the voltage gain,

$$A_{CL} = \frac{v_o}{v_i} = 1 + \frac{R_f}{R_1} \quad (2.20)$$

The gain can be adjusted to unity or more, by proper selection of resistors  $R_f$  and  $R_1$ . Compared to the inverting amplifier, the input resistance of the non-inverting amplifier is extremely large ( $= \infty$ ) as the op-amp draws negligible current from the signal source.

#### Practical Non-Inverting Amplifier

The analysis of a practical non-inverting amplifier can be performed by using the equivalent circuit shown in Fig. 2.7 (b). Writing KCL at the input node,

$$(v_i - v_d) Y_1 + v_d Y_i + (v_i - v_d - v_o) Y_f = 0$$

or,

$$-(Y_1 + Y_i + Y_f) v_d + (Y_1 + Y_f) v_i = Y_f v_o \quad (2.21)$$

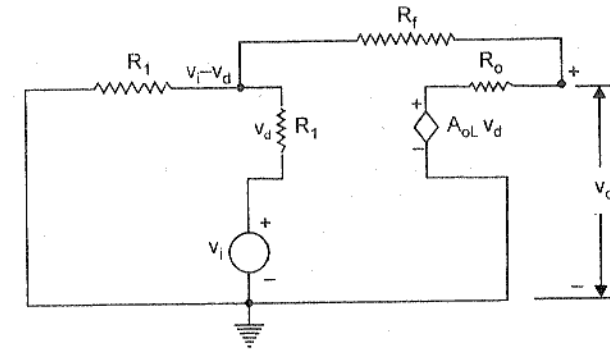


Fig. 2.7 (b) Equivalent circuit of non-inverting amplifier using low frequency model

Similarly at output node, KCL gives

$$(v_i - v_d - v_o) Y_f + (A_{OL} v_d - v_o) Y_o = 0$$

$$\text{that is, } -(Y_f - A_{OL} Y_o) v_d + Y_f v_i = (Y_f + Y_o) v_o \quad (2.22)$$

Now solving Eqs. (2.21) and (2.22) for  $v_o/v_i$ , we get

$$A_{CL} = \frac{v_o}{v_i} = \frac{A_{OL} Y_o (Y_1 + Y_f) + Y_f Y_i}{(A_{OL} + 1) Y_o Y_f + (Y_1 + Y_i) (Y_f + Y_o)} \quad (2.23)$$

where all admittances have been taken for simplicity.

If  $A_{OL} \rightarrow \infty$ , Eq. (2.23) reduces to

$$A_{CL} \approx \frac{A_{OL} Y_o (Y_1 + Y_f)}{A_{OL} Y_o Y_f} = \frac{Y_1 + Y_f}{Y_f} = 1 + \frac{Y_1}{Y_f}$$

$$= 1 + \frac{R_f}{R_1}$$

which is the same expression as in Eq. (2.20)

### 2.3.5 Voltage Follower

In the non-inverting amplifier of Fig. 2.7 (a) if  $R_f = 0$  and  $R_1 = \infty$ , we get the modified circuit of Fig. 2.7 (c). From Eq. (2.20) we get,

$$v_o = v_i \quad (2.24)$$

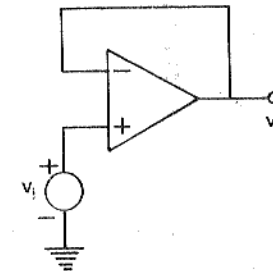


Fig. 2.7 (c) Voltage follower

That is, the output voltage is equal to input voltage, both in magnitude and phase. In other words, we can also say that the output voltage follows the input voltage exactly. Hence, the circuit is called a voltage follower. The use of the unity gain circuit lies in the fact that its input impedance is very high (i.e.  $M\Omega$  order) and output impedance is zero. Therefore, it draws negligible current from the source. Thus a voltage follower may be used as buffer for impedance matching, that is, to connect a high impedance source to a low impedance load.

### Example 2.3

Design an amplifier with a gain of +5 using one op-amp.

#### Solution

Since the gain is positive, we have to make a non-inverting amplifier. In Fig. 2.7 (a) select  $R_1 = 10 \text{ k}\Omega$ . Then from Eq. (2.20)

$$A_{CL} = 1 + R_f/R_1$$

$$\text{or,} \quad 5 = 1 + R_f/10 \text{ k}\Omega$$

$$\text{or,} \quad R_f = 4 \times 10 \text{ k}\Omega = 40 \text{ k}\Omega$$

### Example 2.4

In the circuit of Fig. 2.7 (a), let  $R_1 = 5 \text{ k}\Omega$ ,  $R_f = 20 \text{ k}\Omega$  and  $v_i = 1 \text{ V}$ . A load resistor of  $5 \text{ k}\Omega$  is connected at the output as in Fig. 2.5 (b). Calculate, (i)  $v_o$  (ii)  $A_{CL}$  (iii) the load current  $i_L$  (iv) the output current  $i_o$  indicating proper direction of flow.

#### Solution

$$(i) \quad v_o = \left(1 + \frac{R_f}{R_1}\right) v_i = \left(1 + \frac{20 \text{ k}\Omega}{5 \text{ k}\Omega}\right) (1 \text{ V}) = 5 \text{ V}$$

$$(ii) \quad A_{CL} = \frac{v_o}{v_i} = \frac{5 \text{ V}}{1 \text{ V}} = 5$$

$$(iii) \quad i_L = \frac{v_o}{R_L} = \frac{5 \text{ V}}{5 \text{ k}\Omega} = 1 \text{ mA}$$

$$(iv) \quad i_1 = \frac{v_i}{R_1} = \frac{v_o - v_i}{R_f} = 0.2 \text{ mA}$$

Therefore,  $i_o = i_L + i_1 = 1 \text{ mA} + 0.2 \text{ mA} = 1.02 \text{ mA}$

The op-amp output current  $i_o$  flows outwards from the output junction.

### 2.3.6 Differential Amplifier

A circuit that amplifies the difference between two signals is called a difference or differential amplifier. This type of the amplifier is very useful in instrumentation circuits (see section 4.3). A typical circuit is shown in Fig. 2.8. Since, the differential voltage at the input terminals of the op-amp is zero, nodes 'a' and 'b' are at the same potential, designated as  $v_3$ . The nodal equation at 'a' is,

$$\frac{v_3 - v_2}{R_1} + \frac{v_3 - v_o}{R_2} = 0 \quad (2.25)$$

and at 'b' is

$$\frac{v_3 - v_1}{R_1} + \frac{v_3}{R_2} = 0 \quad (2.26)$$

Rearranging, we get

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_2}{R_1} = \frac{v_o}{R_2} \quad (2.27)$$

$$\left(\frac{1}{R_1} + \frac{1}{R_2}\right) v_3 - \frac{v_1}{R_1} = 0 \quad (2.28)$$

Subtracting Eq. (2.28) from (2.27) we get,

$$\frac{1}{R_1} (v_1 - v_2) = \frac{v_o}{R_2} \quad (2.29)$$

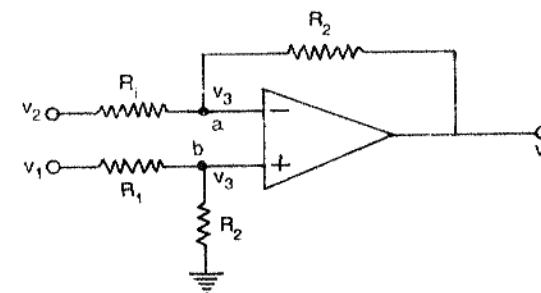


Fig. 2.8 A differential amplifier

Therefore,

$$v_o = \frac{R_2}{R_1} (v_1 - v_2) \quad (2.30)$$

Such a circuit is very useful in detecting very small differences in signals, since the gain  $R_2/R_1$  can be chosen to be very large. For



example, if  $R_2 = 100 R_1$ , then a small difference  $v_1 - v_2$  is amplified 100 times.

### Difference-mode and Common-mode Gains

In Eq. (2.30) if  $v_1 = v_2$  then  $v_o = 0$ . That is, the signal common to both inputs gets cancelled and produces no output voltage. This is true for an ideal op-amp, however, a practical op-amp exhibits some small response to the common mode component of the input voltages too. For example, the output  $v_o$  will have different value for case (i) with  $v_1 = 100 \mu\text{V}$  and  $v_2 = 50 \mu\text{V}$  and case (ii) with  $v_1 = 1000 \mu\text{V}$  and  $v_2 = 950 \mu\text{V}$ , even though the difference signal  $v_1 - v_2 = 50 \mu\text{V}$  in both the cases. The output voltage depends not only upon the difference signal  $v_d$  at the input, but is also affected by the average voltage of the input signals, called the common-mode signal  $v_{\text{CM}}$  defined as,

$$v_{\text{CM}} = \frac{v_1 + v_2}{2}$$

For differential amplifier, though the circuit is symmetric, but because of the mismatch, the gain at the output with respect to the positive terminal is slightly different in magnitude to that of the negative terminal. So, even with the same voltage applied to both inputs, the output is not zero. The output, therefore, must be expressed as,

$$v_o = A_1 v_1 + A_2 v_2 \quad (2.31)$$

where,  $A_1$  ( $A_2$ ) is the voltage amplification from input 1 (2) to the output with input 2(1) grounded. Since  $v_{\text{CM}} = (v_1 + v_2)/2$  and  $v_d = (v_1 - v_2)$ ,

$$v_1 = v_{\text{CM}} + \frac{1}{2} v_d \quad (2.32)$$

$$\text{and} \quad v_2 = v_{\text{CM}} - \frac{1}{2} v_d \quad (2.33)$$

Substituting the value of  $v_1$  and  $v_2$  in Eq. (2.31), we get

$$v_o = A_{\text{DM}} v_d + A_c v_c \quad (2.34)$$

$$\text{where,} \quad A_{\text{DM}} = \frac{1}{2} (A_1 - A_2) \quad (2.35)$$

$$\text{and} \quad A_{\text{CM}} = A_1 + A_2 \quad (2.36)$$

The voltage gain for the difference signal is  $A_{\text{DM}}$  and that for the common-mode signal is  $A_{\text{CM}}$ .

### 2.3.7 Common-Mode Rejection Ratio

The relative sensitivity of an op-amp to a difference signal as compared to a common-mode signal is called common-mode rejection ratio

(CMRR) and gives the figure of merit  $\rho$  for the differential amplifier. So, CMRR is given by:

$$\rho = \left| \frac{A_{\text{DM}}}{A_{\text{CM}}} \right| \quad (2.37)$$

and is usually expressed in decibels (dB). For example, the  $\mu\text{A741}$  op-amp has a minimum CMRR of 70 dB whereas a precision op-amp such as  $\mu\text{A725A}$  has a minimum CMRR of 120 dB. Clearly, we should have  $A_{\text{DM}}$  large and  $A_{\text{CM}}$  should be zero ideally. So, higher the value of CMRR, better is the op-amp.

### Example 2.5

In Fig. 2.9 is shown a differential amplifier using ideal op-amp.

- (a) Find the output voltage  $v_o$ .  
 (b) Show that the output corresponding to common-mode voltage

$v_{\text{CM}} = \frac{(v_1 + v_2)}{2}$  is zero if  $\frac{R'}{R} = \frac{R_2}{R_1}$ . Find  $v_o$  in this case.

- (c) Find CMRR of the amplifier if  $\frac{R'}{R} \neq \frac{R_2}{R_1}$

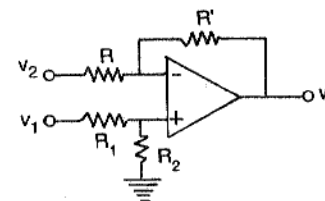


Fig. 2.9 Circuit of Example 2.5

### Solution

The voltage at the non-inverting input terminal is  $\frac{R_2}{R_1 + R_2} v_1$ . Using principle of superposition and Eqs. (2.4) and (2.20), we have

$$(a) \quad v_o = -\frac{R'}{R} v_2 + \left( \frac{R + R'}{R} \right) \left( \frac{R_2}{R_1 + R_2} v_1 \right) \quad (2.38)$$

$$(b) \quad v_{\text{CM}} = \frac{1}{2} (v_1 + v_2) \text{ and } v_d = (v_1 - v_2)$$

$$\text{So, } v_1 = v_{\text{CM}} + \frac{v_d}{2} \text{ and } v_2 = v_{\text{CM}} - \frac{v_d}{2}$$

$v_o$  from Eq. (2.38) is,

$$v_o = -\frac{R'}{R} \left( v_{CM} - \frac{v_d}{2} \right) + \frac{R_2}{R} \frac{R+R'}{R_1+R_2} \left( v_{CM} + \frac{v_d}{2} \right)$$

$$= \left( \frac{R_2}{R} \frac{R+R'}{R_1+R_2} - \frac{R'}{R} \right) v_{CM} + \left( \frac{R'}{R} + \frac{R_2}{R} \frac{R+R'}{R_1+R_2} \right) \frac{v_d}{2} \quad (2.39)$$

Now, if  $\frac{R'}{R} = \frac{R_2}{R_1}$ , we get,

$$\frac{R'}{R} + 1 = \frac{R_2}{R_1} + 1$$

$$\text{or, } \frac{R'+R}{R} = \frac{R_1+R_2}{R_1}$$

So, from Eq. (2.39) the term corresponding to  $v_{CM}$  is zero, and

$$v_o = \left( \frac{R'}{R} + \frac{R_2}{R_1} \right) \frac{v_d}{2} = \left( \frac{R_2}{R_1} \right) v_d \quad (2.40)$$

$$(c) \text{ CMRR} = \frac{A_{DM}}{A_{CM}}$$

From Eq. (2.39), find (i)  $A_{DM} = v_o/v_d$  by putting  $v_{CM} = 0$

and (ii)  $A_{CM} = v_o/v_{CM}$  by putting  $v_d = 0$

then we get

$$\text{CMRR} = \frac{R'(R_1+R_2) + R_2(R+R')}{R'(R_1+R_2) - R_1(R+R')} \quad (2.41)$$

## 2.4 OPERATIONAL AMPLIFIER INTERNAL CIRCUIT

Commercial IC op-amps usually consists of four cascaded blocks as shown in Fig. 2.10. The first two stages are cascaded differential amplifiers used to provide high gain and high input resistance. The third stage acts as a buffer as well as a level shifter. The buffer is usually an emitter follower whose input impedance is very high so that it prevents loading of the high gain stage. The level shifter adjusts the d.c. voltages so that output voltage is zero for zero inputs. The adjustment of d.c. level is required as the gain stages are direct coupled. As it is not possible to fabricate large value of capacitors, all IC's are direct coupled usually. The output stage is designed to provide a low output impedance as demanded by the ideal op-amp characteristics. The output voltage should swing symmetrically with respect to ground. To allow such symmetrical swing, the amplifier is provided with both

positive and negative supply voltages. Power supply voltages of  $\pm 15V$  are common. Additionally, an op-amp generally incorporates circuitry to provide drift compensation and frequency compensation which are discussed in section 3.3.3.

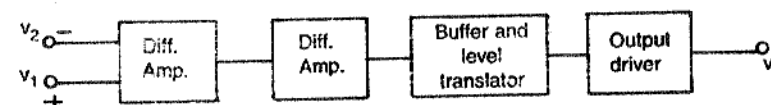


Fig. 2.10 Block schematic of an op-amp

Before describing the detailed IC circuit, we shall discuss each of the blocks in detail.

### 2.4.1 Differential Amplifier

The main purpose of the difference amplifier stage is to provide high gain to the difference-mode signal and cancel the common-mode signal. The relative sensitivity of an op-amp to a difference signal as compared to common-mode signal is called common-mode rejection ratio (CMRR) and gives the figure of merit of the differential amplifier. The higher the value of CMRR, better is the op-amp. Another requisite of a good op-amp is that it should have high input impedance. In this section, we discuss in detail, the various circuits and then modifications to achieve these characteristics of a good op-amp.

A cascaded dc amplifier can provide high gain down to zero frequency as it has no coupling capacitor. However, such an amplifier suffers from the major problem of drift of the operating point due to temperature dependency of  $I_{CBO}$ ,  $V_{BE}$  and  $h_{FE}$  of the transistor. This problem can be eliminated by using a balanced or differential amplifier as shown in Fig. 2.11 (a). It may be seen that it is essentially an

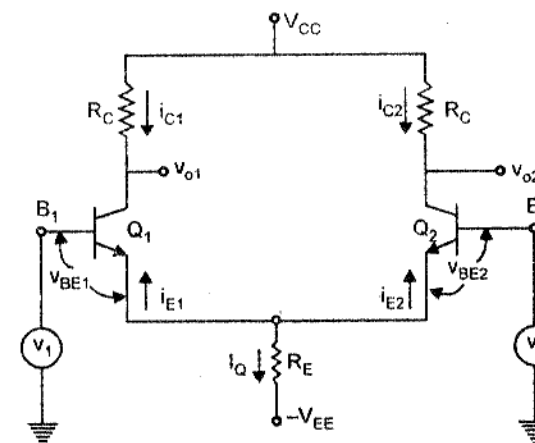


Fig. 2.11 (a) The basic differential amplifier

emitter-coupled differential amplifier. This circuit has low drift on account of symmetrical construction. It can be designed to give high input resistance. It has two input terminals and it may be seen easily that terminal  $B_2$  is the inverting input terminal since transistor  $Q_2$  provides a phase shift of  $180^\circ$  for the output taken at the collector of  $Q_2$ . Obviously,  $B_1$  is the non-inverting input terminal. So, a differential amplifier is well suited to obtain the ideal characteristics of an op-amp as discussed in Sec. 2.3.

A differential amplifier of the type shown in Fig. 2.11 (a) can be used in four different configurations depending upon the number of input signals used and the way output is taken. These four configurations are:

- (i) Differential-input, differential-output or Dual-input balanced-output
- (ii) Differential-input, single ended-output
- (iii) Single-input, differential-output
- (iv) Single-input, single ended-output

If signal is applied to both the inputs, then it is differential input or Dual input and the difference of signals applied to the two inputs gets amplified. In many applications a single input is only used as we shall see later. Similarly, if output voltage is measured between two collectors then it is a differential output. This is also referred to as a balanced output, as both collectors are at the same d.c. potential w.r.t. ground. We will come across these various configuration as we proceed further.

To understand the working of a differential amplifier first consider the case when both the bases  $B_1$  &  $B_2$  are joined together and connected to a voltage  $v_{CM}$  called the common-mode voltage. Thus in Fig. 2.11 (b),  $v_1 = v_2 = v_{CM}$ . As transistors  $Q_1$  and  $Q_2$  are matched and due to symmetry of the circuit, the current  $I_Q$  divides equally through transistors  $Q_1$  and  $Q_2$ , that is,  $i_{E1} = i_{E2} = -I_Q/2$ . The collector currents  $i_{C1}$  and  $i_{C2}$  through the resistors  $R_C$  is  $\alpha_F I_Q/2$ . The voltage at each of the collectors will be  $V_{CC} - \alpha_F \frac{I_Q}{2} R_C$  and, therefore the difference of the voltage between the two collectors ( $v_{01} - v_{02}$ ) will be zero. Now, even if the value of  $v_{CM}$  is changed, the voltage across the collectors will not change. Thus, the differential pair does not respond to (or rejects) the common-mode input signals. Now, consider the case when the voltage  $v_2$  is made zero and voltage  $v_1 = 1$  V (say) as shown in Fig. 2.11 (c). It can be seen that the transistor  $Q_1$  will conduct and transistor  $Q_2$  will be off. The entire current  $I_Q$  will now flow through  $Q_1$ . Since  $Q_1$  is on, the voltage at its emitter will be 0.3 V. This will make emitter-base junction of  $Q_2$  reverse-biased and thus  $Q_2$  will be off. The collector voltages will be  $v_{01} = V_{CC} - \alpha_F I_Q R_C$  and  $v_{02} = V_{CC}$ .

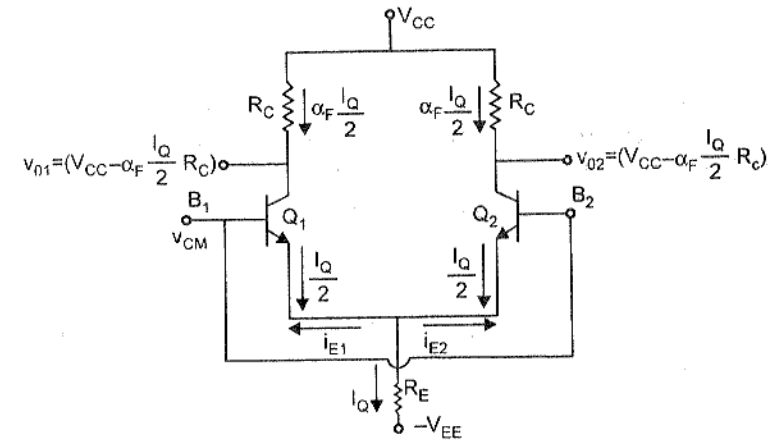


Fig. 2.11 (b) The differential pair with a common-mode input signal  $v_{CM}$

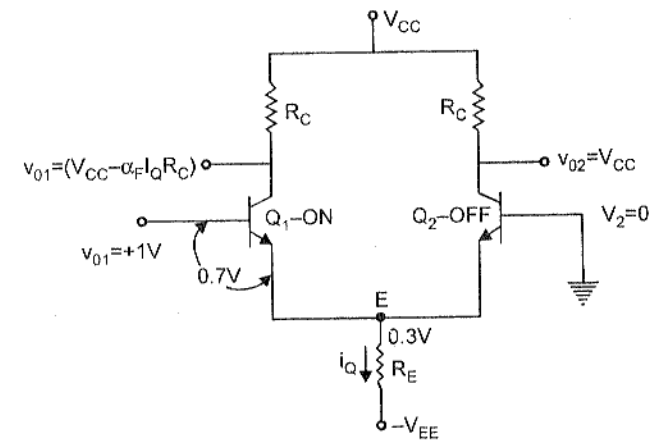


Fig. 2.11 (c) The differential pair with 'large' differential input signal

If, however,  $v_1 = -1$  V and  $v_2 = 0$  V, it can be seen that  $Q_1$  will be off and the entire current  $I_Q$  will flow through  $Q_2$ . The voltage at the common emitter point 'E' will now be  $-0.7$  V which makes  $Q_1$  off and  $Q_2$  on. The collector voltages will be  $v_{01} = V_{CC}$  and  $v_{02} = V_{CC} - \alpha_F I_Q R_C$ .

Thus, we see that the differential pair responds only to the difference mode signals and rejects common-mode signals. In the next section, we discuss the transfer characteristics of the circuit to show that a differential pair can be used either as a switch or a linear amplifier.

#### 2.4.2 Transfer Characteristics

In Fig. 2.11 (a) collector currents  $i_{C1}$  and  $i_{C2}$  for transistors  $Q_1$  and  $Q_2$  biased in the forward-active mode may be given by (neglecting reverse saturation currents of the collector base junction)

$$i_{C1} = \alpha_F I_{ES} e^{v_{BE1}/V_T} \quad (2.42)$$

$$i_{C2} = \alpha_F I_{ES} e^{v_{BE2}/V_T} \quad (2.43)$$

Here,  $I_{ES}$  is the reverse saturation current of emitter-base junction and  $V_T$  is volts equivalent of temperature.

From Eqs. (2.42) and (2.43), we may write

$$\frac{i_{C1}}{i_{C2}} = e^{(v_{BE1} - v_{BE2})/V_T} \quad (2.44)$$

We may also write KVL for the loop containing two emitter-base junctions as

$$v_1 - v_{BE1} + v_{BE2} - v_2 = 0$$

or  $v_{BE1} - v_{BE2} = v_1 - v_2 = v_d$

where,  $v_d$  is the difference of two input voltages.

Also in Fig. 2.11 (a)

$$\begin{aligned} I_Q &= -(i_{E1} + i_{E2}) \\ &= \frac{i_{C1}}{\alpha_F} + \frac{i_{C2}}{\alpha_F} \\ &= \frac{i_{C1}}{\alpha_F} \left( 1 + \frac{i_{C2}}{i_{C1}} \right) \end{aligned} \quad (2.45)$$

Using Eqs. (2.44) & (2.45) and solving for  $i_{C1}$  and  $i_{C2}$ , gives

$$i_{C1} = \frac{\alpha_F I_Q}{1 + e^{-v_d/V_T}} \quad (2.46)$$

$$i_{C2} = \frac{\alpha_F I_Q}{1 + e^{v_d/V_T}} \quad (2.47)$$

From Eqs. (2.46) and (2.47), the transfer characteristics ( $i_C$  vs  $v_d$ ) for a differential amplifier are obtained as shown in Fig. 2.12.

The following important points are observed from the transfer characteristics:

1. For  $v_d > 4 V_T$  ( $\sim 100$  mV),  $i_{C1} = \alpha_F I_Q$  and  $i_{C2} = 0$ , Hence

$$v_{01} = V_{CC} - \alpha_F I_Q R_C$$

and  $v_{02} = V_{CC}$

By proper choice of  $R_C$ ,  $v_{01}$  can be made very small.

2. For  $v_d < -4 V_T$ ,  $i_{C1} = 0$  and  $i_{C2} = \alpha_F I_Q$ . Hence  $v_{01} = V_{CC}$  and  $v_{02}$  is negligible. Thus, for  $4V_T < v_d < -4V_T$ , we can say that a differential amplifier can be made to function as a switch.
3. The differential amplifier functions as a very good limiter for  $v_d > \pm 4 V_T$ .

4. DA can function as an automatic gain control (AGC) by varying  $I_Q$ .
5. Between the values  $-2V_T \leq v_d \leq 2V_T$ , DA functions as a linear amplifier.

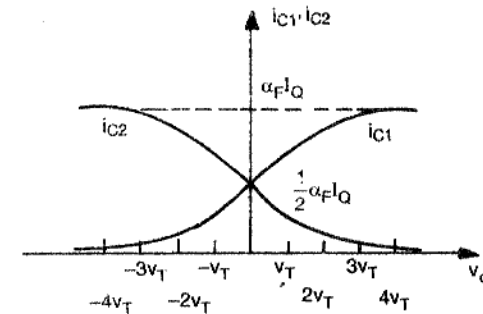


Fig. 2.12 Transfer characteristics ( $i_C$  vs  $v_d$ ) for the differential pair

### 2.4.3 Low Frequency Small Signal Analysis of Differential Amplifier

An ideal dual-input balanced output differential amplifier as shown in Fig. 2.11 (a), should amplify only the differential signal at the two inputs and reject the signal common to these inputs. As transistors  $Q_1$  and  $Q_2$  are a matched pair of transistors, thus any unwanted signal, such as noise or hum pick up which is common to both the inputs would get rejected. However in a practical case transistors  $Q_1$  and  $Q_2$  are not equally matched and output does appear even when same voltage is applied to the two input terminals. In this section, we will discuss how to compute the small signal differential mode gain,  $A_{DM}$  and common-mode gain  $A_{CM}$ . These expressions help in finding the figure of merit CMRR of the differential amplifier and hence the ways to improve it.

The a.c. analysis of the differential amplifier can be performed either by using hybrid- $\pi$  model or  $h$ -parameter model. Both the approaches have been dealt with.

#### Differential-mode gain, $A_{DM}$

In Fig. 2.11 (a) for  $v_1 = v_2$ , the current  $I_Q$  divides equally into the two transistors  $Q_1$  and  $Q_2$  because of the symmetry of the circuit. However, if  $v_1$  is now increased by an incremental voltage (small signal)  $v_d/2$  and  $v_2$  is decreased by  $v_d/2$ , it can be seen that the differential amplifier is being fed by differential small signal  $v_d$ . The common mode small signal is naturally zero. The collector current  $i_{C1}$  will now increase by an incremental current  $i_c$  and  $i_{C2}$  will decrease by an equal amount. The sum of total currents in transistors  $Q_1$  and  $Q_2$  however remains constant as constrained by the constant current  $I_Q$ .

As there is no change of current through  $R_E$ , the voltage  $V_E$  at the common emitter point 'E' remains constant. Thus, for small signal analysis, the common emitter point 'E' can be considered to be at ground potential. Fig. 2.13 (a) shows the small signal equivalent circuit of the differential amplifier under the differential input signal conditions described above. It may be noted that for differential amplifier to behave as a linear amplifier, the differential signal  $v_d \leq 2V_T$  (that is,  $v_d$  should be smaller than about 50 mV) as discussed in the transfer characteristics (section 2.4.2).

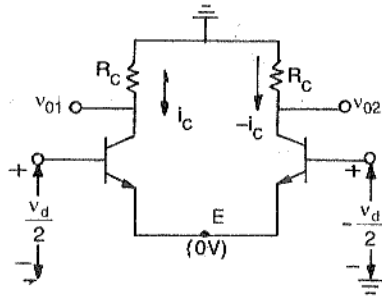


Fig. 2.13 (a) Differential amplifier when differential input signal applied.

**Analysis**

**(i) Using hybrid- $\pi$  Model**

Since the performance of two sides of the differential amplifier is identical, we need to analyze only one side of the differential amplifier called differential-half circuit. Fig. 2.13 (b) shows a single stage CE transistor amplifier fed by a small signal voltage  $v_d/2$  and its a.c. equivalent circuit using hybrid- $\pi$  model is shown in Fig. 2.13 (c).

From Fig. 2.13 (c),

$$\frac{v_{o1}}{v_d/2} = -g_m R_C$$

or 
$$\frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C \tag{2.48}$$

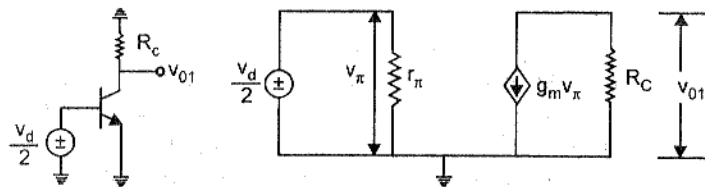


Fig. 2.13 (b) Differential mode half circuit (c) ac-equivalent circuit using hybrid- $\pi$  model.

Similarly, it can be seen that

$$\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C \tag{2.49}$$

The output voltage signal of a differential amplifier can be taken either differentially (i.e. between the two collectors) or single-ended (i.e. between one collector and ground). If the output is taken differentially, then the differential-mode gain,  $A_{DM}$  is given by

$$A_{DM} = \frac{v_{o1} - v_{o2}}{v_d} = -g_m R_C \text{ (differential-input, differential-output)} \tag{2.50}$$

On the other hand, if output is single-ended, (say between collector of transistor  $Q_1$  and ground), then the differential-mode gain  $A_{DM}$  is given by

$$A_{DM} = \frac{v_{o1}}{v_d} = -\frac{1}{2} g_m R_C \text{ (differential-input, single-ended output)} \tag{2.51(a)}$$

and 
$$\frac{v_{o2}}{v_d} = \frac{1}{2} g_m R_C \tag{2.51(b)}$$

In the above analysis, we have not included the transistor model parameter  $r_o$ . If  $r_o$  is included, Eq. (2.50) will modify to

$$A_{DM} = -g_m (R_C \parallel r_o).$$

**(ii) Using 'h' parameters**

The a.c. equivalent circuit for Fig. 2.13(b) using approximate h-parameter model is shown in Fig. 2.13(d)

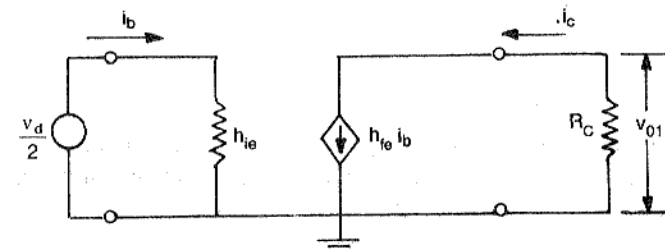


Fig. 2.13 (d) Small signal equivalent circuit of differential half circuit using h-parameter model

From Fig. 2.13 (d),

$$v_{o1} = -i_c R_C = -h_{fe} i_b R_C$$

and 
$$\frac{v_d}{2} = i_b h_{ie}$$

Therefore, differential mode gain,  $A_{DM}$  is given by

$$A_{DM} = \frac{v_{01}}{v_d} = -\frac{1}{2} \frac{h_{fe}}{h_{ie}} R_C \quad (\text{Single-ended output}) \quad (2.52 \text{ (a)})$$

Similarly, we may write

$$A_{DM} = \frac{v_{02}}{v_d} = \frac{1}{2} \frac{h_{fe}}{h_{ie}} R_C \quad (\text{Single-ended output}) \quad (2.52 \text{ (b)})$$

If the output is taken differentially between the two collectors, then

$$A_{DM} = \frac{v_{01} - v_{02}}{v_d} = -\frac{h_{fe}}{h_{ie}} R_C \quad (\text{differential-output}) \quad (2.53)$$

In the above analysis, the source resistance  $R_s$  has not been taken into account.

### Common-mode gain, $A_{CM}$

Now, consider the case when  $v_1$  and  $v_2$  both are increased by an incremental voltage  $v_c$ . The differential signal  $v_d$  now is zero and common-mode signal is  $v_c$ . Both the collector currents  $i_{C1}$  and  $i_{C2}$  will increase by an incremental current  $i_c$ . The current through  $R_E$  now increases by  $2i_c$ . The voltage,  $V_E$  at emitter node is now  $2i_c R_E$  and no longer constant. In order to draw the common mode half circuit, replace resistance  $R_E$  by  $2R_E$  as shown in Fig. 2.14 (a). The common-mode gain,  $A_{CM}$  is calculated from the small-signal hybrid- $\pi$  equivalent model shown in Fig. 2.14 (b). It can be seen,

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{v_{02}}{v_c} = \frac{-\beta_0 R_C}{r_\pi + 2(1 + \beta_0)R_E} \quad (2.54)$$

For  $\beta_0 \gg 1$ ,

$$A_{CM} = \frac{-g_m R_C}{1 + 2g_m R_E} \cong -\frac{R_C}{2R_E} \quad (2.55)$$

It can be seen that, if the output is taken differentially, then the output voltage  $v_{01} - v_{02}$  will be zero and the common-mode gain will be zero. However, if the output is taken single ended, the common-mode gain will be finite and given by Eqs. (2.54) and (2.55).

The common mode gain,  $A_{CM}$ , using  $h$ -parameter model can be easily computed as

$$A_{CM} = \frac{v_{01}}{v_c} = \frac{-h_{fe} R_C}{h_{ie} + (1 + h_{fe})2R_E} \quad (2.56)$$

The common-mode rejection ratio (CMRR) is defined as

$$\text{CMRR} = \frac{|A_{DM}|}{|A_{CM}|}$$

For differential-input, differential-output, using Eqs (2.50) and (2.55), we obtain

$$\begin{aligned} \text{CMRR} &\cong \frac{g_m R_C (1 + 2g_m R_E)}{g_m R_C} \\ &= 1 + 2g_m R_E \\ &\cong 2g_m R_E \end{aligned} \quad (2.57)$$

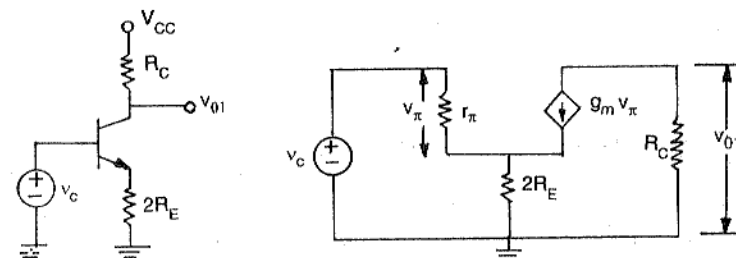


Fig. 2.14 (a) common-mode half circuit (b) ac equivalent ckt using hybrid- $\pi$  model

### 2.4.4 Circuits for Improving CMRR

For CMRR to be large,  $A_{CM}$  should be as small as possible. From Eq. (2.56), it can be seen that  $A_{CM} \rightarrow 0$  as  $R_E \rightarrow \infty$ . There are, however, practical limitations on the magnitude of  $R_E$  because of the quiescent dc voltage across it. If  $R_E$  is made large, the emitter supply  $V_{EE}$  will also have to be increased in order to maintain the proper quiescent current. And if the operating currents of the transistors are allowed to decrease, then  $h_{ie}$  will decrease, thereby decreasing  $h_{fe}$  too. This too will decrease the common mode rejection ratio.

The use of a constant current bias in place of  $R_E$  is found to be a practical solution to the problem discussed above. In Fig. 2.15,  $R_E$  is replaced by a constant current transistor circuit in which  $R_1$ ,  $R_2$  and  $R_3$  can be adjusted to give the same quiescent conditions for the transistors  $Q_1$  and  $Q_2$  as in the original circuit of Fig. 2.11 (a). The modified circuit presents a very high effective emitter resistance  $R_E$  even for very small values of  $R_3$ . Typically,  $R_E$  is hundreds of k $\Omega$  even if  $R_3$  is as small as 1 k $\Omega$ .

Let us calculate the current  $I_Q$  and verify that the emitter circuit really behaves as a constant current source. Writing KVL for the base circuit of  $Q_3$ , we get

$$V_{BE3} + I_3 R_3 = V_D + (V_{EE} - V_D) \frac{R_2}{R_1 + R_2} \quad (2.58)$$

Here  $V_D$  represents the drop across the diode D. If the base current is neglected, then

$$I_Q \approx I_3 = \frac{1}{R_3} \left( \frac{V_{EE} R_2}{R_1 + R_2} + \frac{V_D R_1}{R_1 + R_2} - V_{BE3} \right) \quad (2.59)$$

By proper choice of resistors  $R_1$  and  $R_2$ , it is possible to set,

$$\frac{V_D R_1}{R_1 + R_2} = V_{BE3} \quad (2.60)$$

Then, 
$$I_Q \approx \frac{1}{R_3} \left( \frac{V_{EE} R_2}{R_1 + R_2} \right) \quad (2.61)$$

So, it can be seen that the current  $I_Q$  will be essentially constant as it does not depend upon signal voltages  $v_1$  and  $v_2$ .

What is the use of the diode D in this circuit? The diode D makes  $I_Q$  independent of temperature. We know that  $V_{BE3}$  decreases approximately by 2.5 mV/°C and the diode D also has the same temperature dependence. Hence, the two variations cancel each other and  $I_Q$  becomes independent of temperature. It is usually difficult to satisfy Eq. (2.60) with a single diode D in the circuit of Fig. 2.15 as

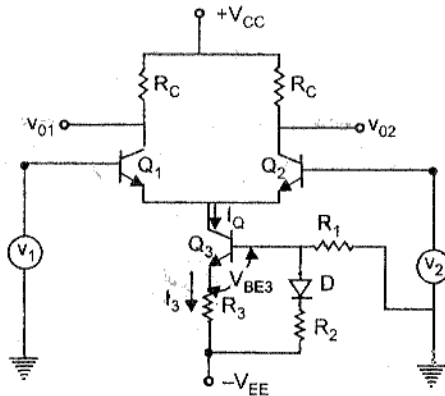


Fig. 2.15 Differential amplifier using constant current bias

$V_D$  and  $V_{BE3}$  have almost the same value. Hence two diodes are normally used for  $V_D$ .

With  $I_Q$  constant, it can be shown that the common-mode gain is zero, so that the circuit provides very high CMRR. Under quiescent conditions (no ac signal) the current  $I_Q$  gets divided equally in identical

transistors  $Q_1$  and  $Q_2$  and  $I_{C1} = I_{C2} = I_{Q/2}$ . Now if the same signal ( $v_1 = v_2$ ) is applied to both the inputs, there will still be no change in the collector currents  $i_{C1}$  and  $i_{C2}$  as  $I_Q$  is constant. Thus the small signal current  $i_c$  flowing through the load resistor  $R_C$  is zero resulting in zero output voltage. Thus we can state that a diff-amp, if supplied by a constant current bias gives very high CMRR. The constant current circuit of the type shown in Fig. 2.15 is used in Motorola MC1530 (Fig. 2.21). A more commonly used IC op-amp  $\mu A-741$  uses a different type of constant current source which is very simple and uses less number of components. This circuit is called current mirror and offers extremely large resistance under a.c. conditions, thereby providing a high value of CMRR.

### Constant Current Source (Current Mirror)

A constant current source makes use of the fact that for a transistor in the active mode of operation, the collector current is relatively independent of the collector voltage. In the basic circuit shown in Fig. 2.16 transistors  $Q_1$  and  $Q_2$  are matched as the circuit is fabricated using IC technology. It may be noted that bases and emitter of  $Q_1$  and  $Q_2$  are tied together and thus have the same  $V_{BE}$ . In addition, transistor  $Q_1$  is connected as a diode by shorting its collector to base.

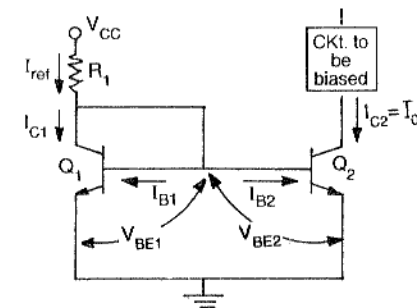


Fig. 2.16 The basic BJT current mirror

The input current  $I_{ref}$  flows through the diode-connected transistor  $Q_1$  and thus establishes a voltage across  $Q_1$ . This voltage in turn appears between the base and emitter of  $Q_2$ . Since  $Q_2$  is identical to  $Q_1$ , the emitter current of  $Q_2$  will be equal to emitter current of  $Q_1$  which is approximately equal to  $I_{ref}$ . Thus, we can say that as long as  $Q_2$  is maintained in the active region, its collector current  $I_{C2} = I_o$  will be approximately equal to  $I_{ref}$ . Since the output current  $I_o$  is a reflection or mirror of the reference current  $I_{ref}$ , the circuit is often referred to as a current mirror.

This mirror effect is however, valid only for large values of  $\beta$ . To study the effect of  $\beta$  on the operation of the current mirror circuit, we analyze it further.

The collector currents  $I_{C1}$  and  $I_{C2}$  for transistors  $Q_1$  and  $Q_2$  can be approximately expressed as

$$\text{Analysis} \quad I_{C1} \cong \alpha_F I_{ES} e^{V_{BE1}/V_T} \quad (2.62)$$

$$I_{C2} \cong \alpha_F I_{ES} e^{V_{BE2}/V_T} \quad (2.63)$$

From Eqns. (2.62) and (2.63), we may write

$$\frac{I_{C2}}{I_{C1}} = e^{(V_{BE2} - V_{BE1})/V_T} \quad (2.64)$$

Since  $V_{BE1} = V_{BE2}$ , we obtain

$$I_{C2} = I_{C1} = I_C = I_0$$

Also since both the transistors are identical,  $\beta_1 = \beta_2 = \beta$ .

KCL at the collector of  $Q_1$  gives

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \quad (2.65)$$

$$= I_{C1} + \frac{I_{C1}}{\beta_1} + \frac{I_{C2}}{\beta_2}$$

$$= I_C \left( 1 + \frac{2}{\beta} \right) \quad (2.66)$$

Solving Eq. (2.66),  $I_C$  may be expressed as

$$I_C = \frac{\beta}{\beta + 2} I_{ref} \quad (2.67)$$

where  $I_{ref}$  from Fig. 2.16 can be seen to be

$$I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \cong \frac{V_{CC}}{R_1} \quad (\text{as } V_{BE} = 0.7 \text{ V is small}) \quad (2.68)$$

From Eq. (2.67), for  $\beta \gg 1$ ,  $\beta / (\beta + 2)$  is almost unity and the output current  $I_0$  is equal to the reference current,  $I_{ref}$  which for a given  $R_1$  is constant. Typically  $I_0$  varies by about 3% for  $50 \leq \beta \leq 200$ .

The circuit however operates as a constant current source as long as  $Q_2$  remains in the active region. From the volt-ampere characteristics of  $Q_2$  shown in Fig. 2.17, it can be seen that for  $V_{CE2} < 0.3 \text{ V}$ ,  $Q_2$  is saturated. For  $V_{CE2} > 0.3 \text{ V}$ , transistor operates in the active

region and  $I_{C2}$  is essentially constant. The slight increase in  $I_{C2}$  is due to Early effect. The slope of the curve in this region gives the output resistance  $r_0$  of the current source.

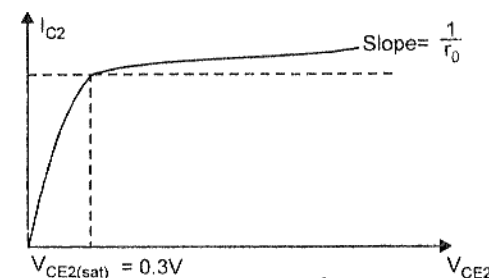


Fig. 2.17 Volt-ampere characteristics for current mirror

The consequences of Early effect is to deviate  $I_{C1}/I_{C2}$  from unity. These, however, are not being discussed here. For all practical purposes, Early voltage may be assumed to be infinite, so that  $r_0 \rightarrow \infty$  and  $I_{C2}$  is constant.

### Example 2.6

The current mirror of Fig. 2.16 is to provide a 1.0 mA current with  $V_{CC} = 10 \text{ V}$ . Assume  $\beta = 125$  and  $V_{BE} = 0.7 \text{ V}$ . Determine (a) the value of  $R_1$  (b) value of  $R_1$  for  $I_C = 10 \mu\text{A}$ .

### Solution

(a) From Eq. (2.67), we have

$$1.0 \text{ mA} = \frac{125}{125 + 2} \times \frac{10 \text{ V} - 0.7 \text{ V}}{R_1}$$

$$R_1 = 9.15 \text{ k}\Omega$$

(b) Again using Eq. (2.67), the value of  $R_1$  is found to be

$$R_1 = 915 \text{ k}\Omega$$

### Widlar current source

The basic current mirror of Fig. 2.16 has a limitation. Whenever, we need low value current source as in example 2.6 part (b), the value of the resistance  $R_1$  required is sufficiently high and can not be fabricated economically in IC circuits. In Fig. 2.18 is shown a widlar current source which is particularly suitable for low value of currents. The circuit differs from the basic current mirror only in the resistance  $R_E$  that is included in the emitter lead of  $Q_2$ . It can be seen that due to  $R_E$ , the base-emitter voltage  $V_{BE2}$  is less than  $V_{BE1}$  and consequently current  $I_0$  is smaller than  $I_{C1}$ .



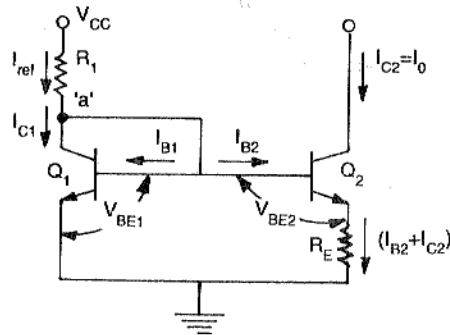


Fig. 2.18 Widlar current source

The ratio of collector currents  $I_{C1}$  and  $I_{C2}$  using Eqs. (2.62) and (2.63) is given by

$$\frac{I_{C1}}{I_{C2}} = e^{(V_{BE1} - V_{BE2})/V_T} \quad (2.69)$$

Taking natural logarithm of both sides, we get

$$V_{BE1} - V_{BE2} = V_T \ln \left( \frac{I_{C1}}{I_{C2}} \right) \quad (2.70)$$

Writing KVL for the emitter base loop

$$V_{BE1} = V_{BE2} + (I_{B2} + I_{C2})R_E \quad (2.71)$$

$$\text{or} \quad V_{BE1} - V_{BE2} = (1/\beta_2 + 1) I_{C2} R_E \quad (2.72)$$

From Eqs. (2.70) and (2.72) we obtain

$$\left( \frac{1}{\beta} + 1 \right) I_{C2} R_E = V_T \ln \frac{I_{C1}}{I_{C2}} \quad (2.73)$$

$$\text{or} \quad R_E = \frac{V_T}{\left( 1 + \frac{1}{\beta} \right) I_{C2}} \ln \frac{I_{C1}}{I_{C2}} \quad (2.74)$$

A relation between  $I_{C1}$  and the reference current  $I_{ref}$  is obtained by writing KCL at the collector point of  $Q_1$  (note 'a')

$$I_{ref} = I_{C1} + I_{B1} + I_{B2} \quad (2.75)$$

$$= I_{C1} \left( 1 + \frac{1}{\beta} \right) + \frac{I_{C2}}{\beta} \quad (2.76)$$

(Assuming  $\beta_2 = \beta_1 = \beta$  for identical transistors)

In the widlar current source  $I_{C2} \ll I_{C1}$ , therefore the term  $I_{C2}/\beta$  may be neglected in Eq. (2.76),

$$\text{Thus} \quad I_{ref} \cong I_{C1} \left( 1 + \frac{1}{\beta} \right) \quad (2.77)$$

$$\text{or} \quad I_{C1} = \frac{\beta}{\beta + 1} I_{ref} \quad (2.78)$$

$$\text{where} \quad I_{ref} = \frac{V_{CC} - V_{BE}}{R_1} \quad (2.79)$$

$$\text{For } \beta \gg 1, \quad I_{C1} \cong I_{ref} \quad (2.80)$$

The design and advantages of Widlar current source are illustrated in the following example:

### Example 2.7

Design a Widlar current source for generating a constant current  $I_0 = 10 \mu\text{A}$ . Assume  $V_{CC} = 10 \text{ V}$ ,  $V_{BE} = 0.7 \text{ V}$ ,  $\beta = 125$ . Use  $V_T = 25 \text{ mV}$ .

### Solution

For the Widlar current source of Fig. 2.18, we must first decide a suitable value for  $I_{ref}$ . If we choose  $I_{ref} = 1 \text{ mA}$ , then,  $R_1$  is given by

$$R_1 = \frac{10 \text{ V} - 0.7 \text{ V}}{1 \text{ mA}} = 9.3 \text{ k}\Omega$$

The value of  $R_E$  is determined from Eq. (2.74)

$$R_E = \frac{0.025}{\left( 1 + \frac{1}{125} \right) 10 \times 10^{-6}} \ln \left( \frac{1 \text{ mA}}{10 \mu\text{A}} \right) \\ = 11.5 \text{ k}\Omega$$

It is clearly seen that Widlar circuit allows the generation of small constant using relatively small resistors.

Sometimes, it is convenient to use emitter resistances in both the transistors  $Q_1$  and  $Q_2$  as shown in Fig. 2.19. If  $R_1 = R_2$  the currents  $I_{C1} = I_{C2}$ . The same circuit can also be used to provide different currents in  $Q_1$  and  $Q_2$ , as we shall now see.

### Analysis

Rewriting Eq. (2.64) as

$$V_{BE2} - V_{BE1} = V_T \ln \frac{I_{C2}}{I_{C1}} \quad (2.81)$$

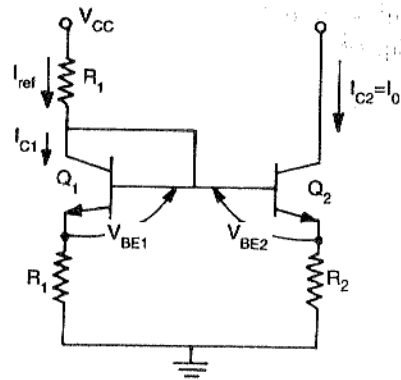


Fig. 2.19 A current mirror with magnification ( $I_{C2}/I_{C1} \cong R_1/R_2$ )

Writing KVL in the base-emitter loop

$$V_{BE2} - V_{BE1} = I_{C1}R_1 - I_{C2}R_2 \text{ (Neglecting base current)} \quad (2.82)$$

From Eq. (2.81) and Eq. (2.82),

$$I_{C1}R_1 - I_{C2}R_2 = V_T \ln \frac{I_{C2}}{I_{C1}} \quad (2.83)$$

$$\frac{I_{C2}}{I_{C1}} \frac{R_2}{R_1} = 1 - \frac{V_T}{I_{C1}R_1} \ln \frac{I_{C2}}{I_{C1}} \quad (2.84)$$

$$\frac{I_{C2}}{I_{C1}} = \frac{R_1}{R_2} \left( 1 - \frac{V_T}{I_{C1}R_1} \ln \frac{I_{C2}}{I_{C1}} \right) \quad (2.85)$$

For the range  $0.1 < \frac{I_{C2}}{I_{C1}} < 10$ , we can assume  $\frac{I_{C2}}{I_{C1}} \cong \frac{R_1}{R_2}$ . Thus even

large ratios  $\frac{I_{C2}}{I_{C1}}$  (say 10) is easily obtained by the modified circuit.

### Current Repeaters

The basic current mirror of Fig. 2.16 can be used to source current to more than one load. Such a circuit is called current repeater and is shown in Fig. 2.20. If all the transistors are identical, then the current

$$I_C = I_{C1} = \dots = I_{CN} \cong I_{ref}$$

It can be seen from Fig. 2.20 at node 'a'

$$I_{ref} = I_C + I_B + NI_B \text{ (Assuming identical transistors)} \quad (2.86)$$

$$= I_C + \frac{(1+N)}{\beta} I_C$$

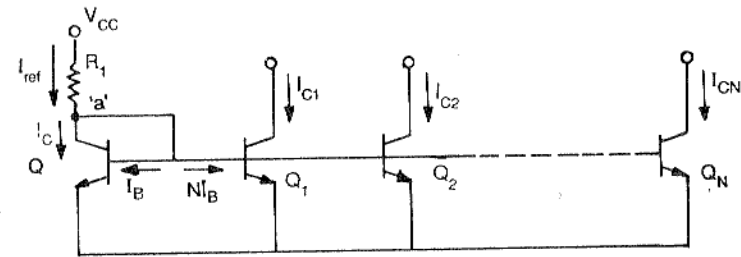


Fig. 2.20 A current repeater to source current to  $N$  transistors  $Q_1, Q_2, \dots, Q_N$

$$= I_C \left( 1 + \frac{(1+N)}{\beta} \right) \quad (2.87)$$

$$\text{Thus } I_C = I_{ref} \frac{\beta}{\beta + 1 + N} \quad (2.88)$$

It is possible to achieve different value of  $I_{C1}, I_{C2}, \dots, I_{CN}$  by scaling the emitter area of transistors  $Q_1, Q_2, \dots, Q_N$ . The same can also be achieved by using emitter resistance as it illustrated by the example that follows.

### Example 2.8

For the circuit shown in Fig. 2.21 determine  $I_{C1}, I_{C2}$ , and  $I_{C3}$ . Assume  $\beta = 125$

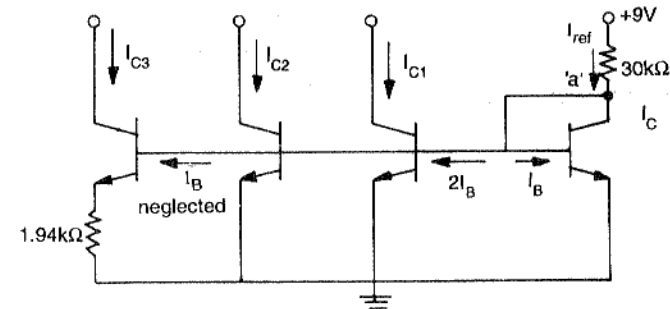


Fig. 2.21 Circuit for Example 2.8

### Solution

$$I_{ref} = \frac{9V - 0.7V}{30 \text{ k}\Omega} = 0.277 \text{ mA}$$

Also at node 'a'

$$I_{ref} = I_C + 3I_B \text{ (Assume } I_{B3} \text{ of Widlar source negligible)}$$

$$= I_C \left( 1 + \frac{3}{\beta} \right)$$

$$I_C = I_{\text{ref}} \left( \frac{\beta}{3 + \beta} \right)$$

Putting the values and solving, we get,

$$I_{C1} = I_{C2} = 0.271 \text{ mA}$$

Calculate  $I_{C3}$ , using Eq. (2.74) gives

$$1.94 = \frac{0.025}{I_{C3} \left( 1 + \frac{1}{125} \right)} \ln \frac{0.271}{I_{C3}}$$

Solving the transcendental equation by trial and error, we obtain

$$I_{C3} = 0.0287 \text{ mA}$$

### Improved current source circuits

A good current source must meet two requirements. The first is that the output current,  $I_0$  should not be dependent upon  $\beta$  and secondly the output resistance of the current source should be very high. The need for high output resistance current source can be seen because the common-mode gain of the differential amplifier (used as basic building block in op-amps) can only be reduced by using high resistance current sources. Also, all differential amplifiers invariably use current source as a load. Thus to obtain high voltage gain a large output resistance load is required. Now, we discuss two circuits that exhibit reduced dependence on  $\beta$  or increased output resistance.

### A current source with gain

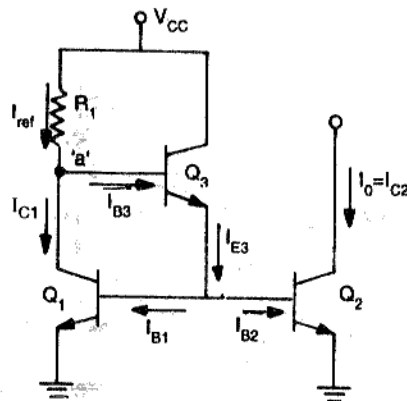


Fig. 2.22 A current source with gain

The circuit shown in Fig. 2.22 includes a transistor  $Q_3$  whose emitter current supplies the base currents of  $Q_1$  and  $Q_2$ . The expression for the source current  $I_0 = I_{C2}$  be derived by writing KCL at node 'a'

$$I_{\text{ref}} = I_{C1} + I_{B3}$$

$$= I_{C1} + \frac{I_{E3}}{1 + \beta}$$

$$= I_{C2} + \frac{I_{E3}}{1 + \beta} \quad (V_{BE1} = V_{BE2}; I_{C1} = I_{C2} = I_0) \quad (2.89)$$

$$\text{Also } I_{E3} = I_{B1} + I_{B2}$$

$$= 2I_B \quad (\text{since } Q_1 \text{ and } Q_2 \text{ are identical})$$

Thus,

$$I_{\text{ref}} = I_{C1} + \frac{2I_B}{1 + \beta} \quad (2.90)$$

$$= I_C + \frac{2I_C}{\beta(1 + \beta)}$$

$$= I_C \left( 1 + \frac{2}{\beta(1 + \beta)} \right)$$

$$\text{or } I_0 = I_C = I_{\text{ref}} \frac{\beta(1 + \beta)}{\beta^2 + \beta + 2} \quad (2.91)$$

It is easily seen from Eq. (2.91) that the output current is essentially independent of  $\beta$ . The output resistance of the current source is only  $r_0$ . It can however be increased by using emitter resistances in  $Q_1$  and  $Q_2$  as is done in the modified Widlar source circuit in Fig. 2.19. The two emitter resistors can also be used to make  $I_0$  different from  $I_{\text{ref}}$ .

### Wilson current source

The final current source shown in Fig. 2.23 provides an output current  $I_0$ , which is very nearly equal to  $I_{\text{ref}}$  and also exhibits a very high output resistance.

### Analysis

$$\text{Since } V_{BE1} = V_{BE2}$$

$$I_{C1} = I_{C2} \text{ and } I_{B1} = I_{B2} = I_B$$

At node 'b'

$$I_{E3} = 2I_B + I_{C2}$$

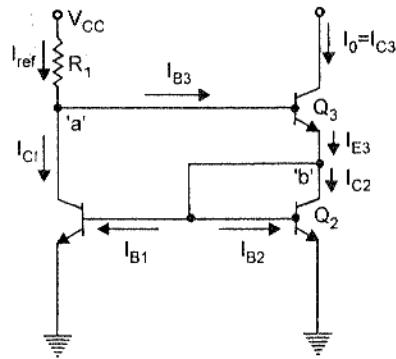


Fig. 2.23 A Wilson current source

$$= \left( \frac{2}{\beta} + 1 \right) I_{C2} \quad (2.92)$$

$I_{E3}$  is also equal to

$$\begin{aligned} I_{E3} &= I_{C3} + I_{B3} \\ &= I_{C3} \left( 1 + \frac{1}{\beta} \right) \end{aligned} \quad (2.93)$$

From Eqs. (2.92) and (2.93), we obtain

$$\begin{aligned} I_{C3} \left( 1 + \frac{1}{\beta} \right) &= I_{C2} \left( 1 + \frac{2}{\beta} \right) \\ I_{C3} &= I_0 = \left( \frac{\beta + 2}{\beta + 1} \right) I_{C2} \end{aligned} \quad (2.94)$$

Since  $I_{C1} = I_{C2}$

$$I_0 = \left( \frac{\beta + 2}{\beta + 1} \right) I_{C1} \quad (2.95)$$

At node 'a'

$$\begin{aligned} I_{ref} &= I_{C1} + I_{B3} \\ &= \frac{\beta + 1}{\beta + 2} I_0 + \frac{I_0}{\beta} \\ &= \frac{\beta^2 + 2\beta + 2}{\beta^2 + 2\beta} I_0 \end{aligned}$$

$$\text{or} \quad I_0 = \frac{\beta^2 + 2\beta}{\beta^2 + 2\beta + 2} I_{ref} \quad (2.96)$$

$$\text{where} \quad I_{ref} = \frac{V_{CC} - 2V_{BE}}{R_1} \quad (2.97)$$

$$\text{The difference } I_0 - I_{ref} = \frac{2}{\beta^2 + 2\beta + 2} I_{ref} \quad (2.98)$$

is extremely small error for modest values of  $\beta$ . The output resistance of a Wilson current mirror is substantially greater ( $\cong \beta \frac{r_0}{2}$ ) than simple current mirror or Widlar current mirror.

### More Solved Examples

#### Example 2.9

For the circuit shown in Fig. 2.24, determine the value of  $I_0$  for  $\beta = 100$ . Assume  $V_{BE} = 0.7$  V

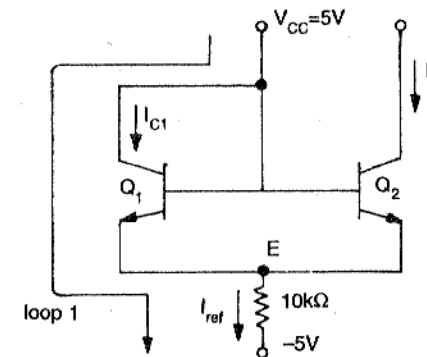


Fig. 2.24 Circuit for Example 2.9

#### Solution

Writing KVL for the indicated loop 1

$$5V - V_{BE} - 10 \text{ k}\Omega \times I_{ref} + 5V = 0$$

$$I_{ref} = \frac{10V - 0.7}{10 \text{ k}\Omega} = 0.93 \text{ mA}$$

At emitter node 'E'

$$\begin{aligned} I_{ref} &= 2I_E \quad (\text{Assuming identical transistors}) \\ &= 2(I_C + I_B) \\ &= 2I_C \left( 1 + \frac{1}{\beta} \right) \end{aligned}$$

Then 
$$I_C = \frac{\beta}{2(1+\beta)} I_{\text{ref}} = 0.46 \text{ mA}$$

Due to mirror effect  $I_0 = I_{C1} = I_C = 0.46 \text{ mA}$

### Example 2.10

For the circuit shown in Fig. 2.25.

- (a) Determine  $I_{C1}$  and  $I_{C2}$   
 (b) Find  $R_C$  so that  $V_0 = 6 \text{ V}$ . Assume  $\beta = 200$

### Solution

(a) 
$$I_{\text{ref}} = \frac{12 \text{ V} - 0.7 \text{ V}}{15 \text{ k}\Omega} = 0.75 \text{ mA}$$

and 
$$I_1 = \frac{0.7 \text{ V}}{2.8 \text{ k}\Omega} = 0.25 \text{ mA}$$

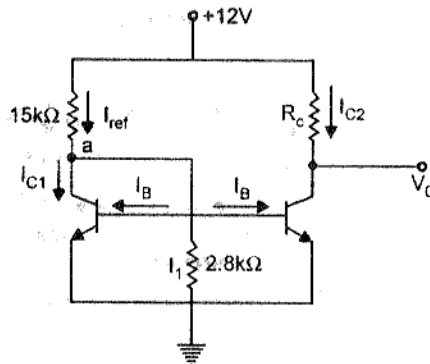


Fig. 2.25 Circuit for Example 2.10

At node 'a'

$$I_{\text{ref}} = I_{C1} + 2I_B + I_1$$

$$= I_{C1} \left( 1 + \frac{2}{\beta} \right) + I_1$$

Solving for  $I_{C1}$  gives

$$I_{C1} = 0.495 \text{ mA}$$

$$\approx 0.5 \text{ mA}$$

$$I_{C2} = I_{C1} \quad (\text{due to mirror effect})$$

(b) From the outer loop

$$12 \text{ V} = I_{C2} R_C + V_0$$

$$R_C = \frac{12 \text{ V} - 6 \text{ V}}{0.5 \text{ mA}} = 12 \text{ k}\Omega$$

### Example 2.11

Figure 2.26 shows a modified current mirror circuit. Determine the emitter current in transistor  $Q_3$  if  $\beta = 100$  and  $V_{BE} = 0.75 \text{ V}$ .

### Solution

From Fig. 2.26 at node 'a'

$$\begin{aligned} I &= I_{C1} + I_1 \\ &= I_{C1} + I_{B1} + I_1' \end{aligned}$$

or, 
$$I = I_{C1} \left( 1 + \frac{1}{\beta} \right) + I_1'$$

$$\approx I_{C1} + I_1' \quad (\text{as } \beta \gg 1)$$

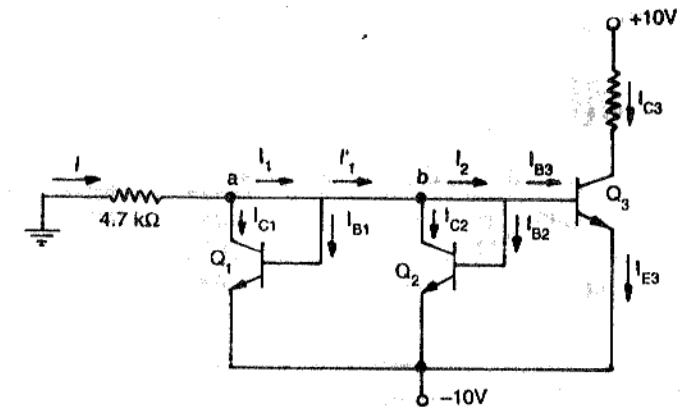


Fig. 2.26 Circuit of Example 2.11

Also at node 'b'

$$\begin{aligned} I_1' &= I_{C2} + I_2 \\ &= I_{C2} + I_{B2} + I_{B3} \end{aligned}$$

$$= I_{C2} \left( 1 + \frac{1}{\beta} \right) + I_{B3}$$

$$\approx I_{C2} + I_{B3}$$

Putting the value of  $I_1'$ , we get

$$\begin{aligned} I &= I_{C1} + I_{C2} + I_{B3} \\ &= 2I_C + I_{B3} \quad [\text{as } I_{C1} = I_{C2} = I_C] \end{aligned}$$

$$\approx I_C \left( 2 + \frac{1}{\beta} \right) \approx 2I_C$$

The current  $I$  is given by,

$$I = \frac{10 - 0.75}{4.7 \text{ k}\Omega} = \frac{9.25}{4.7 \text{ k}\Omega} = 1.97 \text{ mA}$$

The collector current of  $Q_3$  is equal to the collector current of  $Q_1$  and  $Q_2$  due to mirror action. Therefore, the emitter current

$$I_{E3} \approx I_{C3} = I_C = \frac{I}{2} = 0.98 \text{ mA}$$

#### 2.4.5 Input Resistance

The resistance offered by the differential amplifier of Fig. 2.27 to the differential input signal ( $v_1 - v_2$ ) is called differential input resistance  $R_{id}$ . The emitters of  $Q_1$  and  $Q_2$  are floating as  $R_E$  is replaced by a constant current source, therefore  $R_{id} \approx h_{ie1} + h_{ie2} = 2 h_{ie}$ . If input 2 is grounded, then input 1 is loaded by  $2 h_{ie}$ . The value of  $h_{ie}$  can be increased by reducing the biasing currents for  $Q_1$  and  $Q_2$  and input resistance of the order of 500 k $\Omega$  can be obtained.

Higher values of input resistance can be obtained by using a Darlington pair in place of transistor  $Q_1$  and  $Q_2$  of Fig. 2.27 as shown in Fig. 2.28. One drawback of the Darlington differential amplifier is the higher offset voltage  $V_{os}$ , (due to cascaded stages) which is about 2 times larger than the ordinary two transistor differential amplifier.

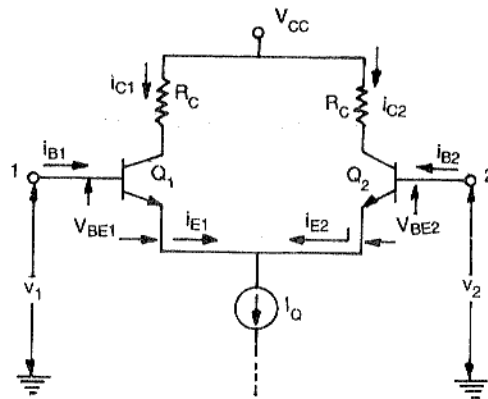


Fig. 2.27 Differential amplifier

The most important feature of the Darlington pair differential amplifier is its extraordinary large current gain. For the circuit shown in Fig. 2.28, the overall current gain is

$$\begin{aligned} \beta &= \frac{I_C}{I_{B1}} = \frac{I_{C1} + I_{C2}}{I_{B1}} \\ &= \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B1}} \end{aligned}$$

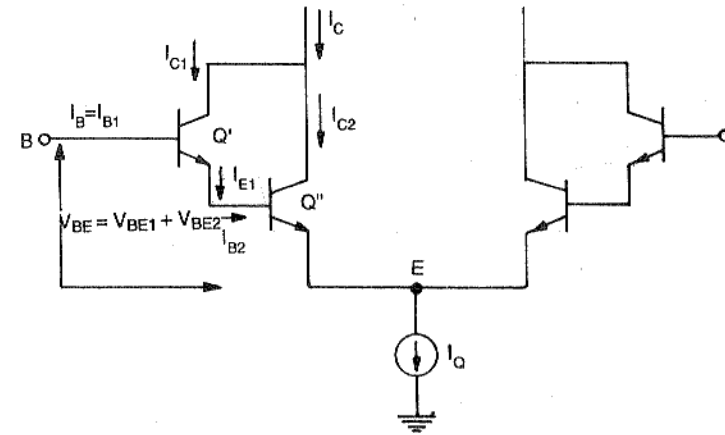


Fig. 2.28 Differential amplifier using Darlington pair

$$\begin{aligned} &= \frac{I_{C1}}{I_{B1}} + \frac{I_{C2}}{I_{B2}} \times \frac{I_{B2}}{I_{B1}} \\ &= \beta_1 + \beta_2 (\beta_1 + 1) \left[ \begin{array}{l} I_{B2} = I_{E1} \\ = I_{C1} + I_{B1} \end{array} \right] \\ &\approx \beta_2 \beta_1 \end{aligned}$$

So, the overall current gain  $\beta$  of the Darlington circuit will be of the order of 10,000 if the current gain of the individual transistor is about 100. Another method to get higher input resistance is to fabricate a FET differential pair as the input stage with the rest of the stages made of BJTs. Input resistance of the order of  $10^{12} \Omega$  is possible with such JFET inputs. A number of such op-amps are described in Sec. 2.6.

#### 2.4.6 Active Load

The open circuit voltage gain of an op-amp should be as large as possible and this is achieved by cascading gain stages. However, this increases the phase shift too and amplifier becomes more susceptible to breaking out into oscillations. One can think of increasing gain by using large collector resistance values as gain is proportional to load resistor  $R_C$ . However, there are limitations to the maximum value of  $R_C$  to be used due to the following two reasons:

- (i) A large value of resistance requires a large chip area.
- (ii) For large  $R_C$  quiescent drop across it increases and hence a large power supply will be required to maintain a given quiescent collector current. These difficulties are circumvented by using a current source of the type shown in Fig. 2.16 as load in the place of  $R_C$ .

The current mirror discussed earlier has a dc resistance of the order of few kilohms, as the quiescent voltage across it is a fraction of the supply voltage and the current is in milliamperes. However, since it acts as a constant current source, its dynamic resistance (ac) is very high. Hence, a current mirror can also be used as an active load for an amplifier to obtain a very large voltage gain. Figure 2.29 (a) shows a diff-amp with an active load. The current mirror uses *pnp* transistors  $Q_3$  and  $Q_4$ . The constant current  $I_Q$  may also be obtained from a current mirror. The operation of the circuit in Fig. 2.29 (a) is as follows:

Under the quiescent conditions,  $v_1 = v_2 = 0$ . From symmetry of  $Q_1$  and  $Q_2$ ,  $I_1 = I_2 = I_Q/2$  where base currents are assumed to be neglected. Since  $Q_3$  and  $Q_4$  form a current mirror,  $I = I_1 = I_2$ . The load current  $I_L$  entering the next stage is

$$I_L = I - I_2 = 0 \quad (2.99)$$

However, when  $v_1$  is increased over  $v_2$ ,  $I_1$  increases whereas  $I_2$  decreases, since  $I_1 + I_2 = I_Q$  (constant). Also the current  $I$  always remains equal to  $I_1$  due to the current mirror. The load current is given by

$$\begin{aligned} I_L &= I - I_2 = I_1 - I_2 \\ &= g_m v_1 - g_m v_2 \\ &= g_m (v_1 - v_2) \\ &= g_m v_d \end{aligned} \quad (2.100)$$

The circuit thus behaves as a transconductance amplifier.

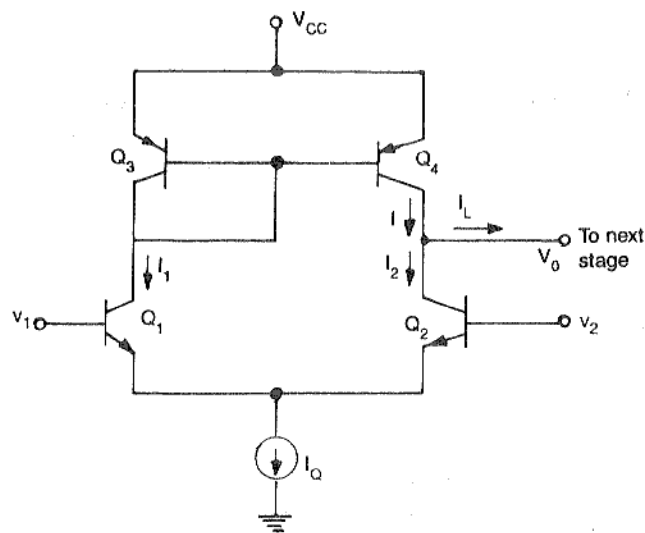


Fig. 2.29 (a) A differential amplifier with an active load  $Q_3$ - $Q_4$ .

A popular op-amp ( $\mu A 741$ ) by Fairchild uses an alternate active load as shown in Fig. 2.29 (b). The transistors  $Q_1$ - $Q_3$  and  $Q_2$ - $Q_4$  are in cascode configuration (*CE-CB*) with input signal as  $v_1$  ( $v_2$ ). The transistors  $Q_5$ ,  $Q_6$  and  $Q_7$  form the active load of the type shown in Fig. 2.22. The transistors  $Q_8$  and  $Q_9$  form the current mirror to provide the constant current  $I_Q$  required for high CMRR of the diff-amp. If base currents are neglected, then  $I_Q \approx I_3$ . The arrangement  $Q_{10}$  and  $Q_{11}$  is another current mirror where  $I_3 \ll I_4$  due to  $5 \text{ k}\Omega$  emitter resistor. Consequently  $I_Q = I_3$  is small (of the order of  $\mu A$ ) giving a very high input resistance.

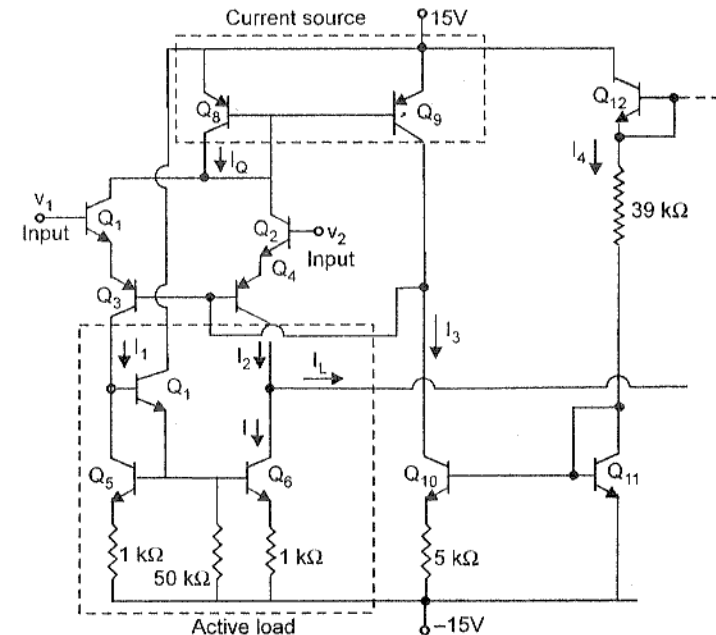


Fig. 2.29 (b) Active load ( $Q_5$ - $Q_6$ - $Q_7$ ) of a low current differential amplifier  $\mu A 741$

Under the quiescent conditions,  $I_1 = I_2 = I_Q/2$ . Since  $I$  is always equal to  $I_1$ , the load current  $I_L = I_2 - I = I_2 - I_1 = 0$ . Now if  $v_1$  is increased and  $v_2$  is decreased,  $I_1$  rises and  $I_2$  falls from the quiescent value of  $I_Q/2$ . With this excitation,  $I_L = I_2 - I_1$  changes from zero to a negative value. Thus the circuit behaves as a transconductance amplifier because  $I_L$  is proportional to  $v_1 - v_2$ .

#### 2.4.7 Level Translator

There are two good reasons for using a level shifter in an IC op-amp. As we want an op-amp to operate down to dc, no coupling capacitor is used. Because of direct coupling, the dc level rises from stage to stage. The increase in dc level tends to shift the operating point of the

next stage. This, in turn, limits the output voltage swing and may even distort the output signal. It, therefore, becomes essential that the quiescent voltage of one stage is shifted before it is applied to the next stage. Another requirement to be satisfied is that the output should have quiescent voltage level of 0V for zero input signal.

The simplest type of a level shifter is shown in Fig. 2.30 (a). It may be noted that this is basically an emitter follower. Hence the level shifter also acts as a buffer to isolate the high gain stages from the output stage. The amount of shift obtained is

$$V_o - V_i = -V_{BE} \approx -0.7 \text{ V} \quad (2.101)$$

If this shift is insufficient, the output can be taken at the junction of two resistors  $R_1$  and  $R_2$ , as shown in Fig. 2.30 (b). The voltage shift is now increased by the drop across  $R_1$ . However, this arrangement has the disadvantage that signal voltage also gets attenuated by  $R_2/(R_1 + R_2)$ . This can be easily circumvented if  $R_2$  is replaced by a current mirror  $I$  as shown in Fig. 2.30 (c). The shift in level now is

$$V_o - V_i = -(V_{BE} + IR_1) \quad (2.102)$$

and there is no ac attenuation due to high resistance of the current source.

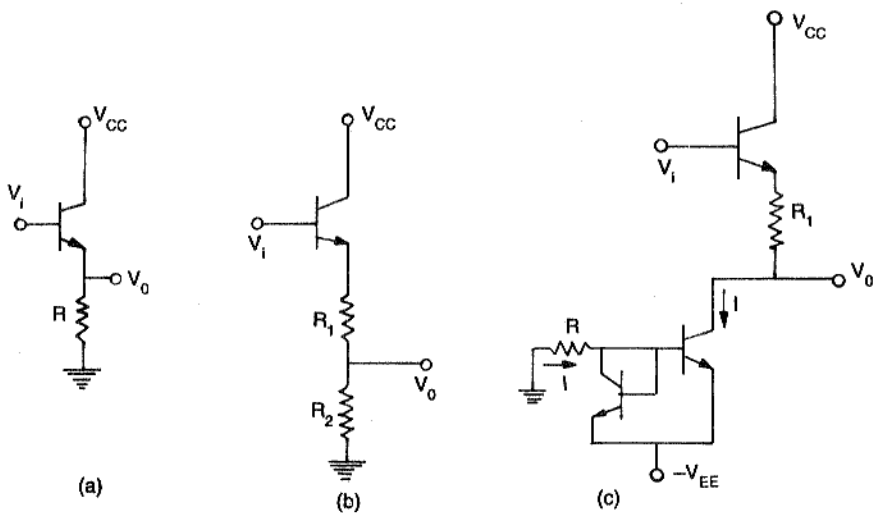


Fig. 2.30 (a)-(c) Level shifters using emitter follower buffer

Another voltage source commonly used in  $\mu A741$  op-amp is shown in Fig. 2.30 (d). It can be seen that if base current is negligible compared to the current in  $R_3$  and  $R_4$ , then the circuit behaves as a  $V_{BE}$  multiplier as,

$$V = \frac{V_{BE}}{R_4} (R_3 + R_4) = V_{BE} \left( 1 + \frac{R_3}{R_4} \right)$$

This voltage source can also be used to replace  $R_1$  in Fig. 2.30 (b).

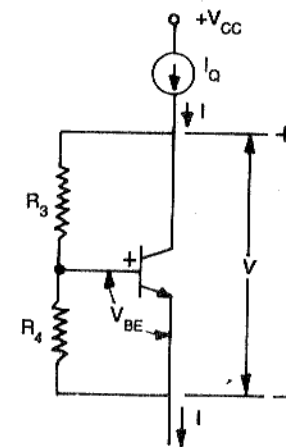


Fig. 2.30 (d) A voltage source  $V$  which is a multiple of  $V_{BE}$

**Example 2.12**

Calculate  $V_1 - V_2$  for the level shifter shown in Fig. 2.31. Assume identical silicon transistors with  $V_{BE} = 0.7 \text{ V}$  and very large values of  $\beta$ .

**Solution**

Transistors  $Q_1$  and  $Q_2$  form a current mirror.

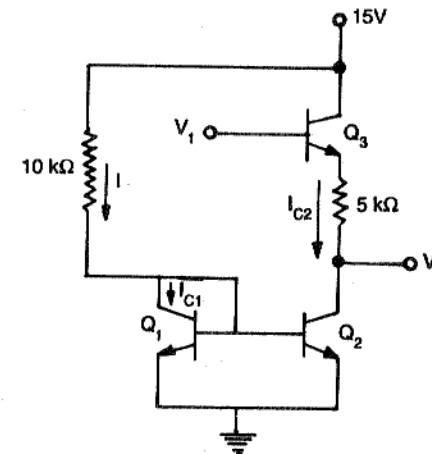


Fig. 2.31 Circuit of Example 2.12

So,

$$I_{C1} = I_{C2} = I$$

and

$$I = \frac{15 - 0.7}{10 \text{ k}\Omega} = 1.43 \text{ mA}$$



$$V_1 - V_2 = V_{BE3} + I_{C2} \times 5 \text{ k}\Omega$$

$$= 0.7\text{V} + 1.43 \times 5 \text{ k}\Omega = 7.85 \text{ V.}$$

2.4.8 Output Stage

The function of the last stage, that is, the output stage in an op-amp is to supply the load current and provide a low impedance output. A simple output stage is an emitter follower with complementary transistors as shown in Fig. 2.32 (a). It can be seen that for  $v_i$  positive, transistor  $Q_1$  is *on* and supplies current to load  $R_L$ . And, if  $v_i$  is negative,  $Q_1$  is cut off and  $Q_2$  acts as a sink to remove current from the load  $R_L$ . There is, however, a limitation in this circuit. The output voltage  $v_o$  remains zero until the input  $v_i$  exceeds  $V_{BE}$  (cut in) = 0.5 V. This is called cross-over distortion. It can be eliminated by applying a bias voltage  $V$  slightly greater than  $2 V_{BE(\text{cut in})} = 1 \text{ V}$  between the two bases, so that a small current flows in the transistors even in the quiescent state.

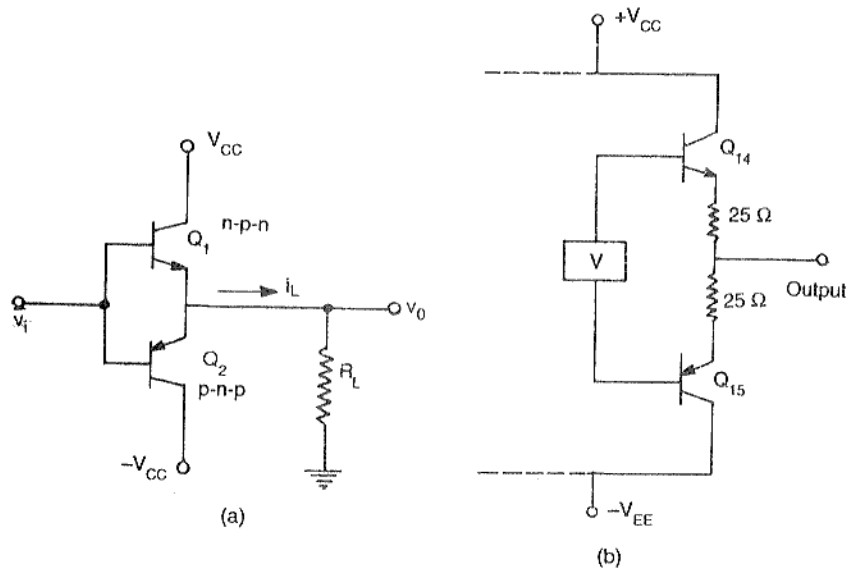


Fig. 2.32 (a) A complementary emitter follower output stage  
(b) Output stage of  $\mu\text{A} 741$

The output stage of  $\mu\text{A} 741$  op-amp is shown in Fig. 2.32 (b). The block marked  $V$  is the  $V_{BE}$  multiplier of the type shown in Fig. 2.30 (d). It is designed to supply a voltage of about 1 V between the bases of the complementary pair of transistors  $Q_{14}$  and  $Q_{15}$ . The small emitter resistors (25 $\Omega$ ) stabilize the quiescent base current.

2.5 EXAMPLES OF IC OP-AMPS

We are now in a position to analyse the complete circuit of commercially available op-amps. Two such IC op-amps discussed are Motorola MC 1530 and Fairchild  $\mu\text{A}741$ .

2.5.1 Motorola MC1530 Op-Amp

The circuit of MC 1530 is shown in Fig. 2.33. It is easily seen that the circuit consists of four stages. Transistors  $Q_2$  and  $Q_3$  form the first diff-amp stage driven by the constant current source  $Q_1$ . The output of the first diff-amp drives the second diff-amp formed by  $Q_4$  and  $Q_5$ . The single ended output of the second diff-amp drives the level shifter  $Q_6$  (emitter follower).  $Q_7$  and diode  $D_3$  forms another constant current source of the type shown in Fig. 2.15. The diode connected transistor  $Q_1$  of Fig. 2.15 is shown by diode  $D_3$  here. The output stage of MC1530 uses  $Q_8$ ,  $Q_9$  and  $Q_{10}$  where  $Q_9$  and  $Q_{10}$  are in totem-pole configuration

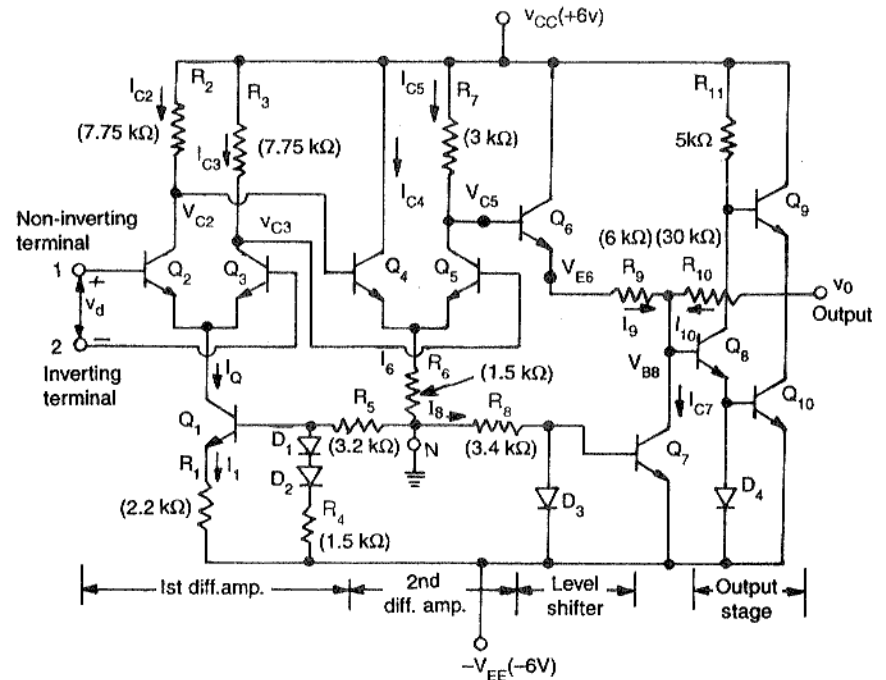


Fig. 2.33 Internal circuit of Motorola MC 1530

Example 2.13

From the circuit of Fig. 2.33 calculate,

- (1) The collector current in each transistor and the output voltage under quiescent conditions.

(2) The open loop voltage gain.

Assume  $h_{fe} = 100$  and  $V_{BE} = V_D = 0.7\text{ V}$

(1) The d.c. analysis is performed by assuming that both the inverting and non-inverting terminals are at ground potential. To determine the collector current in  $Q_2$  and  $Q_3$ , first calculate the constant current  $I_Q$ . If the base current of  $Q_1$  is neglected, then  $I_Q = I_1$ . The voltage  $V_{BN1}$  at the base of transistor  $Q_1$  with respect to ground  $N$  is written using voltage divider rule as,

$$\begin{aligned} V_{BN1} &= \frac{[-V_{EE} + V_D + V_D] R_5}{R_4 + R_5} \\ &= \frac{(-6\text{V} + 1.4\text{V})(3.2\text{ k}\Omega)}{1.5\text{ k}\Omega + 3.2\text{ k}\Omega} = -3.13\text{ V} \end{aligned}$$

$$\begin{aligned} I_1 &= \frac{V_{EE} + V_{BN1} - V_{BE1}}{R_1} \\ &= \frac{6\text{V} - 3.13\text{V} - 0.7\text{V}}{2.2\text{ k}\Omega} = 0.986\text{ mA} \end{aligned}$$

So  $I_Q = 0.986\text{ mA}$

Under dc conditions, half of the  $I_Q$  flows through each of transistors  $Q_2$  and  $Q_3$ . Therefore,  $I_{C2} = I_{C3} = I_{Q2} = 0.493\text{ mA}$ . The voltage at the collector of  $Q_2$  and  $Q_3$  is,

$$\begin{aligned} V_{C2} = V_{C3} &= V_{CC} - R_2 I_{C2} \\ &= 6\text{V} - (7.75\text{ k}\Omega)(0.493\text{ mA}) = 2.18\text{ V} \end{aligned}$$

So the voltage at the base of  $Q_4$  and  $Q_5$  is 2.18 V. The dc voltage at the emitter of  $Q_4$  is,

$$V_{E4} = V_{C2} - V_{BE4} = 2.18\text{V} - 0.7\text{V} = 1.48\text{ V}$$

So,  $I_6 = \frac{V_{E4}}{R_6} = \frac{1.48\text{V}}{1.5\text{ k}\Omega} = 0.987\text{ mA}$

This current divides equally in transistors  $Q_4$  and  $Q_5$ , so that

$$I_{C4} = I_{C5} = \frac{I_6}{2} = 0.494\text{ mA}$$

$$\begin{aligned} V_{C5} &= V_{CC} - I_{C5} R_7 \\ &= 6\text{V} - (0.494\text{ mA})(3\text{ k}\Omega) = 4.52\text{ V} \end{aligned}$$

$$\begin{aligned} V_{E6} &= V_{C5} - V_{BE6} \\ &= 4.52\text{V} - 0.7\text{V} = 3.82\text{ V} \end{aligned}$$

Transistor  $Q_7$  alongwith diode  $D_3$  forms a current mirror of the type shown in Fig. 2.15. Hence,

$$I_{C7} = I_8 = \frac{V_{EE} - V_{D3}}{3.4} = 1.56\text{ mA}$$

To calculate the current  $I_9$ , first calculate the voltage at the base of  $Q_8$ ,

$$\begin{aligned} V_{B8} &= V_{BE8} + V_{D4} - V_{EE} \\ &= 0.7\text{V} + 0.7\text{V} - 6\text{V} = -4.60\text{ V} \end{aligned}$$

$$\begin{aligned} I_9 &= \frac{V_{E6} - V_{B8}}{R_9} = \frac{3.82\text{V} + 4.6\text{V}}{6\text{ k}\Omega} \\ &= 1.40\text{ mA} \end{aligned}$$

$$I_{10} = I_{C7} - I_9 = 1.56\text{ mA} - 1.40\text{ mA} = 0.16\text{ mA}$$

The voltage  $V_o$  at the output terminal is,

$$\begin{aligned} V_o &= I_{10} R_{10} + V_{B8} \\ &= (0.16\text{ mA})(30\text{ k}\Omega) - 4.60\text{V} = 0.20\text{ V} \\ &\approx 0\text{ V (as expected)} \end{aligned}$$

(2) In order to calculate the overall voltage gain, we first calculate the voltage gain of the differential amplifier stages. For this we must know the ac emitter resistance  $h_{ie}$  of the transistor used.

$$h_{ie} = \frac{h_{fe} V_T}{|I_C|}$$

where  $V_T$  is the volt equivalent of temperature = 26 mV at room temperature.

Since  $I_{C2} = I_{C3} = I_{C4} = I_{C5} \approx 0.5\text{ mA}$

So  $h_{ie} = \frac{(100)(26\text{ mV})}{0.5\text{ mA}} = 5.2\text{ k}\Omega$

Since emitter of  $Q_4 - Q_5$  is at ground potential under ac operation the input resistance  $h_{ie}$  of  $Q_4$  and  $Q_5$  is effectively in parallel to collector circuit load ( $R_2$  and  $R_3$ ) of first diff-amp. The effective load of  $Q_2$  and  $Q_3$  is

$$\begin{aligned} R_{L2} = R_{L3} &= 7.75\text{ k}\Omega \parallel 5.2\text{ k}\Omega \\ &= 3.12\text{ k}\Omega \end{aligned}$$

The output of the first stage is double ended, its differential gain is given by Eq. (2.53) as

So, 
$$A_{V1} = \frac{(v_{C3} - v_{C2})}{v_d} = \frac{h_{fe} R_{1,2}}{h_{ie}} = \frac{100 \times 3.12 \text{ k}\Omega}{5.2 \text{ k}\Omega} = 60$$

For the second stage,  $h_{fe} = 100$ ,  $h_{ie} = 5.2 \text{ k}\Omega$  and load  $R_7 = 3 \text{ k}\Omega$  (neglecting loading on  $Q_5$  of the emitter follower  $Q_6$ ). The output of the second stage is single ended, so its differential gain is,

$$A_{V2} = \frac{v_{C5}}{v_{C3}} = -\frac{1}{2} \frac{h_{fe} R_7}{h_{ie}} = -\frac{100 \times 3 \text{ k}\Omega}{2 \times 5.2 \text{ k}\Omega} = -28.9$$

The third stage is the emitter follower, so,  $A_{V3} \approx 1$   
 The last output stage uses voltage shunt feedback network  $R_9 - R_{10}$ ,

so 
$$A_{V4} \approx \frac{R_{10}}{R_9} = -\frac{30}{6} = -5$$

Hence the overall op-amp gain is,  

$$A_v = (60) (-28.9) (-5) = 8670$$

**2.5.2 741 Op-Amp**

741 op-amp has become an industry standard today. The pin configuration and the complete schematic circuit diagram for 741 is shown in Fig. 2.34 (a) and (b) respectively. Since this circuit is quite complex compared to MC1530, only the qualitative analysis is taken up.

In understanding an op-amp circuit as complex as this (20 transistors), first we identify the stages which provide signal gain. The input stage diff-amp consists of transistors  $Q_1 - Q_3$  and  $Q_2 - Q_4$ . Transistors  $Q_{16}$  and  $Q_{17}$  provide the second stage voltage gain. Transistors  $Q_1 Q_3$  and  $Q_2 Q_4$  are in cascode (CE-CB) configuration. Two transistors in series ( $Q_1$  feeds  $Q_3$ ) provide high gain per stage needed to achieve the adequate open-loop gain in a two stage amplifier. The transistors  $Q_5, Q_6$  and  $Q_7$  form the active load for  $Q_3$  and  $Q_4$ . Transistors  $Q_5$  and  $Q_6$  also function as a differential amplifier for the external offset nulling signal. The emitter current of transistors  $Q_5$  and  $Q_6$  can be

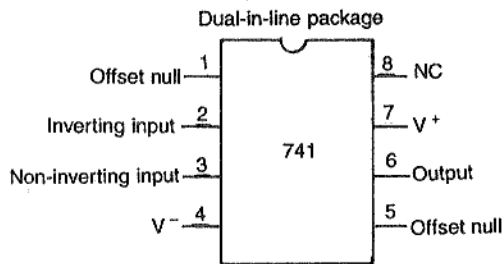


Fig. 2.34 (a) Pin configuration

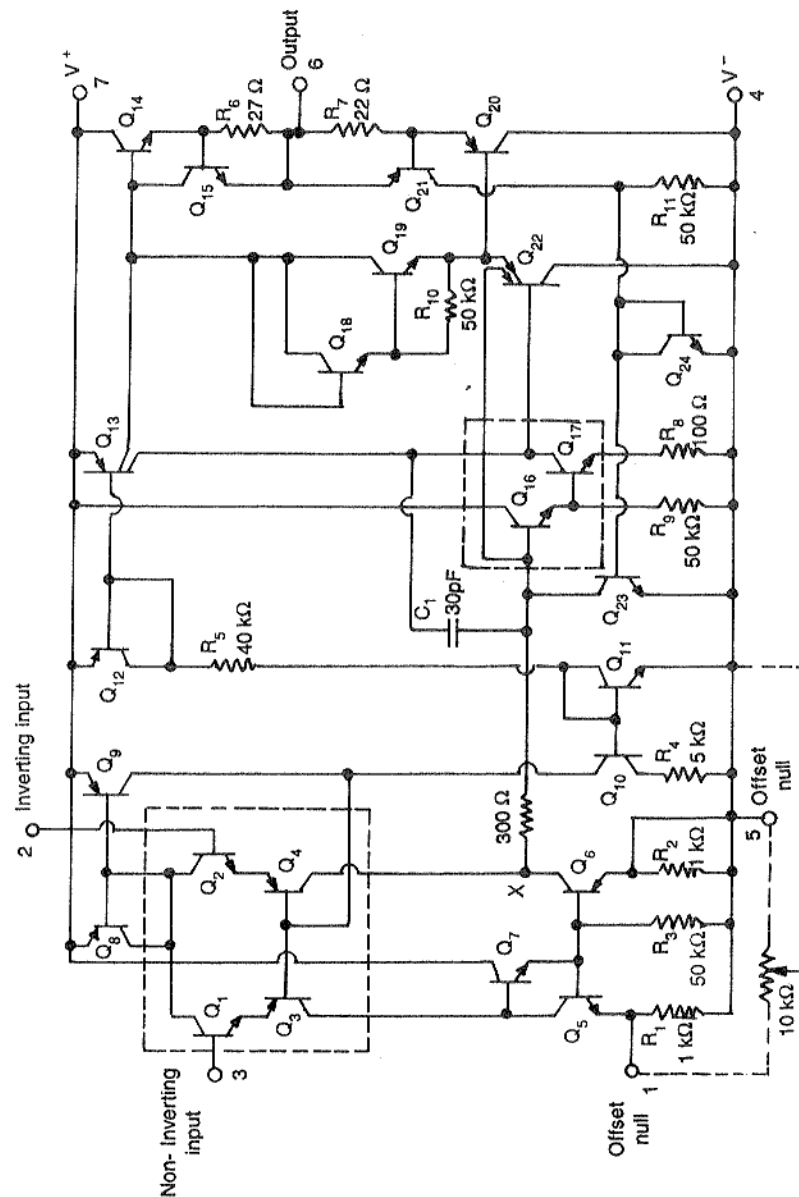


Fig. 2.34 (b) Schematic circuit diagram for 741 op-amp

controlled by varying a 10 kΩ potentiometer that is externally connected between offset null terminals as shown by dotted line in Fig. 2.34(b). Bias currents for the input stage are provided by a complicated arrangement of current mirror pairs.  $Q_{12}$  generates a current in  $Q_{11}$ . This current is reflected over to  $Q_{10}$  (though reduced because of the emitter feedback due to  $R_4$ ). This, in turn, generates a series current in  $Q_9$  which is reflected across another mirror pair to  $Q_8$ . The bias current of  $Q_3$  and  $Q_4$  is effectively driven by the mirror pair  $Q_{10}$  and  $Q_{11}$ . The output of the first diff-amp is taken at the junction of  $Q_4$  and  $Q_6$  (point X) which acts as a complementary symmetry amplifier. The output at this point is proportional to the differential input signal. The output is now amplified by the second stage consisting of transistor  $Q_{16}$  and  $Q_{17}$  in Darlington connection.

The output of common-collector-amplifier formed by  $Q_{16}$  and  $R_9$  drives the CE-amplifier composed of  $Q_{17}$ ,  $R_8$  and a constant current load  $Q_{13}$ . The output of CE-amplifier is a bias source for transistors  $Q_{18}$  and  $Q_{19}$ . Transistors  $Q_{12}$  and  $Q_{13}$  form a current mirror and supply current to transistors  $Q_{17}$ ,  $Q_{18}$  and  $Q_{19}$ . The network consisting of transistors  $Q_{18}$ ,  $Q_{19}$  and  $R_{10}$  is a fixed voltage level shifter shifting the voltage output of  $Q_{17}$  by a fixed amount on its way to the output complementary stage formed by  $Q_{14}$  and  $Q_{20}$ . The level shifter network is designed to bias the output stage in the linear region. The transistors  $Q_{18}$  and  $Q_{19}$  also separate the bases of  $Q_{14}$  and  $Q_{20}$  by two diode drops and thus temperature compensate currents in  $Q_{14}$  and  $Q_{20}$ . Transistor  $Q_{22}$  performs two functions. It serves as a buffer between  $Q_{17}$  and  $Q_{20}$  and also provides a negative feedback to  $Q_{16}$ . The final output is taken at the junction of  $R_6$  and  $R_7$ . The output complementary pair operates so that depending upon the sign of the output, only one of the transistors  $Q_{14}$  or  $Q_{20}$  is conducting at any time. With no input signal, both devices are turned off, resulting in a low quiescent current drain in the output stage.

Transistors  $Q_{15}$ ,  $Q_{21}$  and  $Q_{23}$  protect the circuit by limiting current to the output complementary stage. If the output (load) current exceeds the safe limit, the voltage drop across  $R_6$  and  $R_7$  increases. This turns on  $Q_{15}$  and  $Q_{21}$  which in turn makes  $Q_{23}$  on. This however shorts out, that is turns off the amplifier  $Q_{16}$ – $Q_{17}$ . This reduces the emitter current in  $Q_{22}$  and in turn current in  $Q_{18}$  and  $Q_{19}$ . The reduction in the currents of  $Q_{18}$  and  $Q_{19}$  lowers the currents in  $Q_{14}$  and  $Q_{20}$ . The diode-connected transistor  $Q_{24}$  is a temperature compensating diode for transistor  $Q_{23}$ . Finally the internal 30-pF capacitor provides the high frequency roll-off to stabilize the circuit.

### Example 2.14

For the op-amp circuit shown in Fig. 2.35

- (1) Perform the dc analysis. Assume  $\beta = 100$ ,  $V_{BE} = 0.7V$ . Note that the transistor  $Q_7$  has four times the areas of transistors  $Q_3$  and  $Q_4$ .
- (2) Compute the overall voltage gain.

### Solution

It can be seen that the circuit has the following four stages:

- Dual-input, differential-output
  - Dual-input, single-ended output
  - Level translator
  - Emitter follower
- (1) For dc analysis, assume that the input terminals are shorted to ground.

The reference current  $I$  of the current mirror  $Q_3$ – $Q_4$  is obtained as

$$I = \frac{V_{EE} - V_{BE3}}{R}$$

$$= \frac{15V - 0.7V}{28.6 \text{ k}\Omega} = 0.5 \text{ mA}$$

Due to current mirror action,

$$I_{CQ4} = I = 0.5 \text{ mA}$$

and  $I_{CQ1} = I_{CQ2} = I_{CQ4}/2 = 0.25 \text{ mA}$

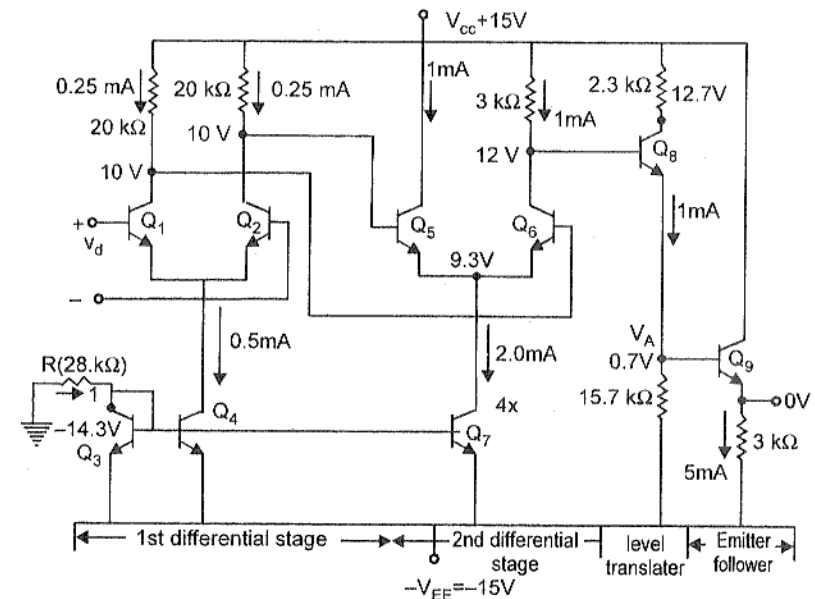


Fig. 2.35 Circuit for Example 2.14

Thus, each of  $Q_1$  and  $Q_2$  are biased at 0.25 mA. The collector voltages for  $Q_1$  and  $Q_2$  are

$$V_{CQ1} = V_{CQ2} = V_{CC} - I_{C1}R_{C1}$$

$$= 15V - 0.25 \text{ mA} \times 20 \text{ k}\Omega$$

$$= +10V$$

Now, proceeding to the next differential stage, voltage at the emitter of  $Q_5$  and  $Q_6$  will be

$$\begin{aligned} V_{EQ5} &= V_{EQ6} = 10 \text{ V} - 0.7 \text{ V} \\ &= 9.3 \text{ V} \end{aligned}$$

The differential pair  $Q_5 - Q_6$  is biased by the current mirror transistor  $Q_7$ . Since the area of  $Q_7$  is 4 times that of  $Q_3$  and  $Q_4$ , the transistor  $Q_7$  supplies a current  $4 \times 0.5 = 2 \text{ mA}$ .

Thus, collector currents of  $Q_5$  and  $Q_6$  are

$$I_{CQ5} = I_{CQ6} = \frac{I_{CQ7}}{2} = 1 \text{ mA}$$

Hence, collector voltage of  $Q_6$  is

$$\begin{aligned} V_{CQ6} &= V_{CC} - I_{CQ6} R_{C6} \\ &= 15 \text{ V} - 1 \text{ mA} \times 3 \text{ k}\Omega \\ &= 12 \text{ V} \end{aligned}$$

This causes a voltage at the emitter of *pnp* transistor  $Q_8$  at

$$V_{EQ8} = 12.7 \text{ V}$$

The emitter current of  $Q_8$  is

$$I_{EQ8} = \frac{15 \text{ V} - 12.7 \text{ V}}{2.3 \text{ k}\Omega} = 1 \text{ mA}$$

The voltage  $V_A$  at the collector of  $Q_8$  or the base of  $Q_9$  is

$$\begin{aligned} V_A &= -15 \text{ V} + 1 \text{ mA} \times 15.7 \text{ k}\Omega \\ &= 0.7 \text{ V} \end{aligned}$$

Since the emitter of  $Q_9$  will be 0.7 V below the base terminal, the voltage at the output terminal 6 is 0 V as is expected. The emitter current of  $Q_9$  is

$$\begin{aligned} I_{EQ9} &= [0 - (-15 \text{ V})] / 3 \text{ k}\Omega \\ &= 5 \text{ mA} \end{aligned}$$

- (2) A.C. Analysis. The ac emitter resistance of the transistor  $Q_1 - Q_2$  is

$$h_{ie} \text{ (} Q_1 - Q_2 \text{)} = \frac{h_{ie} V_T}{|I_C|} = \frac{100 \times 25 \text{ mV}}{2.5 \text{ mA}} = 10 \text{ k}\Omega$$

The ac emitter resistance of transistor  $Q_5 - Q_6$  is

$$h_{ie} \text{ (} Q_5 - Q_6 \text{)} = \frac{100 \times 25 \text{ mV}}{1 \text{ mA}} = 2.5 \text{ k}\Omega$$

Since emitter of ( $Q_5 - Q_6$ ) is at ground potential under ac conditions, the effective load for  $Q_1 - Q_2$  is

$$\begin{aligned} R_{L1} &= R_{L2} = 20 \text{ k}\Omega \parallel 2.5 \text{ k}\Omega \\ &= 2.2 \text{ k}\Omega \end{aligned}$$

Voltage gain of the first differential stage is

$$A_{DM1} = \frac{h_{fe} R_{L2}}{h_{ie}} = \frac{100 \times 2.2 \text{ k}\Omega}{10 \text{ k}\Omega} = 22$$

Voltage gain of second stage which is differential input, single-ended is

$$A_{DM2} = -\frac{1}{2} \frac{h_{fe} R_{L6}}{h_{ie}}$$

Assuming no loading effect on this stage due to level translator stage,

$$A_{DM2} = -\frac{1}{2} \times \frac{100 \times 3 \text{ k}\Omega}{2.5 \text{ k}\Omega} = -60$$

The gain of the level translator stage is

$$A_3 \cong -\frac{R_L}{R_E} = -\frac{15.7 \text{ k}\Omega}{2.3 \text{ k}\Omega} = -6.82$$

The last stage is emitter follower, so its voltage gain  $A_{V4} \cong 1$

So the overall voltage gain is

$$\begin{aligned} A_V &= (22) (-60) (-6.82) (1) \\ &= 9002 \end{aligned}$$

## 2.6 FET OPERATIONAL AMPLIFIER

The op-amp circuits discussed so far are bipolar op-amps. Op-amps using field transistors (FETs) in the input stage offer some very significant advantages over bipolar op-amps, especially in areas as input impedance, input bias and offset currents and slewing rate as shown in Table 2.1.

Table 2.1

Parameter	BJT	JFET	MOSFET
Input resistance	k $\Omega$	10 <sup>9</sup> $\Omega$ (gigaohms)	10 <sup>12</sup> $\Omega$ (teraohms)
Input gate current	$\mu$ A	1 nA	1 pA
Input offset current	20 nA	2 pA	0.5 pA
Slewing rate	1 V/ $\mu$ s	3 V/ $\mu$ s	10 V/ $\mu$ s

It is now possible to fabricate JFET/MOSFET and BJTs on the same chip using ion implantation techniques. Op-amps which use FET input stages and BJT for the remaining stages are termed as BIFET/BIMOS. By the mid 1980s, BIMOS circuits were produced commercially. Some of the FET IC op-amps available are discussed here briefly.

### JFET Op-amps

An example of a FET input hybrid op-amp is the LH0022/42/52 (National semiconductor) series. This op-amp uses a pair of JFET transistors only for the input-stage differential amplifier and the rest of the circuit uses bipolar transistors. A simplified diagram of this op-amp is shown in Fig. 2.35. The input-stage differential amplifier consists of  $Q_1$  through  $Q_4$  in which  $Q_1$  and  $Q_2$  are  $n$ -channel JFETs operating in a common-drain or source-follower configuration. These JFETs drive  $Q_3$  and  $Q_4$  which operate in the common-base configuration. Thus the differential amplifier uses a compound JFET/bipolar transistor configuration. This provides very high input resistance and very low input current characteristics of JFETs and high-voltage gain that is obtainable from bipolar transistors. This compound differential amplifier drives an active load consisting of  $Q_5$  through  $Q_7$ , operating as a current mirror. The rest of this op-amp is of conventional design as discussed for  $\mu A741$ . Here diodes  $D_1$  and  $D_2$  are used to provide a pre-bias across  $Q_{14}$  and  $Q_{20}$  to minimize cross-over distortion.

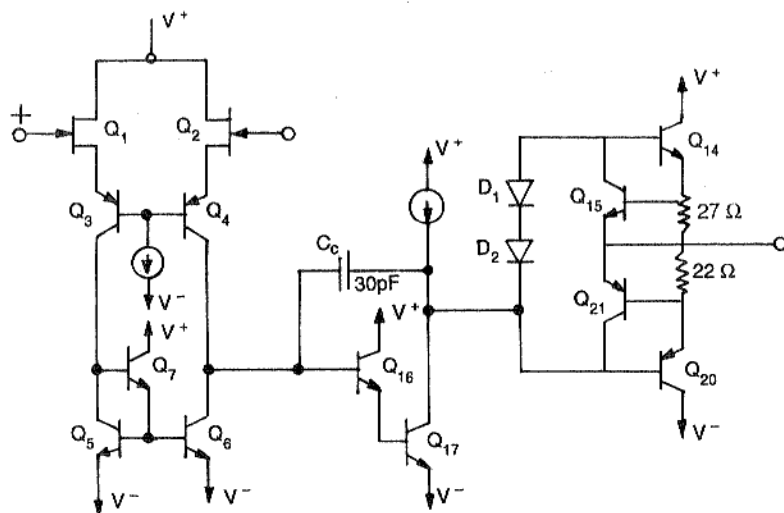


Fig. 2.35 Hybrid JFET-input op-amp LH00 22/42/52 series (National Semiconductor)

### MOSFET Op-Amps

An interesting example of a monolithic MOSFET op-amp is the CA3130 (RCA) which contains both MOSFETs and bipolar transistors on the same chip. A simplified schematic diagram of this device is shown in Fig. 2.36.

The input stage is a differential amplifier consisting of a pair of  $p$ -channel enhancement-mode MOSFETs  $Q_6$  and  $Q_7$ . This differential amplifier is biased by a  $200 \mu A$  MOSFET current source, and it drives a current mirror active load using  $Q_9$  and  $Q_{10}$ . Resistors  $R_5$  and  $R_6$  ( $1 \text{ k}\Omega$ ) in the active load circuit are used together with an externally connected potentiometer (across pins 1 and 5) for offset voltage nulling. The quiescent voltage drop across these resistors in  $100 \mu A \times 1 \text{ k}\Omega = 100 \text{ mV}$ , so that a  $\pm 100 \text{ mV}$  offset adjustment range is available. Diodes  $D_5$  and  $D_8$  are connected between the input terminal to protect the thin gate oxide of the input MOSFETs against excessive voltage spikes and static electricity discharge, which could cause breakdown of the oxide layer and result in irreversible damage to the transistors. The voltage gain of this first stage is only about 5, due to low transfer conductance of the MOSFETs.

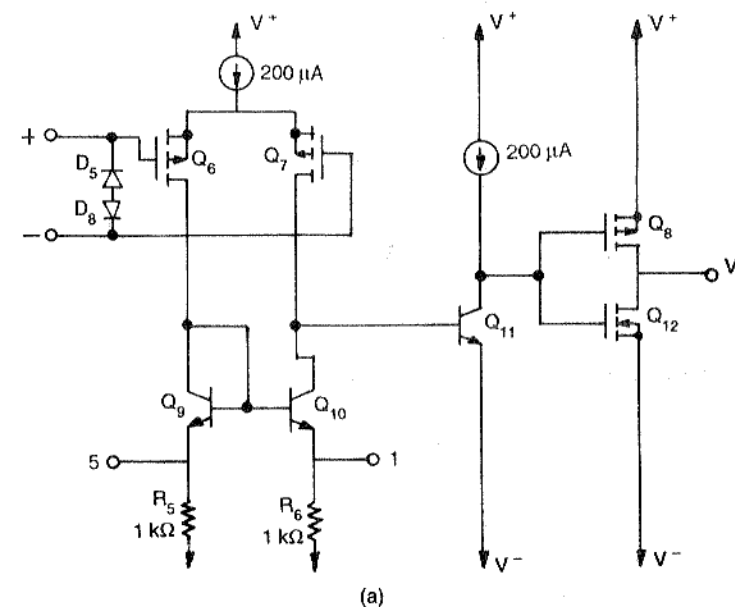


Fig. 2.36 MOSFET-input CMOS output op-amp: CH3130 (RCA Corporation) a simplified schematic diagram

The second stage consists of a bipolar transistor  $Q_{11}$  connected as a common-emitter amplifier, with a  $200 \mu A$  MOSFET current source serving as the active load. As a result of the high dynamic impedance

seen looking into the MOSFET output stage, the voltage gain of the second stage is very large ( $\approx 6000$ ). The output stage is a complementary pair of MOSFETs (CMOS) with  $Q_8$  being the PMOS and  $Q_{12}$  being the NMOS transistor. The use of CMOS pair in the output stage provides significantly low drainage of current from the power supply.

### Summary

1. An op-amp is available in three types of IC packages: metal can, dual-in-line and flat pack.
2. There are five basic terminals: two input terminals, one output terminal and two supply terminals.
3. In open loop mode, the output of the op-amp is at positive or negative saturation level. It does not operate linearly in this mode.
4. Negative feedback stabilizes the gain. Two feedback connections used are: inverting amplifier and non-inverting amplifier.
5. A special case of non-inverting amplifier is the voltage follower.
6. A differential amplifier amplifies the difference between two input signals.
7. An operational amplifier is a direct coupled high gain amplifier consisting of one or more differential amplifiers, followed by a level translator and an output stage.
8. For proper operation of the differential amplifier, matched components must be used. The diff-amp can be biased by using emitter bias (a combination of  $R_E$  and  $V_{BE}$ ), a constant current bias or a current mirror.
9. A current mirror can be used as an active load because it has high ac resistance.
10. MOSFET op-amps offer very high input resistance ( $10^{12} \Omega$ ), low input current ( $\sim 1\text{pA}$ ) and high slewing rate ( $\sim 10\text{V}/\mu\text{s}$ ).

### Review Questions

- 2.1. What is an op-amp?
- 2.2. What are the different linear IC packages?
- 2.3. A 741 op-amp is available in a 14-pin dual-in-line package. What is the terminal number for (i) inverting input (ii) non-inverting input (iii) output?
- 2.4. Explain with figures how two supply voltages  $V^+$  and  $V^-$  are obtained from a single supply.
- 2.5. List six characteristics of an ideal op-amp.
- 2.6. Explain the meaning of open loop and closed loop operation of an op-amp.
- 2.7. Name the type of the feedback used if an external component is connected between the output terminal and the inverting input.

- 2.8. What is the input impedance of a non-inverting op-amp amplifier?
- 2.9. If the open loop gain of an op-amp is very large, does the closed loop gain depend upon the external components or the op-amp?
- 2.10. What is a practical op-amp? Draw its equivalent circuit.
- 2.11. Define common mode rejection ratio.
- 2.12. Explain why  $\text{CMRR} \rightarrow \infty$  for an emitter coupled differential amplifier when  $R_E \rightarrow \infty$ .
- 2.13. Why is  $R_E$  replaced by a constant current bias circuit in a diff-amp?
- 2.14. List and explain the function of all the basic building blocks of an op-amp.
- 2.15. Explain methods for increasing the input resistance of an op-amp.
- 2.16. Explain the difference between constant current bias and current mirror.
- 2.17. Explain why active load is used?
- 2.18. What is a  $V_{BE}$  multiplier?
- 2.19. What is cross-over distortion and how it is eliminated?
- 2.20. Why is cascode configuration used in an op-amp?
- 2.21. Why are FET op-amps better than BJT op-amps?
- 2.22. What is meant by a BIMOS or BIFET amplifier?

### PROBLEMS

- 2.1. In an op-amp of Fig. 2.4 (a),  $v_2 = 0$ . What must be the voltage at  $v_1$  to give an output of 5 V if  $A_{OL} = 50000$ .
- 2.2. Design an inverting amplifier with a gain of  $-5$  and an input resistance of  $10 \text{ k}\Omega$ .
- 2.3. Design a non-inverting amplifier with a gain of 10.
- 2.4. For the circuit shown in Fig. P. 2.4, calculate the range of gain and input impedance.

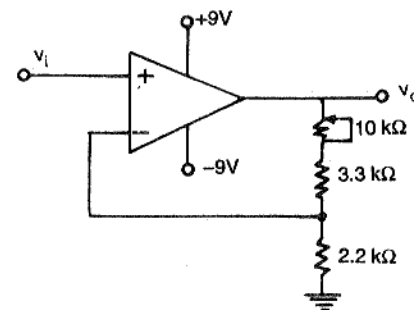


Fig. P. 2.4

- 2.5. Calculate the exact closed loop gain of the inverting amplifier of Fig. 2.5 (b) if  $A_{OL} = 200,000$ ,  $R_i = 2 \text{ M}\Omega$  and  $R_o = 75 \Omega$ .

- 2.6. For the circuit shown in Fig. P. 2.6, calculate the expression of  $v_o/v_i$ .

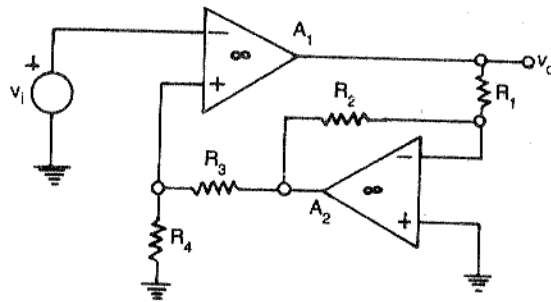


Fig. P. 2.6

- 2.7. In the circuit of Fig. P. 2.7 if  $R_i = \infty$  show that the output admittance  $Y_{of}$  is given by

$$Y_{of} = \frac{1}{R_o} \left( 1 - A_{OL} \frac{R}{R + R'} \right) + \frac{1}{R + R'}$$

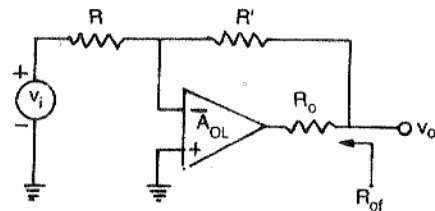


Fig. P. 2.7

- 2.8. Show that the input impedance for the non-inverting amp of Fig. P. 2.8 is

$$R_{if} = R_i \left( 1 + \frac{Z_1}{Z_1 + Z_f} \cdot A_v \right)$$

where  $R_i$  the input resistance of op-amp is large and  $R_o = 0$  and  $A_v$  is the gain without feedback.

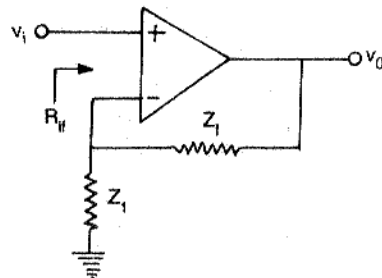


Fig. P. 2.8

- 2.9. Refer to Fig. P. 2.9

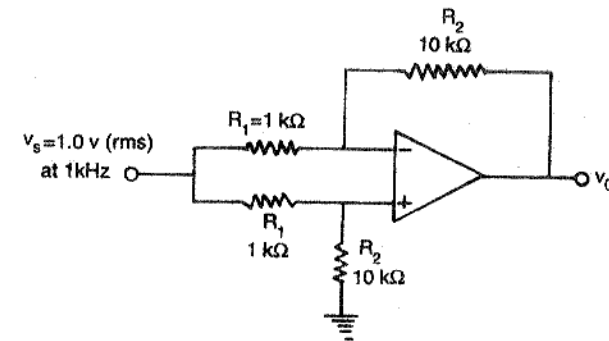


Fig. P. 2.9

- (a) Find  $v_o$  if CMRR = 100 dB at 1 kHz.  
 (b) Find  $v_o$  resulting from 1% mismatches between the two  $R_1$  resistors.  
 (c) Find  $v_o$  resulting from 1% mismatch between two  $R_2$  resistors.
- 2.10. Derive the expression for the output voltage  $v_o$  for the circuit shown in Fig. P. 2.10.

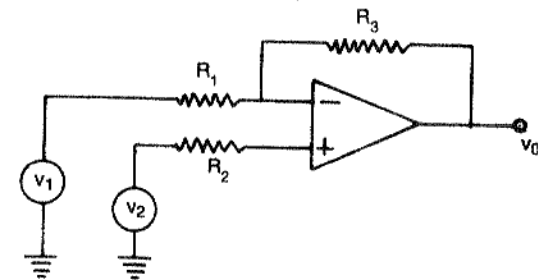


Fig. P. 2.10

- 2.11. Calculate the output voltage of the circuit in Fig. P. 2.11 if the input signal is a 5.5 mA current.

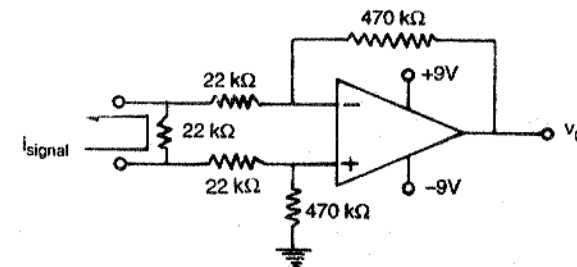


Fig. P. 2.11



- 2.12. What is the voltage at point A and B for the circuit shown in Fig. P. 2.12 if  $v_1 = 5\text{ V}$  and  $v_2 = 5.1\text{ V}$ .

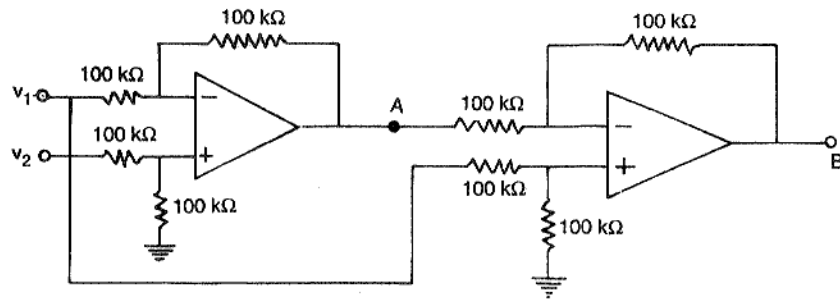


Fig. P. 2.12

- 2.13. For op-amp,  $\text{CMRR} = 10^5$  and differential gain  $A_{\text{DM}} = 10^5$ . Calculate the common mode gain  $A_{\text{CM}}$  of the op-amp.  
 2.14. The  $\text{CMRR}$  of an op-amp is  $10^4$ . Two sets of signals are applied to it. First set is  $V_1 = +20\ \mu\text{V}$  and  $V_2 = -20\ \mu\text{V}$  and second set is  $V_1 = 540\ \mu\text{V}$  and  $V_2 = 500\ \mu\text{V}$ . Calculate the percent difference in output voltage for the two sets of signals.  
 2.15. For the current mirror shown in Fig. P. 2.15, determine  $R$  so that  $I_o = 100\ \mu\text{A}$ .

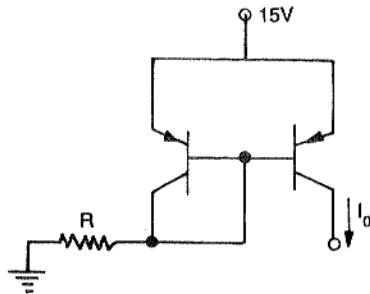


Fig. P. 2.15

- 2.16. In the circuit of Fig. P. 2.16,  $I_R = 50\ \mu\text{A}$ , what is the ratio  $R_1/R_2$  needed for  $I_o = 100\ \mu\text{A}$ ?

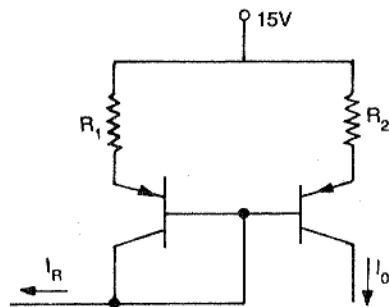


Fig. P. 2.16

- 2.17. For the current mirror shown in Fig. 2.13 (a),  $I_{C2} = 10\ \mu\text{A}$ . If  $V_{\text{BE}} = 15\text{ V}$ , calculate  $R_1$ .  
 2.18. For a modified current mirror shown in Fig. P. 2.18, calculate (i) the current through the collector resistor  $R_c$  and (ii) the collector current in each transistor. Assume  $V_{\text{BE}} = 0.7\text{ V}$  and  $\beta = 100$ .

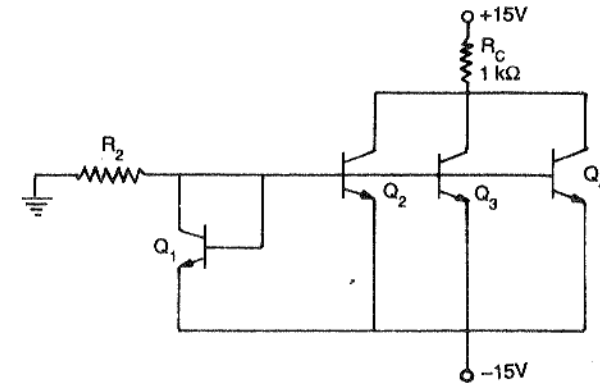


Fig. P. 2.18

- 2.19. For the circuit of Fig. P. 2.19, show that  $V_o = (V_Z + V_{\text{BE}}) (1 + R_1/R_2)$

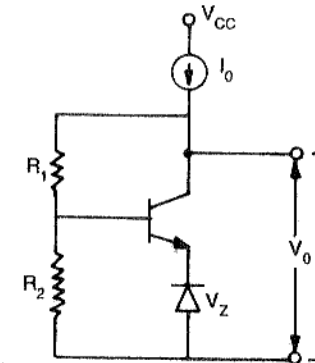


Fig. P. 2.19

- 2.20. For the simple op-amp shown in Fig. P. 2.20, all *n*pn transistors have  $\beta = 200$  and all *p*np transistors have  $\beta = 50$ . Verify that  $v_o = 0$  for  $v_1 = v_2 = 0$ . The current sources shown are realized by *p*np current sources.  
 2.21. For the cascaded differential amplifier shown in Fig. P. 2.21 (i) perform the dc analysis and (ii) calculate the overall voltage gain. Assume  $h_{\text{fe}} = 100$ ,  $V_{\text{BE}} = V_{\text{D}} = 0.7\text{ V}$ .

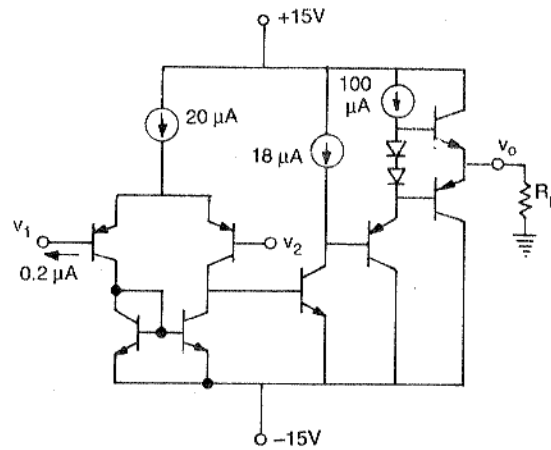


Fig. P. 2.20

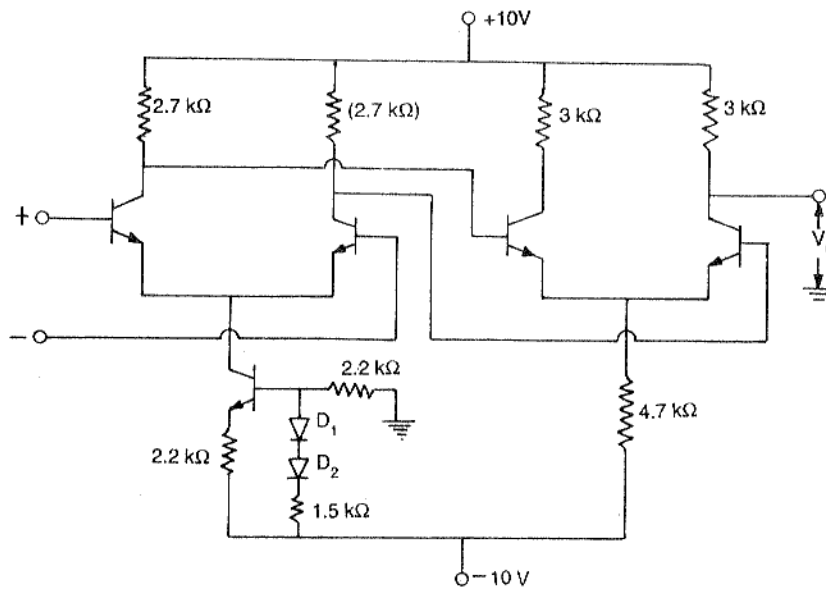


Fig. P. 2.21

**Experiment**

To construct and verify experimentally the theoretical closed loop voltage gain using 741 op-amp for the following:

- (i) Inverting amplifier
- (ii) Non-inverting amplifier
- (iii) Voltage follower

**Procedure**

- (1) Connect the op-amp as an inverting amplifier as shown in Fig. E. 2.1 (a)

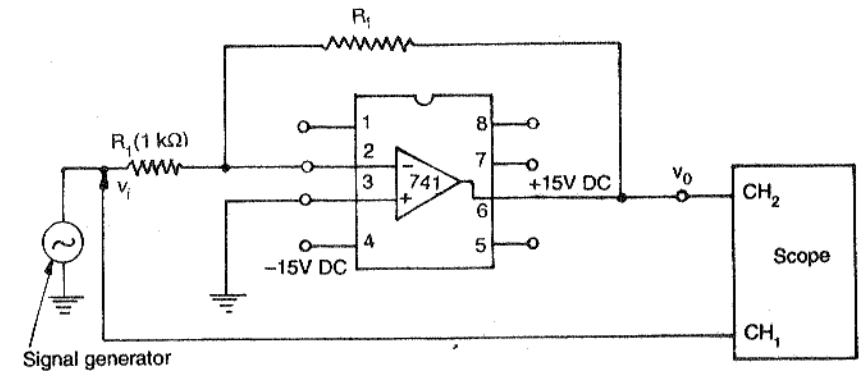


Fig. E. 2.1 (a) Inverting amplifier

- (2) Connect a dual channel scope to simultaneously view  $v_o$  and  $v_i$ . Adjust the signal generator to give 200 mV peak to peak sine wave at 100 Hz. Then measure and record the peak value of  $v_o$  for  $R_f$ : 1 kΩ, 10 kΩ, 33 kΩ and 100 kΩ. Note the phase of  $v_o$  with respect to  $v_i$ .
- (3) Calculate the theoretical closed loop gain  $= R_f/R_1$  for each value of  $R_f$  and compare it with the experimental value of  $v_o/v_i$ .
- (4) Now connect the op-amp as a non-inverting amplifier as shown in Fig. E. 2.1 (b)

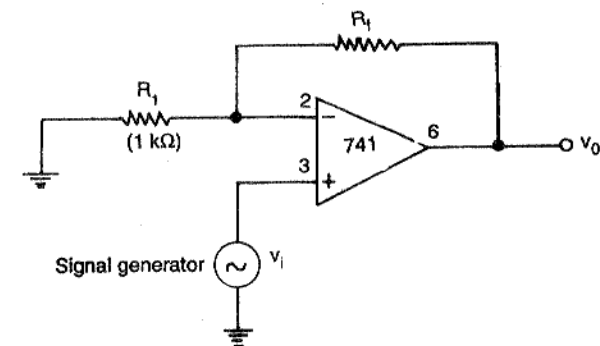


Fig. E. 2.1 (b) Non-inverting amplifier

- (5) Repeat step 2.
- (6) Calculate the theoretical gain  $= 1 + R_f/R_1$  for each value of  $R_f$  and compare it with the experimental value of  $v_o/v_i$ .
- (7) Next make a voltage follower circuit as shown in Fig. E. 2.1. (c)

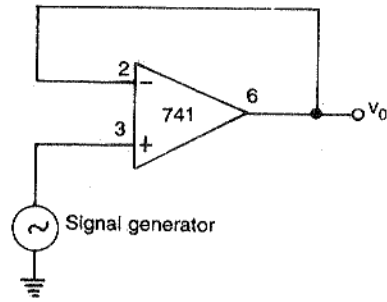


Fig. E. 2.1 (c) Voltage follower

- (8) Measure and record the output voltage  $v_o$  for different input settings: 2 V peak at 100 Hz, 1 V peak at 500 Hz and 5 V peak at 1 kHz. Note the phase of  $v_o$  with respect to  $v_i$  in each case.
- (9) Verify that the voltage gain of the voltage follower is always equal to 1.

**COMPUTER ANALYSIS**

**Program 2.1**

*Inverting Op-Amp Amplifier*

Fig C 2.1(a) shows an inverting op-amp amplifier with various terminals numbered for writing the PSPICE program. The PSPICE description is provided in program 2.1 listing. For circuit values of  $R_1 = 1 \text{ k}\Omega$ ,  $R_f = 10 \text{ k}\Omega$ , the gain of the inverting amplifier is

$$A_v = -\frac{R_f}{R_1} = -10$$

*D.C. Analysis*

For input  $V_1 = 1 \text{ V}$ , the output voltage  $V_0$  should  $V_0 = -10 (1\text{V}) = -10 \text{ V}$ .

From the result file, it can be seen that the output  $V_0$  at node 5 is  $-9.998 \text{ V}$  which gives an error or 0.02% only.

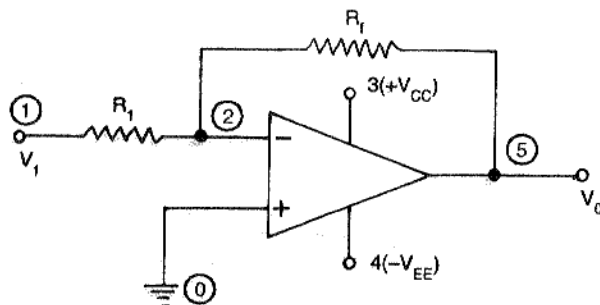


Fig. C 2.1 (a) Circuit for program 2.1

*Transient Analysis*

A sine wave signal of amplitude 0.1 V and frequency 1 kHz is applied at the input terminal. It can be seen from Fig. C 2.1 (b) that the output is a sine wave of amplitude 1 V, 1 kHz. The output waveform is  $180^\circ$  out of the phase with the input waveform as expected.

**Program 2.1: Listing**

**Inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis**

```

*** Circuit Description
*****
***
R1 1 2 1K
RF 2 5 10K
* Op Amp Analysis
X1 0 2 3 4 5 uA 741
. LIB EVAL. LIB
* Power Supplies
VCC 3 0 DC 12V
VEE 0 4 DC 12V
* Input Signal Source
V1 1 0 DC 1V SIN(0 0.1V 1KHZ)
* Output
.DC V1 1 1 1
.TRAN . 5us 5ms 0ms .01 ms
.PROBE
.PRINT DC V(5) V(1)
END
    
```

\*\*\* DC Transfer Curves Temperature = 27.000 DEG C

\*\*\*\*\*

V1	V(5)	V(1)
1.000E+00	-9.998E+00	1.000E+00

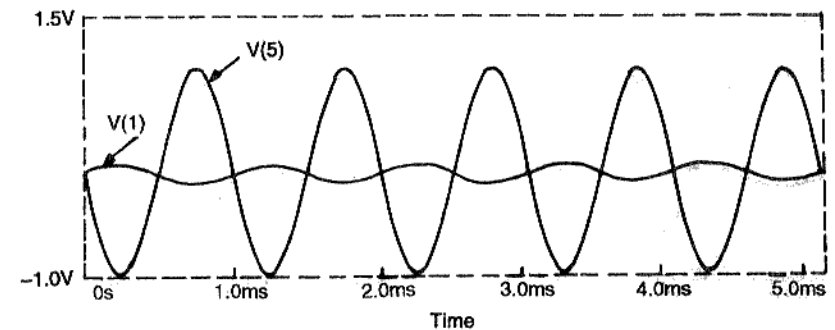


Fig. C 2.1 (b) Inverting Amplifier: Transient Analysis (Output Voltage Vs Time)

**Program 2.2**

**Non-inverting op-amp Amplifier**

The circuit of a non-inverting op-amp amplifier for writing the PSPICE program is shown in Fig. C 2.2 (a).

For the circuit values,  $R_1 = 1 \text{ k}\Omega$  and  $R_f = 9 \text{ k}\Omega$ , the voltage gain is

$$A_V = 1 + \frac{R_f}{R_1} = 1 + \frac{9\text{k}\Omega}{1\text{k}\Omega} = +10$$

$$= 10$$

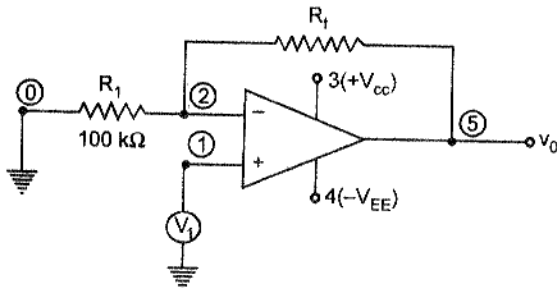


Fig. C 2.2 (a) Circuit for Program 2.2

**D.C. Analysis**

For input voltage  $V_1 = 1\text{V}$ , the output voltage at node 5,  $V(5) = 10\text{V}$

**Transient Analysis**

For input voltage source of amplitude 0.1 V and frequency 1 kHz, the output voltage has an amplitude 1 V at 1 kHz as shown in Fig. C 2.2 (b). It may be noted that there is no phase shift for a non-inverting amplifier.

**Program 2.2 Listing**

Non-inverting Amplifier: DC and Transient (Output Voltage vs Time) Analysis

```

**** Circuit Description
*****
***
R1 0 2 1K
RF 2 5 9K
* Op Amp Analysis
X1 1 2 3 4 5 μA741
.LIB EVAL.LIB
* Power Supplies
VCC 3 0 DC 12V
VEE 0 4 DC 12V
    
```

```

* Input Signal Source
V1 1 0 DC 1V SIN {0} 0.1V 1 KHZ
* Output
.DC V1 1 1 1
.TRAN .5us 5ms 0ms 0.01 ms
.PRINT DC V(5) V(1)
.PROBE
    
```

```

***** DC Transfer Curves Temperature = 27.000 DEG C
*****
***
    
```

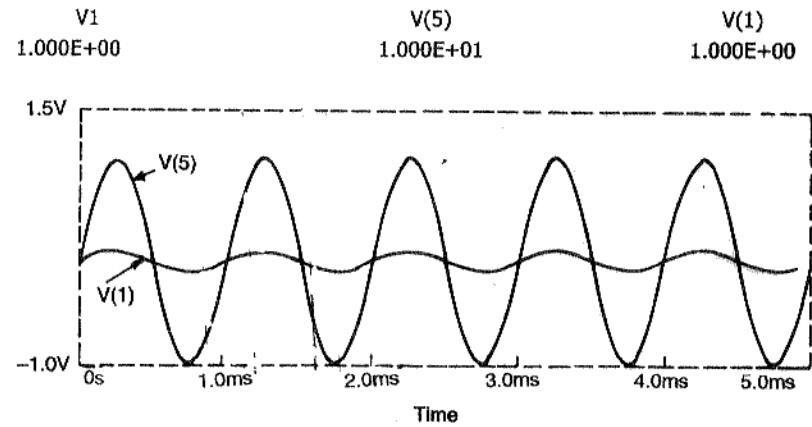


Fig. C 2.2 (b) Non-Inverting Amplifier: Transient Analysis (Output Voltage Vs Time)

**Program 2.3 Voltage Follower**

The circuit diagram of a voltage follower and its PSPICE description are shown in Fig. C 2.3(a) and program 2.3 listing respectively.

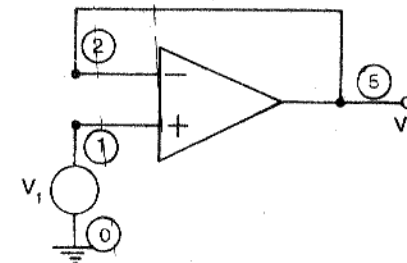


Fig. C 2.3 (a) Circuit for program 2.3

The voltage gain for both d.c. and a.c. input is found to be unity and without change in phase as expected. The transient analysis is shown in Fig. C 2.3 (b). It may be noted that waveforms at node 1 and 5 overlap each other indistinguishably.

Program 2.3 Listing

```
* Voltage Follower
*** Circuit Description
*****
***
RF 2 5 IM
* Op Amp Analysis
X1 1 2 3 4 5 μA741
.LIB EVAL.LIB
* Power Supplies
VCC 3 0 DC 12V
VEE 0 4 DC 12V
* Input Signal Source
V1 1 0 DC 2V SIN(0 .1V 1KHZ)
* Output
* DC V1 2 2 2
* TRAN 0.5us 5ms 0ms 0.01 ms
* PRINT DC V(5) V(1)
* PROBE

**** DC Transfer Curves Temperature = 27.000 DEG C
*****
***
```

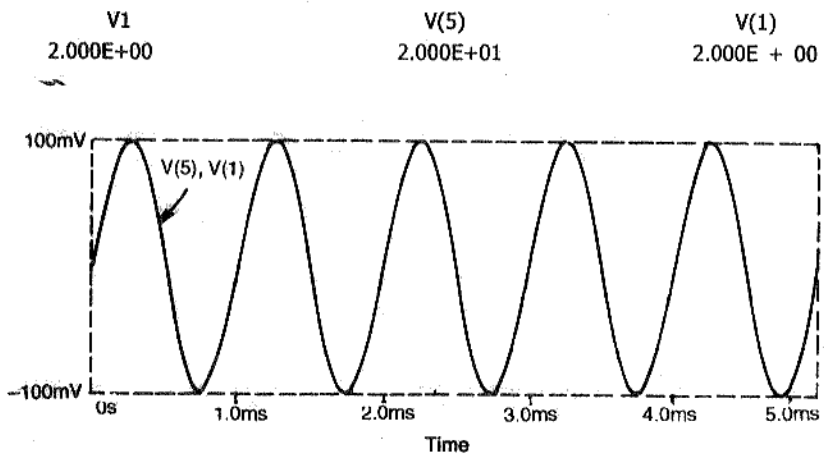


Fig. 2.3 (b) Transient Response of Voltage Follower

## Operational Amplifier Characteristics

### 3.1 INTRODUCTION

Earlier we have used an ideal op-amp, and assumed that the op-amp responds equally well to both ac and dc input voltages. However, a practical op-amp does not behave this way. A practical op-amp has some dc voltage at the output even with both the inputs grounded. The factors responsible for this and the suitable compensating techniques are discussed. Also, under ac conditions the characteristics of an op-amp are frequency dependent. The limitations of an op-amp under ac conditions and methods of compensation are discussed.

### 3.2 DC CHARACTERISTICS

An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way. Current is taken from the source into the op-amp inputs. Also the two inputs respond differently to current and voltage due to mismatch in transistors. A real op-amp also shifts its operation with temperature. These non-ideal dc characteristics that add error components to the dc output voltage are:

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift.

#### 3.2.1 Input Bias Current

The op-amp's input is a differential amplifier, which may be made of BJT or FET. In either case, the input transistors must be biased into