It may be seen that the change in the output state takes place with an increment in input v_i of only 2 mV. This is the uncertainty region where output cannot be directly defined. There are basically two types of comparators:

Non-inverting comparator
Inverting comparator.

The circuit of Fig. 5.2 (a) is called a non-inverting comparator. A fixed reference voltage V_{ref} is applied to (–) input and a time varying

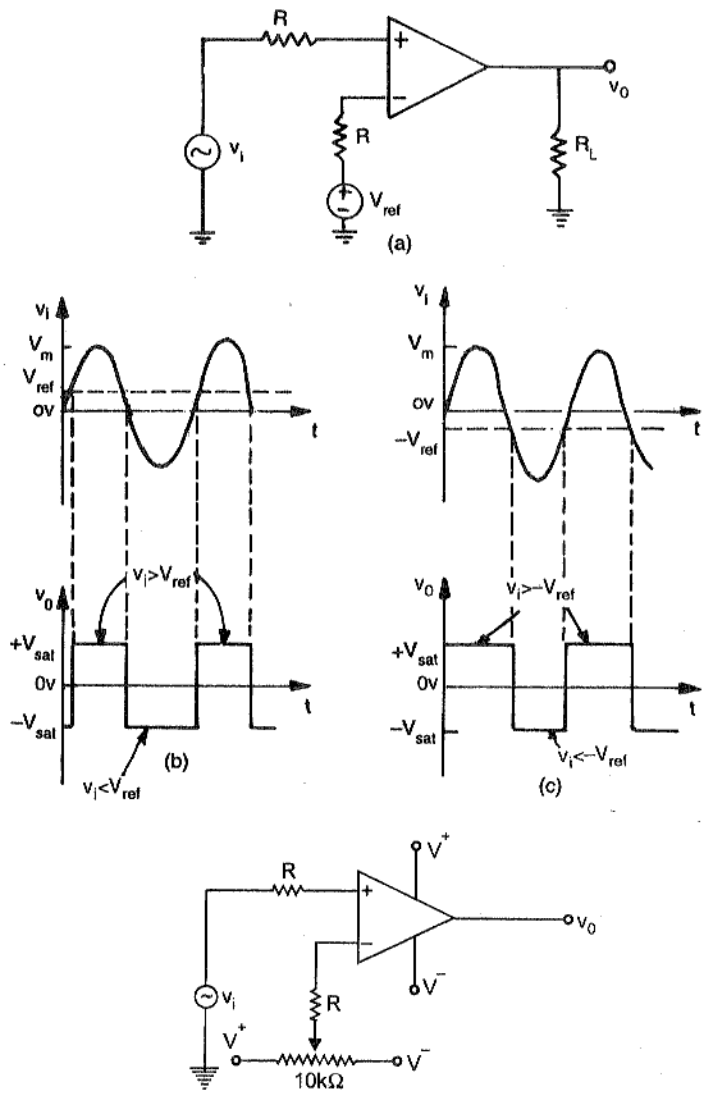


Fig. 5.2 (a) Non-inverting comparator. Input and output waveforms for (b) V_{ref} positive (c) V_{ref} negative (d) Practical noninverting comparator

signal v_i is applied to (+) input. The output voltage is at $-V_{sat}$ for $v_i < V_{ref}$. And v_o goes to $+V_{sat}$ for $v_i > V_{ref}$. The output waveform for a sinusoidal input signal applied to the (+) input is shown in Fig. 5.2 (b and c) for positive and negative V_{ref} respectively.

In a practical circuit V_{ref} is obtained by using a 10 kΩ potentiometer which forms a voltage divider with the supply voltages $V+$ and $V-$ with the wiper connected to (–) input terminal as shown in Fig. 5.2 (d). Thus a V_{ref} of desired amplitude and polarity can be obtained by simply adjusting the 10 kΩ potentiometer.

Figure 5.3 (a) shows a practical inverting comparator in which the reference voltage V_{ref} is applied to the (+) input and v_i is applied to (–) input. For a sinusoidal input signal, the output waveform is shown in Fig. 5.3 (b) and (c) for V_{ref} positive and negative respectively.

Output voltage levels independent of power supply voltages can also be obtained by using a resistor R and two back to back zener diodes at the output of op-amp as shown in Fig. 5.3 (d). The value of resistance R is chosen so the zener diodes operate at the recommended current. It can be seen that the limiting voltages of v_o are $(V_{Z1} + V_D)$ and $-(V_{Z2} + V_D)$ where V_D (~ 0.7 V) is the diode forward voltage.

In the waveforms of Figs. 5.2 and 5.3, the output transitions are shown as taking place instantaneously. Practical circuits, however, take a certain amount of time to switch from one voltage level to another. The actual waveform will therefore exhibit slanted edges as well as delays at the points of input threshold crossing. These effects are more noticeable at high frequencies where the output switching times are comparable or even longer than the input period itself. Thus there is an upper limit to the operating frequency of any comparator.

If 741, the internally compensated op-amp is used as comparator, the primary limitation is the slew rate. Since 741C has slew rate equal to 0.5 V/μs, it takes $2 \times 13/0.5 \simeq 50$ μs ($V_{sat} = \pm$ 13V for 741) to swing from one saturation level to the other. In many applications, this is too long. To increase the response time, it is possible to use uncompensated op-amps such as 301, for comparator applications.

Although uncompensated op-amps make faster comparators than compensated op-amps, there are applications where even higher speeds are required. Also, for interfacing, it is often desired that the output logic levels be compatible with standard logic families such as TTL, CMOS, ECL. To accomodate these needs, monolithic voltage comparators are available. Some of the comparator chips available are the Fairchild μA 710 and 760, the National LM 111, 160 and 311. The response time for 311 is 200 ns whereas 710 is a high speed comparator with a response time of 40 ns. CMOS comparators are also available. Some examples are TLC 372 dual, TLC 374 quad (Texas Instruments), MC 14574 quad (Motorola).

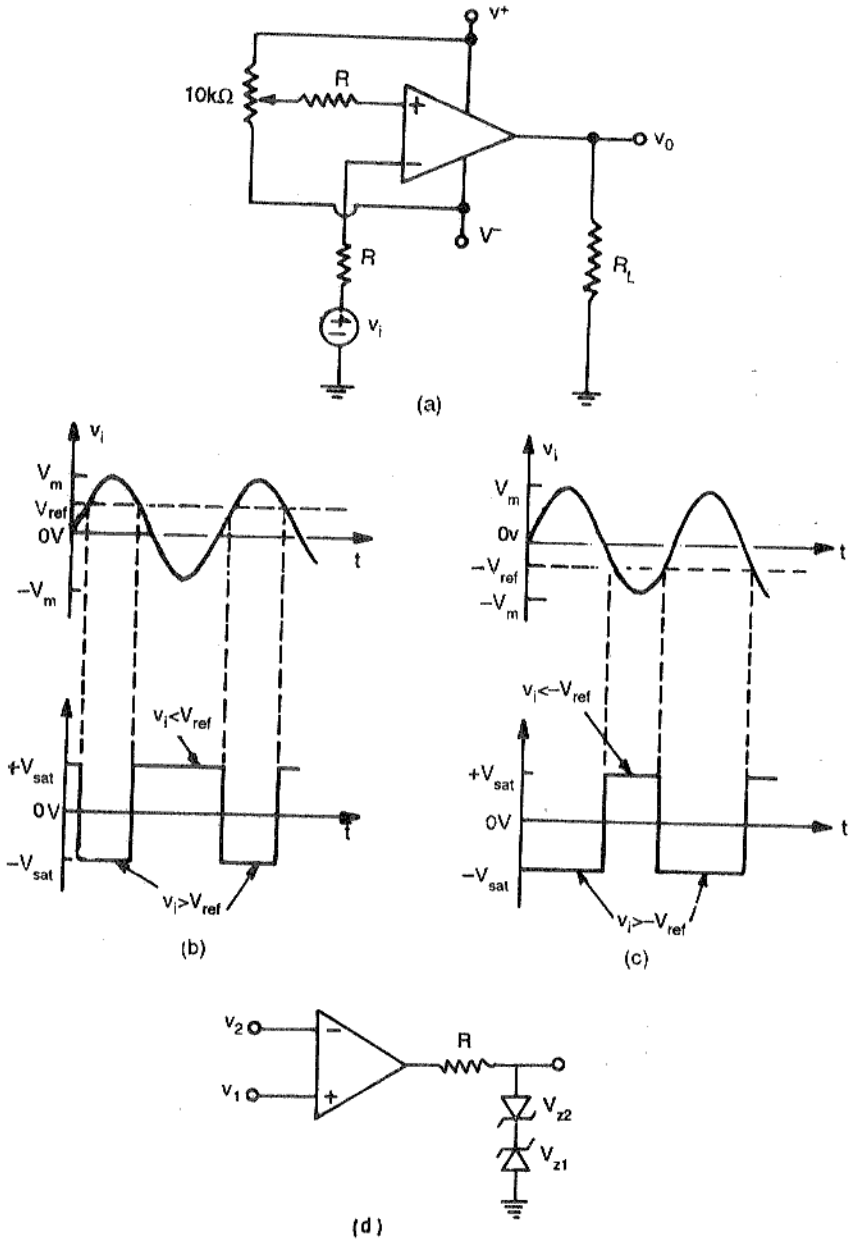


Fig. 5.3 (a) Inverting comparator. Input and output waveforms (b) $V_{ref} > 0$ (c) $V_{ref} < 0$ (d) Comparator with zener diode at the output

5.2.1 Applications of Comparator

Some important applications of comparator are:

Zero crossing detector
Window detector
Time marker generator
Phase meter.

Zero Crossing Detector

The basic comparators of Fig. 5.2 (a) and 5.3 (a) can be used as a zero crossing detector provided that V_{ref} is set to zero. An inverting zero-crossing detector is shown in Fig. 5.4 (a) and the output waveform for a sinusoidal input signal is shown in Fig. 5.4 (b). The circuit is also called a sine to square wave generator.

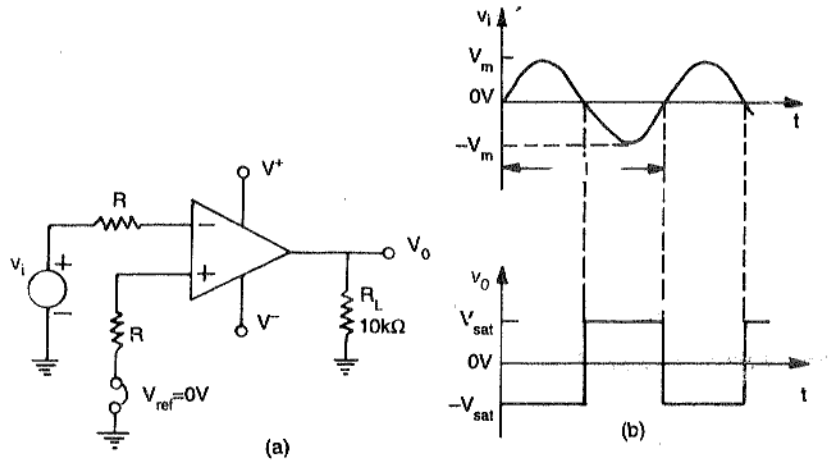


Fig. 5.4 (a) Zero crossing detector (b) Input and output waveforms

Window Detector

Sometimes one may like to mark the instant at which an unknown input is between two threshold levels. This can be achieved by a circuit called window detector. Figure 5.5 shows a three level detector with indicator circuit. There are three indicators: Yellow (LED 3) for input too low (< 3V), Green (LED 2) for safe input (3 – 6V) and Red (LED 1) for high input (> 6V). They are turned ***on*** and ***off*** as indicated in Table 5.1.

Table 5.1 Three level comparator LED specifications

Input (volts)	*Yellow LED 3*	*Green LED 2*	*Red LED 1*
Less than 3 V	On	Off	Off
Between 3 V and 6 V	Off	On	Off
Greater than 6V	Off	Off	On

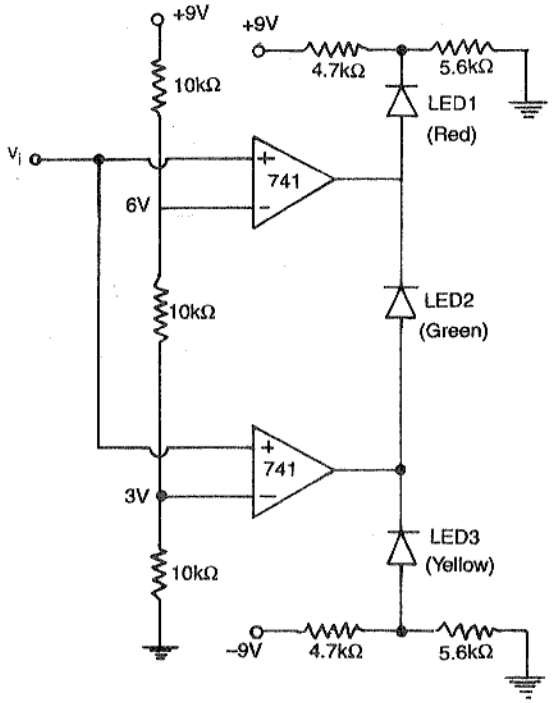


Fig. 5.5 Three level comparator with LED indicator

Time Marker Generator

The circuit is shown in Fig. 5.6 (a). The output of the zero-crossing detector is differentiated by an RC circuit ($RC << T$), so that the voltage v′ is a series of positive and negative pulses as shown in Fig. 5.6 (d). The negative portion is clipped off after passing through the diode D and the waveform v_L is as shown in Fig. 5.6 (e). So, with the help of this circuit, the sinusoid has been converted into a train of

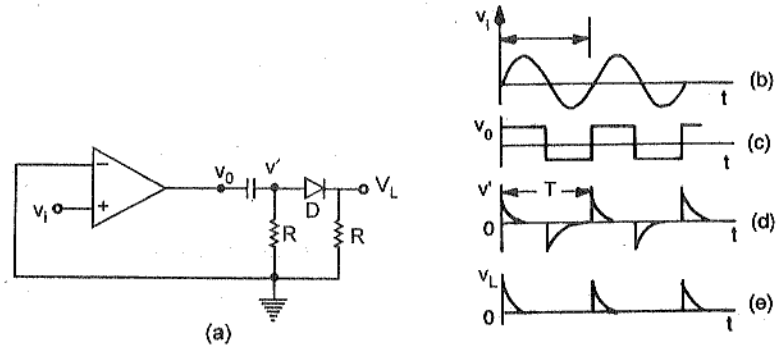


Fig. 5.6 (a) Time marker circuit (b) Input waveform (c) output v_o (d) differentiated output v′ (e) output pulses

positive pulses of sp ...nd may be used for triggering the monoshots, SCR, swe ...ge of CRT etc.

Phase Detector

The phase angle between two voltages can also be measured using the circuit of Fig. 5.6 (a). Both voltages are converted into spikes and the time interval between the pulse spikes of one input and that of the other is measured. The time interval is proportional to the phase difference. One can measure phase angles from 0° to 360° with such a circuit.

Example 5.1

(a) For the comparator shown in Fig. 5.7 (a) plot the transfer curve if the op-amp is an ideal one and $V_{Z1} = V_{Z2} = 9$ V.

(b) Repeat part (a) if the open loop gain of op-amp is 50,000.

Solution

(a) Since $A_{OL} = \infty$, even a small positive or negative voltage at the input drives the output to $\pm V_{sat}$. This causes V_{Z1} or V_{Z2} to break down, giving output voltage $v_o = \pm (V_Z + V_D) = \pm 9.7$ V. The transfer curve is shown in Fig. 5.7 (b).

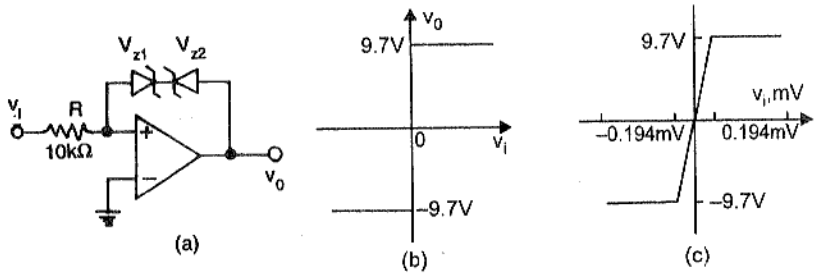


Fig. 5.7 (a) Circuit of Example 5.1 (b) Transfer curve for Example 5.1 (a). (c) Transfer curve for Example 5.1 (b)

(b) Now $A_{OL} = 50{,}000$, so $\Delta v_i = \dfrac{9.7}{A_{OL}} = 0.194$ mV. The zeners break down after ± 0.194 mV as shown in the transfer curve of Fig. 5.7 (c).

5.3 REGENERATIVE COMPARATOR (SCHMITT TRIGGER)

If positive feedback is added to the comparator circuit, gain can be increased greatly. Consequently, the transfer curve of comparator becomes more close to ideal curve. Theoretically, if the loop gain $-\beta A_{OL}$ is adjusted to unity, then the gain with feedback, A_{Vf} becomes

infinite. This results in an abrupt (zero rise time) transition between the extreme values of output voltage. In practical circuits, however, it may not be possible to maintain loop-gain exactly equal to unity for a long time because of supply voltage and temperature variations. So a value greater than unity is chosen. This also gives an output waveform virtually discontinuous at the comparison voltage. This circuit, however, now exhibits a phenomenon called hysteresis or backlash.

Figure 5.8 (a) shows such a regenerative comparator. The circuit is also known as Schmitt Trigger. The input voltage is applied to the (–) input terminal and feedback voltage to the (+) input terminal. The input voltage v_i triggers the output v_o every time it exceeds certain voltage levels. These voltage levels are called upper threshold voltage (V_{UT}) and lower threshold voltage (V_{LT}). The hysteresis width is the difference between these two threshold voltages i.e. $V_{UT} - V_{LT}$. These threshold voltages are calculated as follows.

Suppose the output $v_o = +V_{sat}$. The voltage at (+) input terminal will be

$$V_{ref} + \frac{R_2}{R_1 + R_2}(V_{sat} - V_{ref}) = V_{UT} \qquad (5.1)$$

This voltage is called upper threshold voltage V_{UT}. As long as v_i is less than V_{UT}, the output v_o remains constant at $+V_{sat}$. When v_i is just greater than V_{UT}, the output regeneratively switches to $-V_{sat}$ and remains at this level as long as $v_i > V_{UT}$ as shown in Fig. 5.8 (b).

For $v_o = -V_{sat}$, the voltage at the (+) input terminal is,

$$V_{ref} - \frac{R_2}{R_1 + R_2}(V_{sat} + V_{ref}) = V_{LT} \qquad (5.2)$$

This voltage is referred to as lower threshold voltage V_{LT}. The input voltage v_i must become lesser than V_{LT} in order to cause v_o to switch from $-V_{sat}$ to $+V_{sat}$. A regenerative transition takes place as shown in Fig. 5.8 (c) and the output v_o returns from $-V_{sat}$ to $+V_{sat}$ almost instantaneously. The complete transfer characteristics are shown in Fig. 5.8 (d).

Note that $V_{LT} < V_{UT}$ and the difference between these two voltages is the hysteresis width V_H and can be written as

$$V_H = V_{UT} - V_{LT} = \frac{2 R_2 V_{sat}}{R_1 + R_2} \qquad (5.3)$$

Because of the hysteresis, the circuit triggers at a higher voltage for increasing signals than for decreasing ones. Further, note that if peak-to-peak input signal v_i were smaller than V_H then the Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction would never reset itself, that is, once the output has jumped to, say, $+V_{sat}$ it would remain at this level and never return

to $-V_{sat}$. It may be seen from Eq. (5.3) that hysteresis width V_H is independent of V_{ref}. The resistor R_3 in Fig. 5.8 (a) is chosen equal to $R_1 \| R_2$ to compensate for the input bias current. A non-inverting Schmitt trigger is obtained if v_i and V_{ref} are interchanged in Fig. 5.8 (a) (problem 5.10). The most important application of Schmitt trigger circuit is to convert a very slowly varying input voltage into a square wave output as shown in Fig. 5.8 (e).

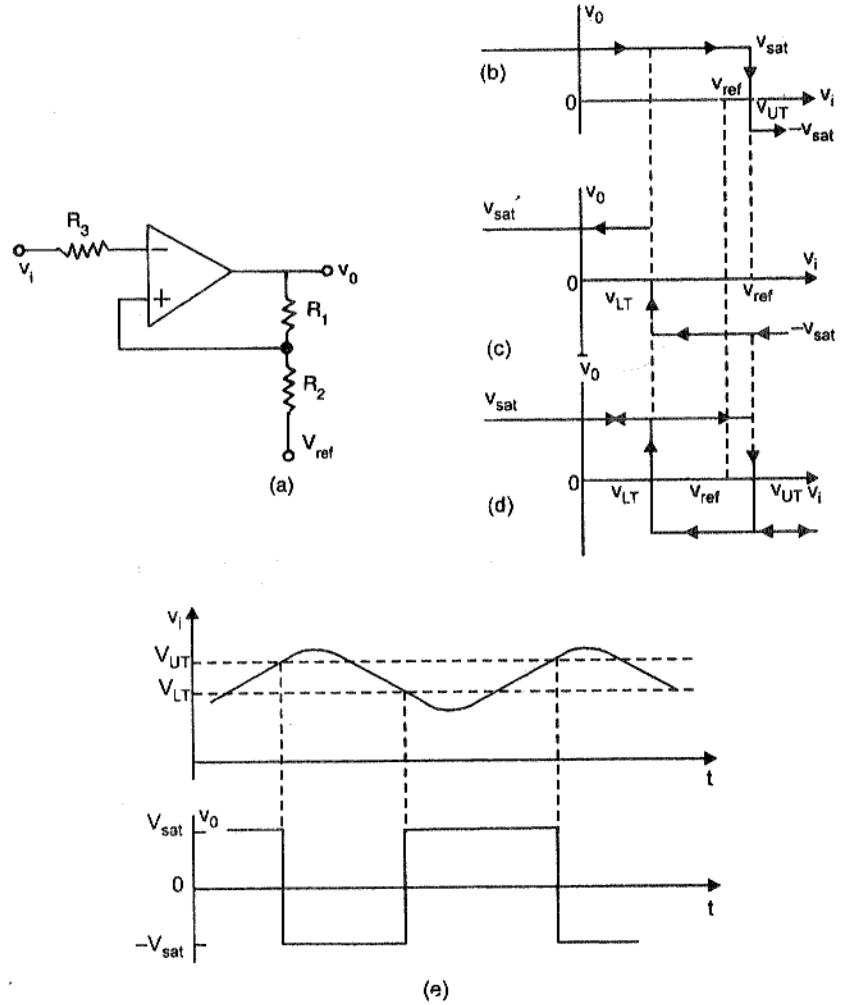
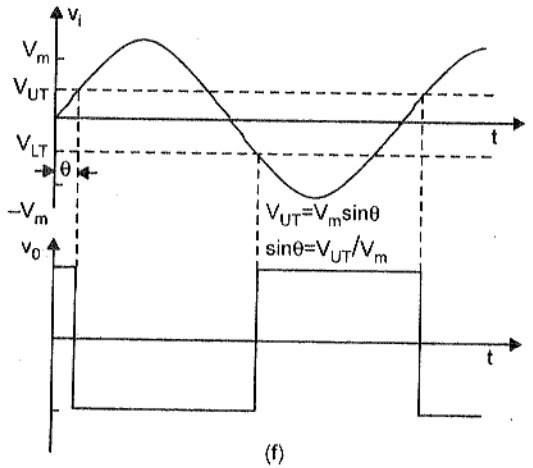


Fig. 5.8 (a) An inverting Schmitt trigger (b, c) Transfer characteristics for v_i increasing and v_i decreasing (d) composite input-output curve (e) Schmitt Trigger used as a squarer

If in the circuit of Fig. 5.8 (a), V_{ref} is chosen as zero volt, it follows from Eqs. (5.1) and (5.2) that

$$V_{UT} = -V_{LT} = \frac{R_2 V_{sat}}{R_1 + R_2}$$

If an input sinusoid of frequency $f = 1/T$ is applied to such a comparator, a symmetrical square wave is obtained at the output. The vertical edge of the output waveform however will not occur at the time the sine wave passes through zero [Fig. 5.8 (f)] but is shifted in phase by θ where $\sin\theta = V_{UT}/V_m$ and V_m is the peak sinusoidal voltage.



(f)

Fig. 5.8 (f) Shift θ in the output waveform for $V_{UT} = -V_{LT}$

Special purpose Schmitt triggers are commercially available. T1–13, T1–14 and T1–132 chips with totem pole output and $V_{UT} = 1.7$ V, $V_{LT} = 0.9$ V are available. The T1–132 package is a quad two-input NAND Schmitt trigger. CMOS Schmitt triggers offer the advantage of high input impedance and low power consumption. Examples of CMOS inverting Schmitt trigger are the CD40106B and 744C14.

Example 5.2

In the circuit of Schmitt trigger of Fig. 5.8 (a), $R_2 = 100\ \Omega$, $R_1 = 50\ k\Omega$, $V_{ref} = 0V$, $v_i = 1V_{pp}$ (peak-to-peak) sine wave and saturation voltage = ± 14V. Determine threshold voltages V_{UT} and V_{LT}.

Solution

From Eqs. (5.1) and (5.2)

$$V_{UT} = \frac{100}{50100} \times 14 = 28\ \text{mV}$$

$$V_{LT} = \frac{100}{50100} \times (-14) = -28\ \text{mV}$$

Example 5.3

A Schmitt trigger with the upper threshold level $V_{UT} = 0$V and hysteresis width $V_H = 0.2$V converts a 1 kHz sine wave of amplitude $4V_{pp}$ into a square wave. Calculate the time duration of the negative and positive portion of the output waveform.

Solution

$$V_{UT} = 0$$

$$V_H = V_{UT} - V_{LT} = 0.2\ \text{V}$$

So, $$V_{LT} = -0.2\ \text{V}$$

In Fig. 5.9, the angle θ can be calculated as

$$-0.2 = V_m \sin(\pi + \theta) = -V_m \sin\theta = -2 \sin\theta$$

$$\theta = \text{arc sin } 0.1 = 0.1 \text{ radian}$$

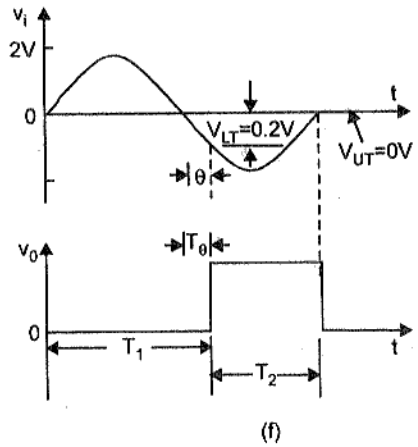
The period, $T = 1/f = 1/1000 = 1$ ms

$$\omega T_\theta = 2\pi\ (1000)\ T_\theta = 0.1$$

$$T_\theta = (0.1/2\pi)\ \text{ms} = 0.016\ \text{ms}$$

So, $$T_1 = T/2 + T_\theta = 0.516\ \text{ms}$$

and $$T_2 = T/2 - T_\theta = 0.484\ \text{ms}$$



(f)

Fig. 5.9 Circuit for Example 5.3

5.4 SQUARE WAVE GENERATOR (ASTABLE MULTIVIBRATOR)

A simple op-amp square wave generator is shown in Fig. 5.10 (a). Also called a free running oscillator, the principle of generation of square wave output is to force an op-amp to operate in the saturation region. In Fig. 5.10 (a) fraction $\beta = R_2/(R_1 + R_2)$ of the output is fed back to the (+) input terminal. Thus the reference voltage V_{ref} is βv_o and may

take values as $+\beta V_{sat}$ or $-\beta V_{sat}$. The output is also fed back to the (–) input terminal after integrating by means of a low-pass RC combination. Whenever input at the (–) input terminal just exceeds V_{ref}, switching takes place resulting in a square wave output. In astable multivibrator, both the states are quasi stable.

Consider an instant of time when the output is at $+V_{sat}$. The capacitor now starts charging towards $+V_{sat}$ through resistance R, as shown in Fig. 5.10 (b). The voltage at the (+) input terminal is held at $+\beta V_{sat}$ by R_1 and R_2 combination. This condition continues as the charge on C rises, until it has just exceeded $+\beta V_{sat}$, the reference voltage. When the voltage at the (–) input terminal becomes just greater than this reference voltage, the output is driven to $-V_{sat}$. At this instant, the voltage on the capacitor is $+\beta V_{sat}$. It begins to dischaıge through R, that is, charges toward $-V_{sat}$. When the output voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. The cycle repeats itself as shown in Fig. 5.10 (b).

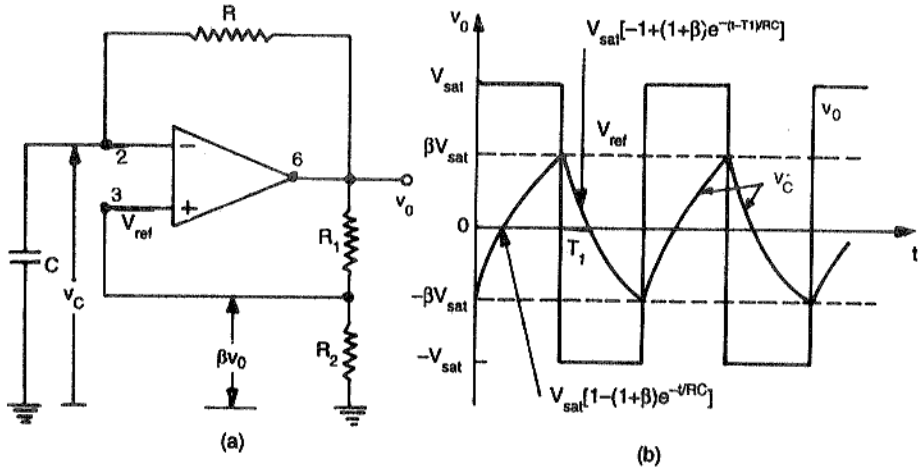


Fig. 5.10 (a) Simple op-amp square wave generator (b) waveforms

The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice versa. The voltage across the capacitor as a function of time is given by,

$$v_c(t) = V_f + (V_i - V_f)e^{-t/RC} \tag{5.4}$$

where, the final value, $V_f = +V_{sat}$

and the initial value, $V_i = -\beta V_{sat}$

Therefore,

$$v_c(t) = V_{sat} + (-\beta V_{sat} - V_{sat})\, e^{-t/RC}$$

or

$$v_c(t) = V_{sat} - V_{sat}\,(1 + \beta)\, e^{-t/RC} \tag{5.5}$$

At $t = T_1$, voltage across the capacitor reaches βV_{sat} and switching takes place, Therefore,

$$v_c(T_1) = \beta V_{sat} = V_{sat} - V_{sat}\,(1+\beta)e^{-T_1/RC} \tag{5.6}$$

After algebraic manipulation, we get,

$$T_1 = RC \ln \frac{1+\beta}{1-\beta} \tag{5.7}$$

This give only one half of the period.

Total time period

$$T = 2T_1 = 2RC \ln \frac{1+\beta}{1-\beta} \tag{5.8}$$

and the output wave form is symmetrical.

If $R_1 = R_2$, then $\beta = 0.5$, and $T = 2RC$ ln 3. And for $R_1 = 1.16R_2$, it can be seen that $T = 2\ RC$

or

$$f_0 = \frac{1}{2RC}$$

The output swings from $+V_{sat}$ to $-V_{sat}$, so,

$$v_o \text{ peak-to-peak} = 2\ V_{sat} \tag{5.9}$$

The peak to peak output amplitude can be varied by varying the power supply voltage. However, a better technique is to use back to back zener diodes as shown in Fig. 5.10 (c). The output voltage is regulated to $\pm\ (V_Z + V_D)$ by the zener diodes.

$$v_o \text{ peak-to-peak} = 2\ (V_Z + V_D) \tag{5.10}$$

Resistor R_{sc} limits the currents drawn from the op-amp to,

$$I_{sc} = \frac{V_{sat} - V_Z}{R_{sc}} \tag{5.11}$$

This circuit works reasonably well at audio frequencies. At higher frequencies, however, slew-rate of the op-amp limits the slope of the output square wave.

If an asymmetric square wave is desired, then zener diodes with different break down voltages V_{Z1} and V_{Z2} may be used. Then the output is either V_{o1} or V_{o2}, where $V_{o1} = V_{Z1} + V_D$ and $V_{o2} = V_{Z2} + V_D$. It can be easily shown that the positive section is given by,

$$T_1 = RC \ln \frac{1 + \beta\, V_{o2}/V_{o1}}{1-\beta} \tag{5.12}$$

The duration of negative section T_2 will be the same as given by Eq. (5.12) with V_{o1} and V_{o2} interchanged.

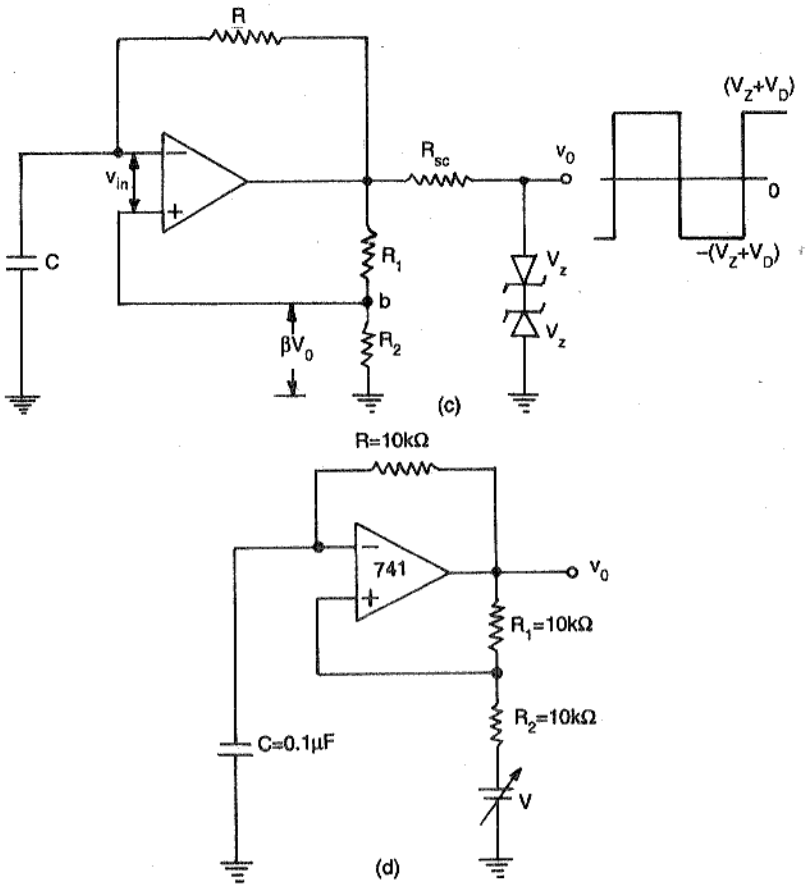


Fig. 5.10 (c) Use of back to back zener diodes. (d) Asymmetric square wave generator

An alternative method to get asymmetric square wave output is to add a dc voltage source V in series R_2 as shown in Fig. 5.10 (d). Now the capacitor C swings between the voltage levels (βV_{sat} + V) and ($-\beta V_{sat}$ + V). If the voltage source V is made variable, voltage to frequency conversion can be achieved though the variation will not be linear.

5.5 MONOSTABLE MULTIVIBRATOR

Monostable multivibrator has one stable state and the other is quasi stable state. The circuit is useful for generating single output pulse of adjustable time duration in response to a triggering signal. The width of the output pulse depends only on external components connected to the op-amp. The circuit shown in Fig. 5.11(a) is a modified form of the astable multivibrator. A diode D_1 clamps the capacitor voltage to

0.7V when the output is at + V_{sat}. A negative going pulse signal of magnitude V_1 passing through the differentiator R_4C_4 and diode D_2 produces a negative going triggering impulse and is applied to the (+) input terminal.

To analyse the circuit, let us assume that in the stable state, the output v_o is at + V_{sat}. The diode D_1 conducts and v_c the voltage across the capacitor C gets clamped to + 0.7V. The voltage at the (+) input terminal through R_1R_2 potentiometric divider is + βV_{sat}. Now, if a negative trigger of magnitude V_1 is applied to the (+) input terminal so that the effective signal at this terminal is less than 0.7V i.e. ([β V_{sat} + (– V_1)] < 0.7 V), the output of the op-amp will switch from + V_{sat} to – V_{sat}. The diode will now get reverse biased and the capacitor starts charging exponentially to $-V_{sat}$ through the resistance R. The voltage at the (+) input terminal is now $-\beta V_{sat}$. When the capacitor voltage v_c becomes just slightly more negative than $-\beta V_{sat}$, the output of the op-amp switches back to + V_{sat}. The capacitor C now starts charging to + V_{sat} through R until v_c is 0.7V as capacitor C gets clamped to the voltage. Various waveforms are shown in Fig. 5.11 (b, c, d).

The pulse width T of monostable multivibrator is calculated as follows:

The general solution for a single time constant low pass RC circuit with V_i and V_f as initial and final values is,

$$v_o = V_f + (V_i - V_f)e^{-t/RC} \tag{5.13}$$

For the circuit, $V_f = -V_{sat}$ and $V_i = V_D$ (diode forward voltage).

The output v_c is,

$$v_c = -V_{sat} + (V_D + V_{sat})\, e^{-t/RC} \tag{5.14}$$

at $t = T$,

$$v_c = -\beta V_{sat} \tag{5.15}$$

Therefore,

$$-\beta\, V_{sat} = -V_{sat} + (V_D + V_{sat})e^{-t/RC}$$

After simplification, pulse width T is obtained as

$$T = RC \ln \frac{(1 + V_D/V_{sat})}{1-\beta} \tag{5.16}$$

where $\beta = R_2/(R_1 + R_2)$

If, $V_{sat} >> V_D$ and $R_1 = R_2$ so that $\beta = 0.5$, then

$$T = 0.69\ RC \tag{5.17}$$

For monostable operation, the trigger pulse width T_p should be much less than T, the pulse width of the monostable multivibrator.

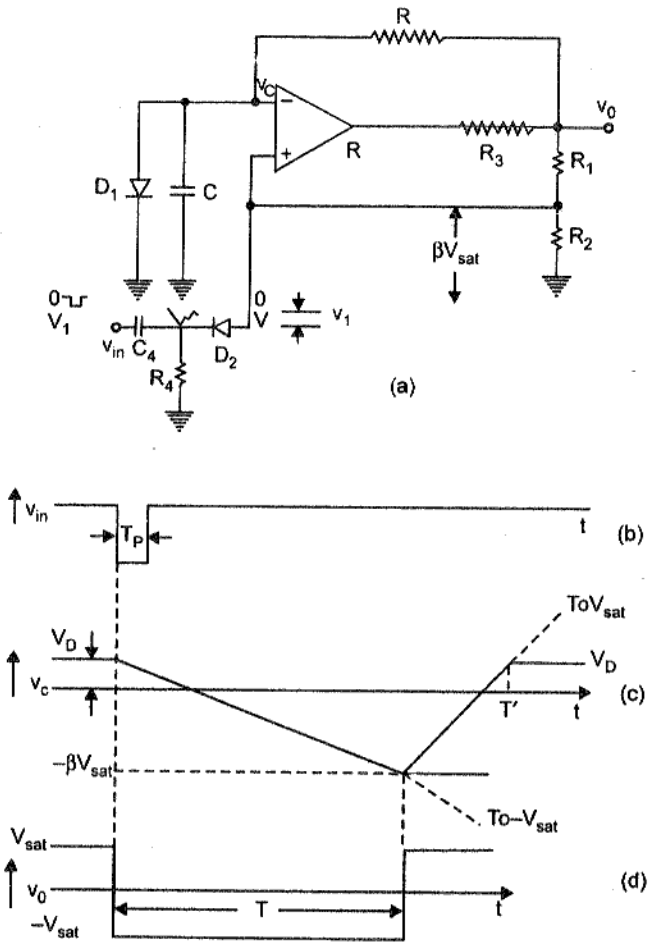


Fig. 5.11 (a) Monostable multivibrator (b) negative going triggering signal (c) capacitor waveform (d) output voltage waveform

The diode D_2 is used to avoid malfunctioning by blocking the positive noise spikes that may be present at the differentiated trigger input.

It may be noted from Fig. 5.11 (b) that capacitor voltage v_c reaches its quiescent value V_D at $T' > T$. Therefore, it is essential that a recovery time $T' - T$ be allowed to elapse before the next triggering signal is applied. The circuit of Fig. 5.11(a) can be modified to achieve voltage to time delay conversion as in the case of square wave generator. The monostable multivibrator circuit is also referred to as time delay circuit as it generates a fast transition at a predetermined time T after the application of input trigger. It is also called a gating circuit as it generates a rectangular waveform at a definite time and thus could be used to gate parts of a system.

5.6 TRIANGULAR WAVE GENERATOR

A triangular wave can be simply obtained by integrating a square wave as shown in Fig. 5.12(a). It is obvious that the frequency of the square wave and triangular wave is the same as shown in Fig. 5.12 (b). Although the amplitude of the square wave is constant at $\pm V_{sat}$, the amplitude of the triangular wave will decrease as the frequency increases. This is because the reactance of the capacitor C_2 in the feedback circuit decreases at high frequencies. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies as in the case of practical integrator.

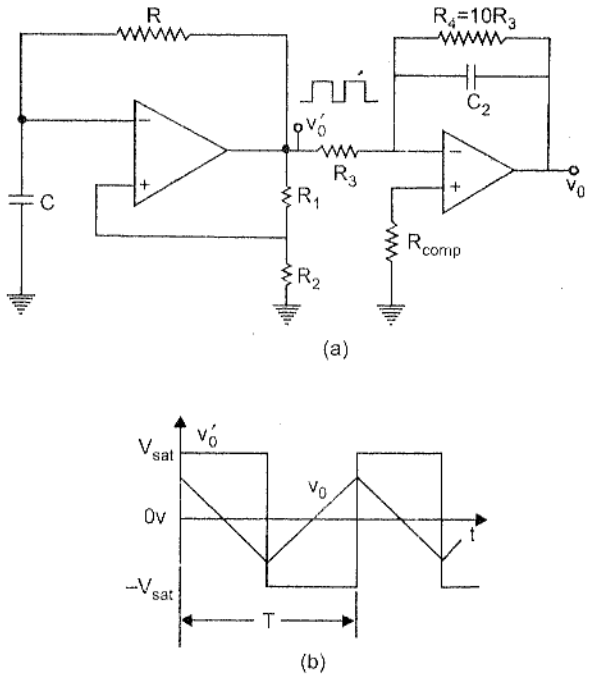
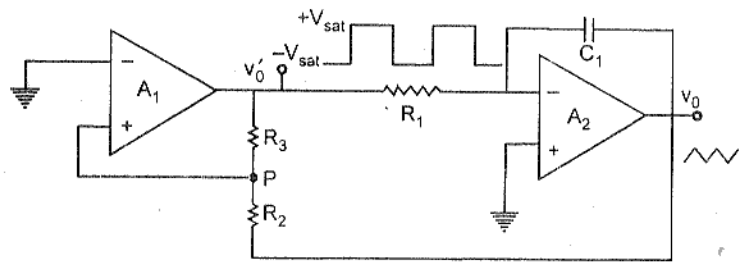


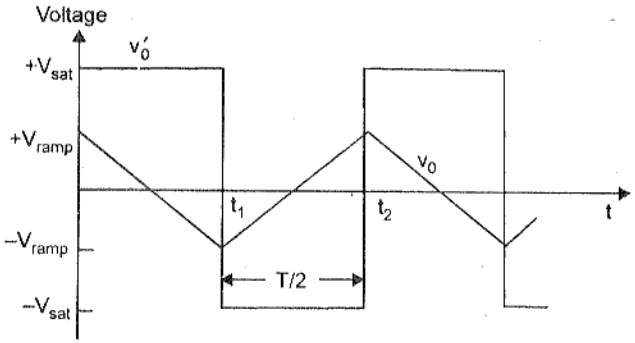
Fig. 5.12 (a) Triangular waveform generator (b) output waveform

Another triangular wave generator using lesser number of components is shown in Fig. 5.13(a). It basically consists of a two level comparator followed by an integrator. The output of the comparator A_1 is a square wave of amplitude $\pm V_{sat}$ and is applied to the (–) input terminal of the integrator A_2 producing a triangular wave. This triangular wave is fed back as input to the comparator A_1 through a voltage divider R_2R_3.

Initially, let us consider that the output of comparator A_1 is at $+V_{sat}$. The output of the integrator A_2 will be a negative going ramp as shown in Fig. 5.13(b). Thus one end of the voltage divider R_2R_3 is



(a)



(b)

Fig. 5.13 (a) Triangular waveform generator using lesser components (b) Waveforms

at a voltage $+V_{sat}$ and the other at the negative going ramp of A_2. At a time $t = t_1$, when the negative going ramp attains a value of $-V_{ramp}$, the effective voltage at point P becomes slightly less than 0V. This switches the output of A_1 from positive saturation to negative saturation level $-V_{sat}$. During the time when the output of A_1 is at $-V_{sat}$, the output of A_2 increases in the positive direction. And at the instant $t = t_2$, the voltage at point P becomes just above 0V, thereby switching the output of A_1 from $-V_{sat}$ to $+V_{sat}$. The cycle repeats and generates a triangular waveform. It can be seen that the frequency of the square wave and triangular wave will be the same. However, the amplitude of the triangular wave depends upon the RC value of the integrator A_2 and the output voltage level of A_1. The output voltage of A_1 can be set to desired level by using appropriate zener diodes. The frequency of the triangular waveform can be calculated as follows:

The effective voltage at point P during the time when output of A_1 is at $+V_{sat}$ level is given by,

$$-V_{ramp} + \frac{R_2}{R_2 + R_3}\left[+V_{sat} - (-V_{ramp})\right] \qquad (5.18)$$

At $t = t_1$, the voltage at point P becomes equal to zero. Therefore, from Eq. (5.18),

$$-V_{ramp} = -\frac{R_2}{R_3}(+V_{sat}) \qquad (5.19)$$

Similarly, at $t = t_2$, when the output of A_1 switches from $-V_{sat}$ to $+V_{sat}$.

$$V_{ramp} = \frac{-R_2}{R_3}(-V_{sat})$$

$$= \frac{R_2}{R_3}(V_{sat}) \qquad (5.20)$$

Therefore, peak to peak amplitude of the triangular wave is,

$$v_o\,(pp) = +V_{ramp} - (-V_{ramp})$$

$$= 2\,\frac{R_2}{R_3}V_{sat} \qquad (5.21)$$

The output switches from $-V_{ramp}$ to $+V_{ramp}$ in half the time period $T/2$. Putting the values in the basic integrator equation

$$\left(v_o = -\frac{1}{RC}\int v_i\,dt\right)$$

$$v_o(pp) = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt$$

$$= \frac{V_{sat}}{R_1C_1}\left(\frac{T}{2}\right)$$

or,
$$T = 2\,R_1C_1\,\frac{v_o\,(pp)}{V_{sat}} \qquad (5.22)$$

Putting the value of v_o (pp) from Eq. (5.21), we get

$$T = \frac{4R_1C_1R_2}{R_3}$$

Hence the frequency of oscillation f_o is,

$$f_o = \frac{1}{T} = \frac{R_3}{4R_1C_1R_2} \qquad (5.23)$$

5.7 SINE WAVE GENERATORS

As oscillator is basically a feedback circuit where a fraction v_f of the output voltage v_o of an amplifier is fed back to the input in the same phase. The block diagram of an oscillator is shown in Fig. 5.14.

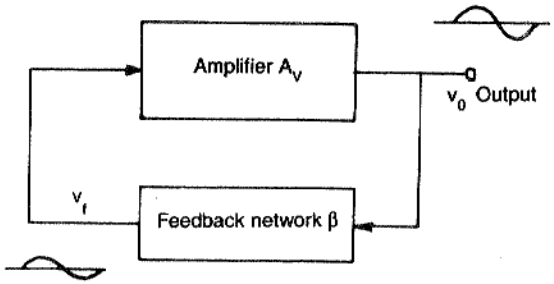


Fig. 5.14 Block diagram of a feedback oscillator

For sustained oscillation, $A_v\beta = 1$. That is, magnitude condition $|A_v\beta| = 1$ and the phase condition, $\angle A_v\beta = 0°$ or 360° must be simultaneously satisfied in the circuit.

There are different types of sine-wave oscillators available according to the range of frequency, namely *RC* oscillators for audio frequency and *LC* oscillators for radio frequency range. Here we will discuss only two types of audio frequency *RC* oscillators.

Phase Shift Oscillator

Figure 5.15 shows a phase shift oscillator. The op-amp provides a phase shift of 180° as it is used in the inverting mode. An additional

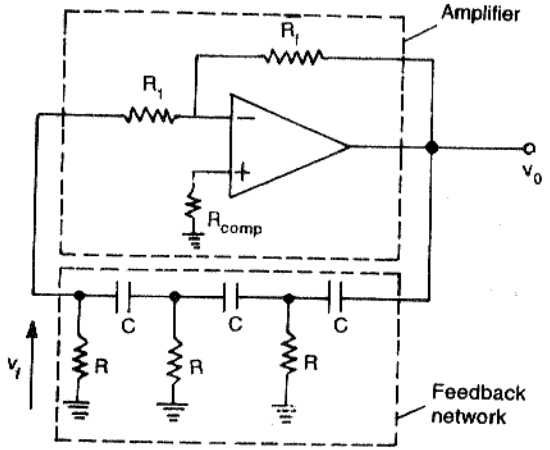


Fig. 5.15 Phase shift oscillator

phase shift of 180° is provided by the feedback *RC* network. The transfer function of the *RC* network can be easily calculated as,

$$\beta = \frac{v_f}{v_o} = \frac{1}{1 + 6/sRC + 5/s^2R^2C^2 + 1/s^3R^3C^3}$$

Letting $s = j\omega$,

$$\beta = \frac{1}{1 - 5(f_1/f)^2 - j[6(f_1/f) - (f_1/f)^3)} \tag{5.24}$$

where $f_1 = \dfrac{1}{2\pi RC}$

For $A_v\,\beta = 1$, β should be real. So the imaginary term in Eq. (5.24) must be equal to zero, that is,

$$6(f_1/f) - (f_1/f)^3 = 0$$

or $\quad f_1/f = \sqrt{6}$

The frequency of the oscillation f_o is given by,

$$f_o = \frac{1}{\sqrt{6}\,(2\pi\,RC)} \tag{5.25}$$

Also, the loop gain $A_v\,\beta = 1$

or, $\quad \dfrac{A_v}{1 - 5\,(f_1/f_o)^2} = 1$

or, $\quad A_v \geq -29$

That is the gain of the inverting op-amp should be atleast 29, or $R_f = 29\,R_1$. The gain A_v is kept greater than 29 to ensure that variations in circuit parameters will not make $|A_v\beta| < 1$, otherwise oscillations will die out.

For low frequencies (< 1 kHz), op-amp 741 may be used, however for high frequencies, LM 318 or LF 351 should be used.

Example 5.4

Design a phase shift oscillator of Fig. 5.15 to oscillate at 100 Hz.

Solution

Let $C = 0.1\ \mu F$. Then from Eq. (5.25)

$$R = \frac{1}{\sqrt{6}\,2\pi\,(10^{-7})\,(100)} = 6.49\ k\Omega$$

Use $R = 6.5\ k\Omega$

To prevent loading of the amplifier by *RC* network, $R_1 \leq 10\,R$

Therefore, let $R_1 = 10\ R = 65\ \text{k}\Omega$

Since $R_f = 29\ R_1$

$R_f = 1885\ \text{k}\Omega$

Wien Bridge Oscillator

Another commonly used audio frequency oscillator is a Wien bridge oscillator. The circuit is shown in Fig. 5.16 (a). It may be noted that the feedback signal in this circuit is connected to the (+) input terminal so that the op-amp is working as a non-inverting amplifier. Therefore, the feedback network need not provide any phase shift. The circuit can be viewed as a Wien bridge with a series RC network in one arm and a parallel RC network in the adjoining arm. Resistors R_1 and R_f are connected in the remaining two arms. The condition of zero phase shift around the circuit is achieved by balancing the bridge.

From the feedback network, the feedback factor β is,

$$\beta = \frac{v_f}{v_o} = \frac{R/(1+j\omega RC)}{[(R - j/\omega C) + R/(1+j\omega RC)]}$$

$$= \frac{R}{3R + j(\omega R^2 C - 1/\omega C)} \qquad (5.26)$$

For $A_v\beta = 1$, β must be real. That is the imaginary term in Eq. (5.26) must be zero.

$$\omega R^2 C - \frac{1}{\omega C} = 0$$

or, $$\omega = \frac{1}{RC}$$

The frequency of oscillation f_o is,

$$f_o = \frac{1}{2\pi RC} \qquad (5.27)$$

At f_o, from Eq. (5.26), β is equal to 1/3. Therefore, for sustained oscillation, the amplifier must have a gain of precisely 3. However, from practical point of view, A_v may be slightly less or greater than 3. For $A_v < 3$, the oscillations will either die down or fail to start when power is first applied. And, for $A_v > 3$, the oscillations will be growing. This problem is eliminated by a practical Wien bridge oscillator with adaptive negative feedback as shown in Fig. 5.16(b). In this circuit, resistor R_4 is initially adjusted to give a gain so that oscillations start. The output signal grows in amplitude until the voltage across R_3 approaches the cut-in voltage of the diode. As the diodes begin to turn-on (one for the positive half cycle and the other for the negative half cycle), the effective feedback resistance R_f decreases because the diode is in parallel with the resistance R_3. This will reduce the gain

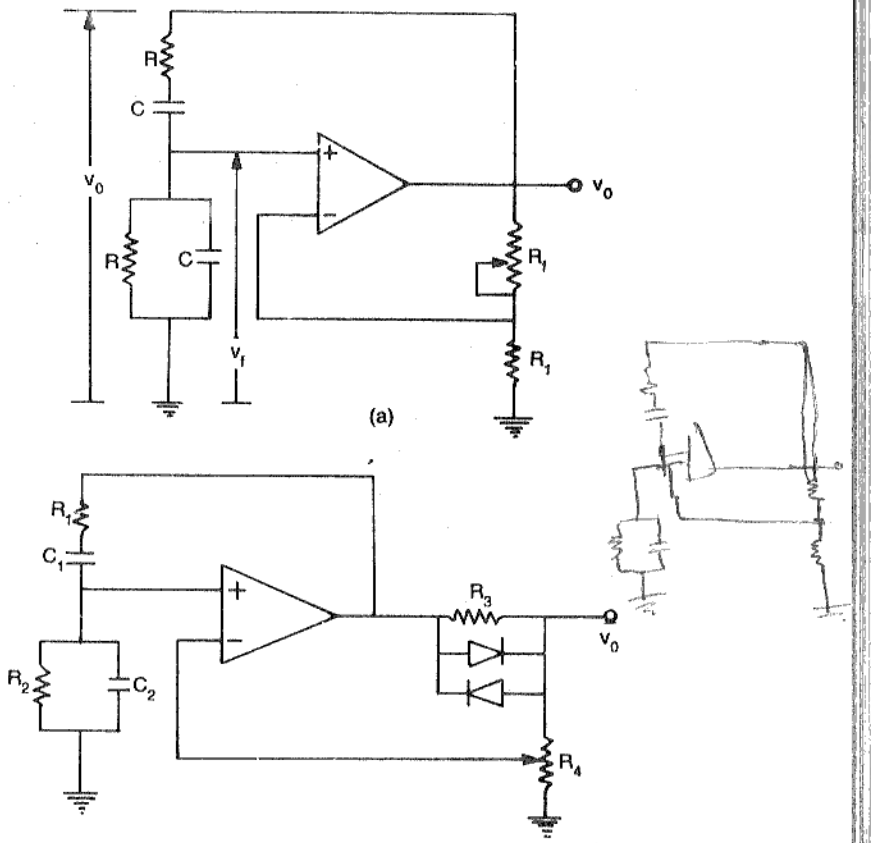


Fig. 5.16 (a) Wien bridge oscillator (b) practical Wien bridge oscillator with adaptive negative feedback

of the amplifier which in turn lowers the output amplitude. Hence sustained oscillations can be obtained. Further, if the output signal falls, the diodes would begin to turn-off thereby increasing R_f which in turn increases gain.

Summary

1. A comparator is an open loop op-amp with analog inputs and a digital output ($\pm V_{sat} \approx V_{cc}$).
2. Reduced output voltage levels can be obtained by using back-to-back zener diodes at the output.
3. Zero crossing detector is a comparator with $V_{ref} = 0$.
4. A window detector determines when an unknown input is between two threshold levels.
5. Schmitt trigger is a comparator with positive feedback.
6. In Schmitt trigger, the input voltage triggers the output every time it exceeds certain voltage levels called upper threshold V_{UT} and lower threshold V_{LT}.

7. A Schmitt trigger converts slowly varying waveforms into square wave.
8. The frequency of a square wave generator depends upon the RC components and the trigger levels of the comparator.
9. A monostable multivibrator is used to generate pulses of desired duration and is also called a gating circuit.
10. A triangular wave can be generated by integrating a square wave.
11. For self-sustained oscillation, two conditions must be satisfied:
    (i) The magnitude of the loop gain $A_v\beta$ must be equal to 1.
    (ii) The total phase shift of the loop gain must be 0°.
12. The phase shift and Wien bridge are the most commonly used sine wave oscillators for audio frequencies. The frequency of oscillation depends upon RC components.

Review Questions

5.1. Draw the characteristics of an ideal comparator and that of a commercially available comparator.
5.2. List the different types of comparators.
5.3. What is the meaning of voltage limiting? Show how it is obtained.
5.4. Draw a circuit for converting a square wave into a series of positive pulses.
5.5. What is a window detector?
5.6. Explain how to measure the phase difference between two signals.
5.7. What is hysteresis? What parameters determine the hysteresis?
5.8. Explain the operation of a square wave generator by drawing the capacitor and output voltage waveforms.
5.9. Explain how a non-symmetrical square wave can be obtained.
5.10. How would you recognize that positive feedback is being used in an op-amp circuit.
5.11. What is the other name of one shot?
5.12. Draw and explain the operation of a triangular wave generator.
5.13. What is the difference between a sawtooth wave and a triangular wave?
5.14. State the two conditions of oscillations.
5.15. Classify the oscillators.
5.16. In Wien bridge oscillator of Fig. 5.16, one set of circuit components determines the frequency of oscillation and another set of components determines if the circuit will oscillate at that frequency. Identify these two set of components.

PROBLEMS

5.1. Draw the input and output waveforms of the op-amp shown in Fig. P. 5.1.

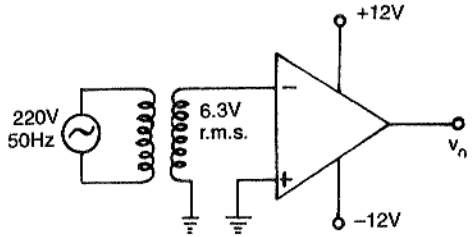


Fig. P. 5.1

5.2. Draw output of the op-amp shown in Fig. P. 5.2. (a) for given v_2 as in Fig. P. 5.2. (b) when (i) $V_1 = 0$ (ii) $V_1 = 4$V.

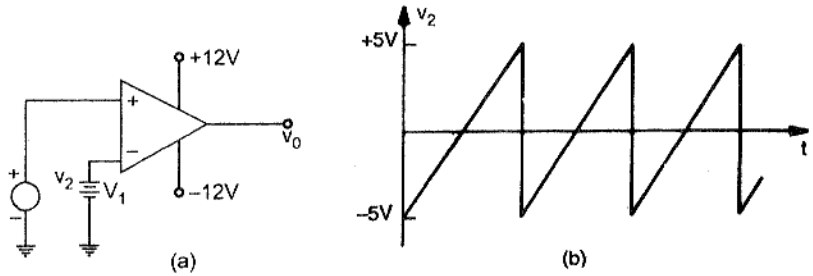


Fig. P. 5.2 (a) & (b)

5.3. For the circuit shown in Fig. P. 5.3., what is the condition of each of the LEDs for (i) $v_i = 1$ V (ii) $v_i = 2$ V.

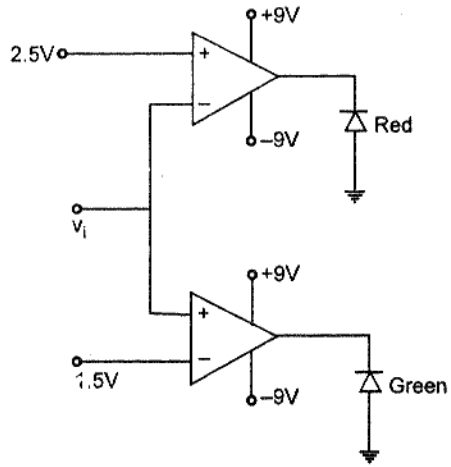


Fig. P. 5.3

5.4. For the circuit shown in Fig. P. 5.4, calculate the trigger points if supply voltage $V = \pm$ 12 V. Plot the output voltage v_o vs t if v_i is a 100 Hz triangular wave of magnitude ± 10 V.

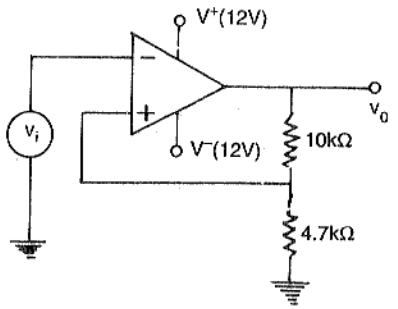


Fig. P. 5.4

5.5. In the circuit of Fig. 5.7 (a) v_i = 100 mV peak sine wave at 100 Hz, R = 1 kΩ and $V_{Z1} = V_{Z2}$ = 6.2 V and the op-amp is a 741 with supply voltages = ± 12 V. Draw the output waveform.

5.6. For the circuit shown in Fig. P.5.6, v_i = 500 mV peak 100 Hz sine wave, R = 100 Ω, V_Z = 6.2 V, V_D = 0.7 V and supply voltages = ± 15 V. Determine the output voltage swing and draw the output waveform.

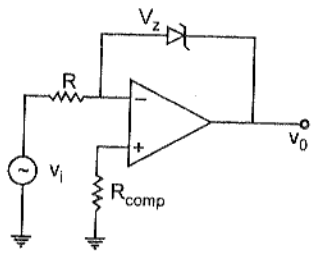


Fig. P. 5.6

5.7. In a Schmitt Trigger of Fig. 5.8 (a) hysteresis of 0.1 V is desired. Calculate V_{ref}, V_{sat} and R_1 if $V_{UT} = V_{ref}$, A_{OL} = 100,000 and loop gain is 1000 and R_2 = 1 kΩ.

5.8. The Schmitt Trigger of Fig. 5.8 (a) uses 9V zener diodes. Calculate R_1/R_2 and V_{ref} if V_D = 0.7 V, V_{UT} = 0 and V_H = 0.2 V.

5.9. (a) In the Schmitt trigger of Fig. 5.8 (a), v_o = 8 V, V_{UT} = 4 V and V_{LT} = 3 V. Calculate R_1/R_2 and V_{ref}.
(b) Calculate the value of V_{ref} so that V_{LT} is negative.
(c) Calculate V_{ref} for $V_{UT} = -V_{LT}$.

5.10. For the non-inverting Schmitt comparator circuit shown in Fig. P. 5.10, calculate the threshold levels V_{UT} and V_{LT} and the hysteresis V_H.

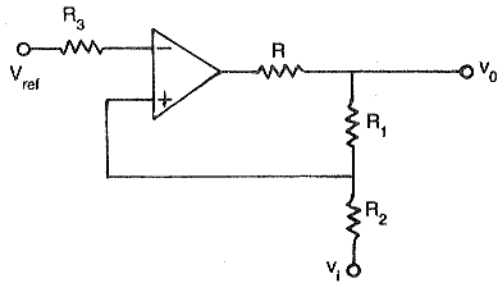


Fig. P. 5.10

5.11. In the square wave oscillator of Fig. 5.10 (a) calculate the frequency of oscillation if P_2 = 10 kΩ, R_1 = 11.6 kΩ, R = 100 kΩ, C = 0.01 μF.

5.12. Design a square wave oscillator for f = 1 kHz. The op-amp is a 741 with supply voltages ± 15 V.

5.13. Design a monostable multivibrator with trigger pulse shaping which will drive a LED ***on*** for 0.5 second each time it is pulsed.

Experiment 5.1

(a) To study the operation of 741 op-amp as a comparator.
(b) To design a Schmitt trigger for V_{UT} = + 0.5V and V_{LT} = – 0.5V and show its use for generating a square wave output.

(a) Comparator

Procedure

1. Connect the circuit shown in Fig. E. 5.1 (a) and adjust the 10 kΩ potentiometer so that V_{ref} = +0.5V.
2. Adjust the signal generator so that v_i = 2 V pp sine wave at 1 kHz.
3. Using a CRO observe the input and output waveform simultaneously. Plot the output waveform.
4. Adjust the 10 kΩ potentiometer so that V_{ref} = – 0.5V. Repeat step 3.
5. To make a zero crossing detector, set V_{ref} = 0V and observe the output waveforms.

(b) Schmitt Trigger

Design: In Fig. E. 5.1 (b)

$$V_{UT} = \frac{R_2}{R_1 + R_2} V_{sat}$$

and

$$V_{LT} = \frac{R_2}{R_1 + R_2} (-V_{sat})$$

For 741, with supply voltages = ± 15V, the saturation voltage ± V_{sat} = ± 14 V.

So, $$0.5\text{V} = \frac{R_2}{R_1 + R_2}(14\text{ V})$$

Or, $R_1 = 27\ R_2$

Choose, $R_2 = 1\ \text{k}\Omega$

So, $R_1 = 27\ \text{k}\Omega$ (take a 50 kΩ pot)

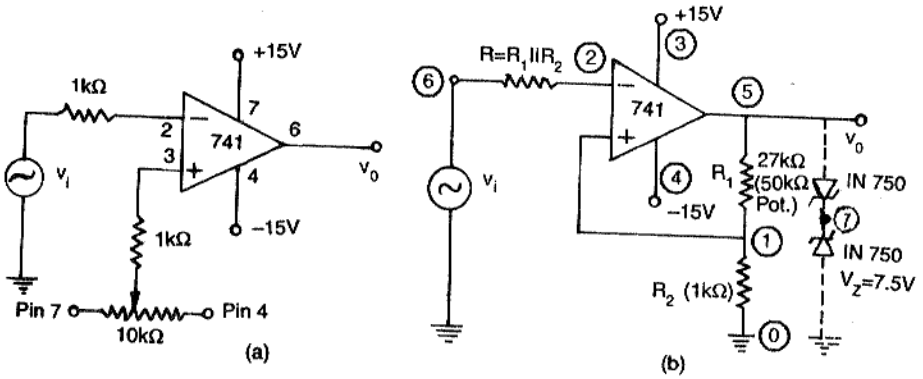


Fig. E. 5.1 (a) Comparator (b) Schmitt trigger

Procedure

1. Connect the circuit of Fig. 5.1(b) with the values obtained in the design. Please note than Fig. E. 5.1(b) has been numbered for PSPICE simulation given in Computer program 5.1.
2. Adjust the signal generator so that $v_i = 2$ V pp sine wave at 1 kHz.
3. Plot the input and output waveforms.
4. Connect two zener diodes (IN 750, $V_z = 7.5$ V) at the output and find value of R_1 to get the same values of V_{UT} and V_{LT}.

Computer Program 5.1 (Schmitt Trigger)

Fig. E. 5.1. (b) has been numbered for PSPICE simulation and its listing is shown below. The input and output waveforms have been shown in Fig. C. 5.1 (a) and (b) for (i) without zener diodes (ii) with zener diodes

Program 5.1 Listing

```
*Schmitt Trigger- SINE WAVE INPUT
R   6  2  1K
R1  5  1  27K
R2  1  0  1K
*Zener Diodes at the output
*D1  5  7  DIN750
*D2  0  7  DIN750
*  Op-amp analysis
   X1  1  2  3  4  5  UA741
   .LIB  EVAL.LIB
*  Power supplies
   VCC  3  0  DC  15V
   VEE  0  4  DC  15V
*  Input signal source
   Vi  6  0  SIN (0  2  1KHZ)
*  Output
   .TRAN  .001MS  3MS  1MS  .001MS
   .PROBE
   .END
```

* In order to study the response with zener diodes connected at the output, modify the program listing by removing stars(*) against diodes D_1 and D_2.

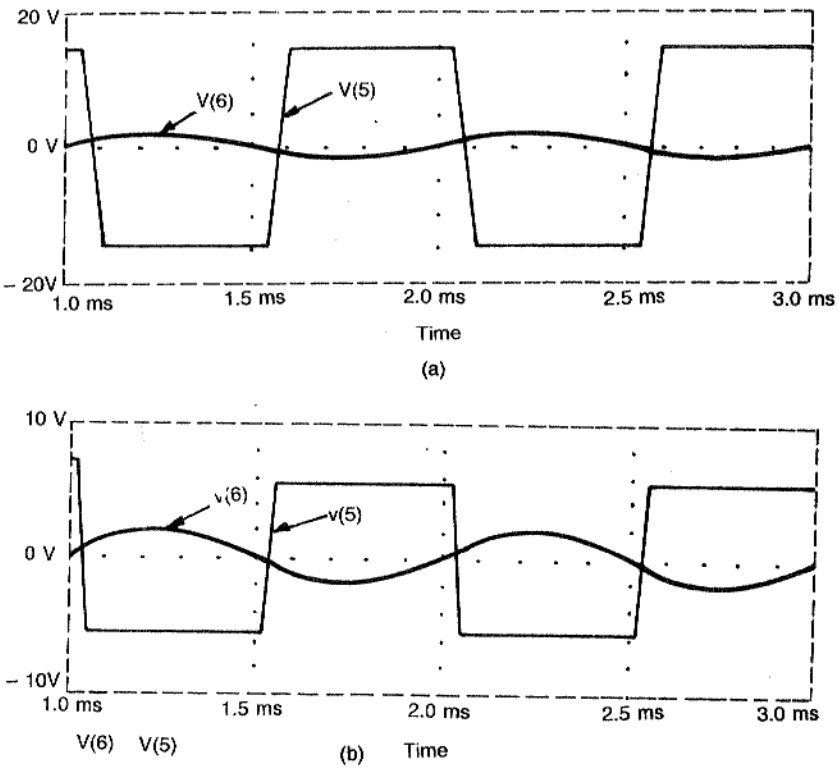


Fig. C. 5.1 Response of Schmitt trigger (a) without zener diodes (b) with zener diodes

Experiment 5.2

Design a square wave oscillator for f_o = 1 kHz and study its performance. Use a 741 op-amp and dc supply voltage = ± 12V.

Design

In the circuit shown in Fig. 5.10(a), use $R_1 = 1.16\ R_2$ so that the frequency of oscillation f_o is given by,

$$f_o = \frac{1}{2RC}$$

Choose, $R_2 = 10\ \text{k}\Omega$,

Then $R_1 = (1.16)\ (10\ \text{k}\Omega) = 11.6\ \text{k}\Omega$

Take $$R = \frac{1}{2 f_o C} = \frac{1}{2(10^3)\,(0.05 \times 10^{-6})}$$

$$\simeq 10\ \text{k}\Omega$$

So, $R_2 = 10\ \text{k}\Omega$; $R_1 = 11.6\ \text{k}\Omega$ (take 20 kΩ potentiometer)

$R = 10\ \text{k}\Omega$ and $C = 0.05\ \mu\text{F}$

Procedure

1. Make a circuit as shown in Fig. 5.10 (a) with the values of components as obtained in the design.
2. See the output waveform (pin 6) and the capacitor voltage waveform (pin 2) on the oscilloscope and measure amplitude and frequency.
3. Plot these waveforms on a linear graph paper.
4. To get reduced peak amplitude of the square wave, connect two zener diodes (V_Z ~ 6V) at the output terminal as shown in Fig. 5.10(c).
5. See the output waveforms on a scope and plot the waveforms on a graph paper.

Computer Exercise

Verify the output waveforms of the square wave oscillator designed above using PSPICE.

Experiment 5.3

(a) To construct a phase shift oscillator for f_o = 500 Hz and study its operation.

(b) To construct a Wien bridge oscillator for f_o = 1000 Hz and study its operation.

Design equations and component values:

(a) Phase shift oscillator:

In Fig. 5.15,

$$f_o = \frac{1}{2\pi\sqrt{6}\,RC} \quad \text{and} \quad R_f \geq 29\ R_1$$

Choose $C = 0.1\ \mu\text{F}$,

Then $$R = \frac{1}{2\pi\,(500)\,(\sqrt{6})\,(10^{-7})} = 1.3\ \text{k}\Omega\ (\text{use } 1.5\ \text{k}\Omega)$$

To prevent loading, $R_1 \geq 10\,R$

Therefore, take $R_1 = 10\ R = 15\ \text{k}\Omega$

$R_f = 29\ R_1 = 29 \times 15\ \text{k}\Omega$

$= 435\ \text{k}\Omega$

(Use R_f = 500 kΩ potentiometer)

(b) Wien bridge oscillator:

In Fig. 5.16(a),

$$f_o = \frac{1}{2\pi\,RC} \quad \text{and} \quad R_f = 2R_1$$

Choose $C = 0.05\ \text{mF}$

So, $$R = \frac{1}{2\pi\,(1000)\,(0.05 \times 10^{-6})} = 3.1\ \text{k}\Omega$$

Take $R_1 = 10R = 30\ \text{k}\Omega$

and $R_f = 2R_1 = 60\ \text{k}\Omega$ (Use 100 kΩ pot)

Procedure

1. Set up the Phase shift oscillator of Fig. 5.15 with the values obtained in the design.
2. See the output waveform on an oscilloscope. Adjust R_f to obtain a sine wave output.
3. Measure the frequency of oscillator and voltage amplitude.
4. Repeat steps 1, 2 and 3 for the Wien bridge oscillator.

6

Voltage Regulator

6.1 INTRODUCTION

The function of a voltage regulator is to provide a stable dc voltage for powering other electronic circuits. A voltage regulator should be capable of providing substantial output current. Voltage regulators are classified as:

Series regulator
Switching regulator

Series regulators use a power transistor connected in series between the unregulated dc input and the load. The output voltage is controlled by the continuous voltage drop taking place across the series pass transistor. Since the transistor conducts in the active or linear region, these regulators are also called linear regulators. Linear regulators may have fixed or variable output voltage and could be positive or negative. The schematic, important characteristics, data sheet, short circuit protection, current fold-back, current boosting techniques for linear voltage regulators such as 78 XX series, 723 IC are discussed.

Switching regulators, on the other hand, operate the power transistor as a high frequency ***on/off*** switch, so that the power transistor does not conduct current continuously. This gives improved efficiency over series regulator. In Sec. 6.4 the principle of switching power supply and its advantages over linear type of voltage regulator are discussed.

6.2 SERIES OP-AMP REGULATOR

A voltage regulator is an electronic circuit that provides a stable dc voltage independent of the load current, temperature and ac line voltage variations. Figure 6.1 shows a regulated power supply using discrete components. The circuit consists of following four parts:

1. Reference voltage circuit
2. Error amplifier

3. Series pass transistor
4. Feedback network.

It can be seen from Fig. 6.1 that the power transistor Q_1 is in series with the unregulated dc voltage V_{in} and the regulated output voltage V_o. So it must absorb the difference between these two voltages whenever any fluctuation in output voltage V_o occurs. The transistor Q_1 is also connected as an emitter follower and therefore provides sufficient current gain to drive the load. The output voltage is sampled by the $R_1 - R_2$ divider and fed back to the (–) input terminal of the op-amp error amplifier. This sampled voltage is compared with the reference voltage V_{ref} (usually obtained by a zener diode). The output V_o' of the error amplifier drives the series transistor Q_1.

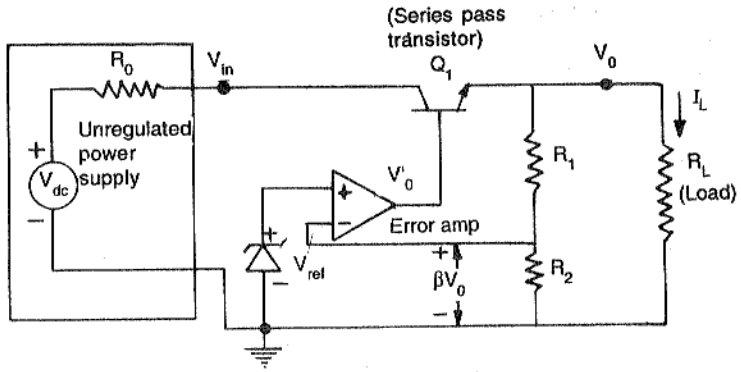


Fig. 6.1 A regulated power supply

If the output voltage increases, say, due to variation in load current, the sampled voltage βV_o also increases where

$$\beta \cong \frac{R_2}{R_1 + R_2} \tag{6.1}$$

This, in turn, reduces the output voltage V_o' of the diff-amp due to the 180° phase difference provided by the op-amp amplifier. V_o' is applied to the base of Q_1, which is used as an emitter follower. So V_o follows V_o', that is V_o also reduces. Hence the increase in V_o is nullified. Similarly, reduction in output voltage also gets regulated.

6.3 IC VOLTAGE REGULATORS

With the advent of micro-electronics, it is possible to incorporate the complete circuit of Fig. 6.1 on a monolithic silicon chip. This gives low cost, high reliability, reduction in size and excellent performance. Examples of monolithic regulators are 78XX/79XX series and 723 general purpose regulators.

6.3.1 Fixed Voltage Series Regulator

78XX series are three terminal, positive fixed voltage regulators. There are seven output voltage options available such as 5, 6, 8, 12, 15, 18 and 24 V. In 78XX, the last two numbers (XX) indicate the output voltage. Thus 7815 represents a 15 V regulator. There are also available 79XX series of fixed output, negative voltage regulators which are complements to the 78XX series devices. There are two extra voltage options of – 2 V and – 5.2 V available in 79XX series. These regulators are available in two types of packages.

Metal package (TO – 3 type)
Plastic package (TO – 220 type)

Figure 6.2 shows the standard representation of monolithic voltage regulator. A capacitor C_i (0.33 μF) is usually connected between input terminal and ground to cancel the inductive effects due to long distribution leads. The output capacitor C_o (1 μF) improves the transient response.

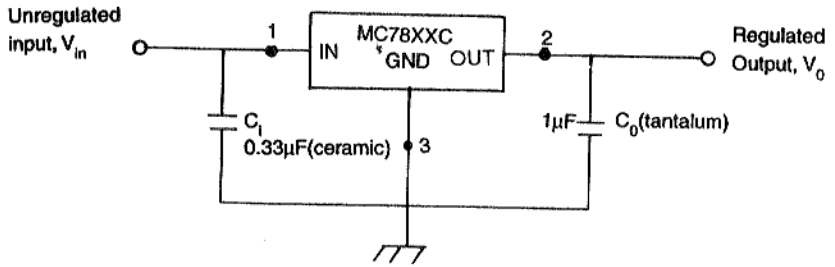


Fig. 6.2 Standard representation of a three terminal positive monolithic regulator

National Semiconductor also produce three terminal voltage regulators in LM series. There are three series available for different operating temperature ranges:

LM	100	series	– 55°C	to	+125°C
LM	200	series	– 25°C	to	+85°C
LM	300	series	0°C	to	+70°C

The popular series are LM 340 positive regulators and LM 320 negative regulators with output ratings comparable to 78XX/79XX series.

Characteristics

There are four characteristics of three terminal IC regulators which must be mentioned.

1. V_o : The regulated output voltage is fixed at a value as specified by the manufacturer. There are a number of models available for different output voltages, for example, 78XX series has output voltage at 5, 6, 8 etc.

2. $|V_{in}| \geq |V_o| + 2$ volts: The unregulated input voltage must be atleast 2 V more than the regulated output voltage. For example, if $V_o = 5$ V, then $V_{in} = 7$ V.
3. $I_{o(max)}$: The load current may vary from 0 to rated maximum output current. The IC is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.
4. Thermal shutdown: The IC has a temperature sensor (built-in) which turns off the IC when it becomes too hot (usually 125° C to 150°C). The output current will drop and remain there until the IC has cooled significantly.

Table 6.1 gives the electrical characteristics of 7805 voltage regulator and the connection diagram of packages available. Some of the important performance parameters listed in the data sheet are explained as follows:

Line/Input Regulation

It is defined as the percentage change in the output voltage for a change in the input voltage. It is usually expressed in millivolts or as a percentage of the output voltage. Typical value of line regulation from the data sheet of 7805 is 3 mV.

Load Regulation

It is defined as the change in output voltage for a change in load current and is also expressed in millivolts or as a percentage of V_o. Typical value of load regulation for 7805 is 15 mV for 5 mA < I_o < 1.5 A.

Ripple Rejection

The IC regulator not only keeps the output voltage constant but also reduces the amount of ripple voltage. It is usually expressed in dB. Typical value for 7805 is 78 dB.

The Schematic diagram of MC 78XXC* is shown in Fig. 6.3. The circuit consists of a reference voltage V_{ref} This circuit basically consists of level shifter with zener diode input and the transistor Q_9 used as emitter follower buffer. The circuit enclosed in the shaded region is a difference amplifier consisting of a current mirror (Q_4, Q_5), and an active load (Q_6, Q_7, Q_8). The combination of R_1R_2 forms the feedback network for sampling the output voltage. The sampled voltage is fed to one of the inputs of the difference amplifier. The Darlington pair Q' Q'' forms series pass element Q_1 of the circuit shown in Fig. 6.1.

*C stands for commercial use.

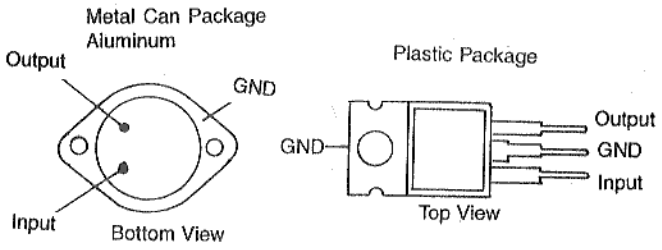
Table 6.1 Electrical characteristics of 7805 voltage regulator

Absolute Maximum Ratings	
Input Voltage (5 V through 18 V)	35 V
(24 V)	40 V
Internal Power Dissipation	Internally limited
Storage Temperature Range	−65°C to + 150°C
Operating Junction Temperature Range	
μA7800	−55°C to + 150°C
μA7800C	0°C to + 125°C

7805C

Electrical Characteristics V_{IN} = 10 V, I_{OUT} = 500 mA, 0°C ≤ T_j ≤ 125°C, C_{IN} = 0.33 μF, C_{OUT} = 0.1 μF, unless otherwise specified.

Characteristic	*Condition*	*Min*	*Typ*	*Max*	*Unit*
Output Voltage	T_j = 25°C	4.8	5.0	5.2	V
Line Regulation	T_j = 25°C, 7 V ≤ V_{IN} ≤ V		3	100	mV
	8 V ≤ V_{IN} ≤ 12 V		1	50	mV
Load Regulation	T_j = 25°C, 5 mA ≤ I_{OUT} ≤ 1.5 A		15	100	mV
	250 mA ≤ I_{OUT} ≤ 750 mA		5	50	mV
Output voltage	7 V ≤ V_{IN} ≤ 20 V, 5 mA ≤ I_{OUT} ≤ 1.0 A, P ≤ 15 W	4.75		5.25	V
Quiescent Current	T_j = 25°C		4.2	8.0	mA
Quiescent Current Change with line	7 V ≤ V_{IN} ≤ 25 V			1.3	mA
Quiescent Current Change with load	5 mA ≤ I_{OUT} ≤ 1.0 A			0.5	mA
Output Noise Voltage	T_A = 25°C, 10 Hz ≤ 1 ≤ 100 kHz		40		μV
Ripple Rejection	f = 120 Hz, 8 V ≤ V_{IN} ≤ 18 V	62	78		dB
Dropout Voltage	I_{OUT} = 1.0 A, T_j = 25°C		2.0		V
Output Resistance	f = 1 kHz		17		mΩ
Short-Circuit Current	T_j = 25°C. V_{IN} = 35 V		750		mA
Peak Output Current	T_j = 25°C		2.2		A
Average Temperature coefficient of output voltage	I_{OUT} = 5 mA, 0°C ≤ T_j ≤ 125°C		1.1		mV/°C



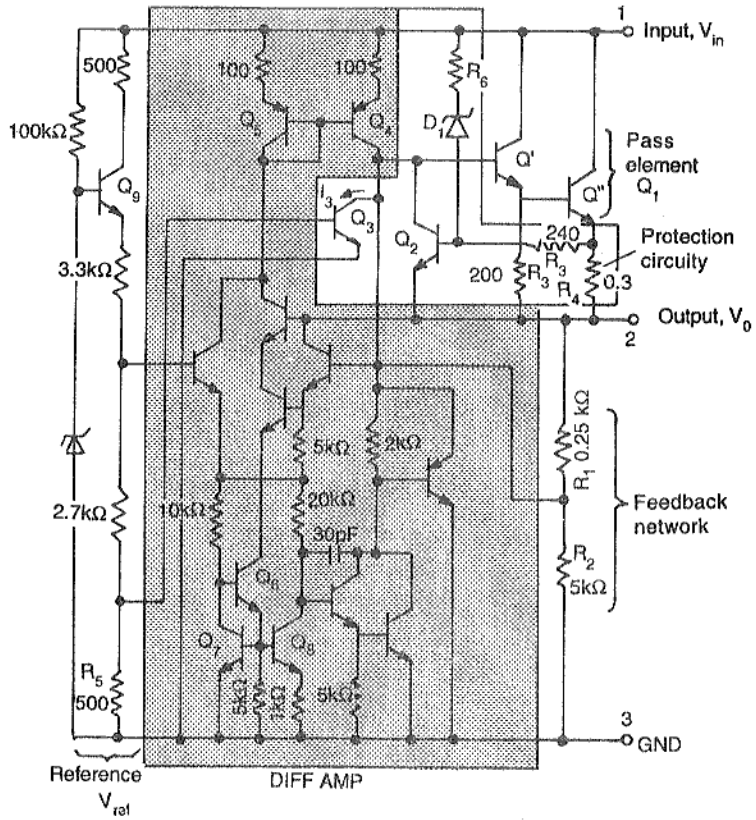


Fig. 6.3 Schematic diagram for MC 7800C series monolithic regulator

The monolithic regulator has in-built circuitry enclosed in the solid line to provide:

Over-current protection.

Thermal overload protection.

Current is limited by R_3, R_4 and transistor Q_2. If the output voltage goes low due to overload, the excess voltage appears across the pass element (Q' Q''), that is, across the collector emitter of Q''. When this voltage is more than the break-down voltage of the zener diode D_1, it starts conducting. This provides sufficient base current to transistor Q_2 and drives it ***on***. Now, because of the collector current of Q_2 when fully ***on***, current flowing to the base of Q' is reduced. This in turn reduces the conduction of Q''. Thus the volt-ampere product of the pass element (Q' Q'') is limited.

The thermal overload protection is provided by the resistor R_5 and transistor Q_3. The voltage drop across resistor R_5 is directly applied to the base-emitter of Q_3. When the temperature goes high, Q_3 conducts more, thereby reducing the base drive of $Q'Q''$ combination. This provides thermal protection.

Current Source

The three terminal fixed voltage regulator can be used as a current source. Figure 6.4(a) shows the circuit where 7805 has been wired to supply a current of 1 ampere to a 10 Ω, 10 watt load.

$$I_L = I_R + I_Q \tag{6.2}$$

where I_Q is the quiescent current and is about 4.2 mA for 7805. (See Table 6.1)

$$I_L = \frac{V_R}{R} + I_Q \tag{6.3}$$

Since I_L = 1A, $$\frac{V_R}{R} \simeq 1\text{A} \quad (I_Q << I_L) \tag{6.4}$$

Also V_R = 5 V (Voltage between terminal 2 and 3)

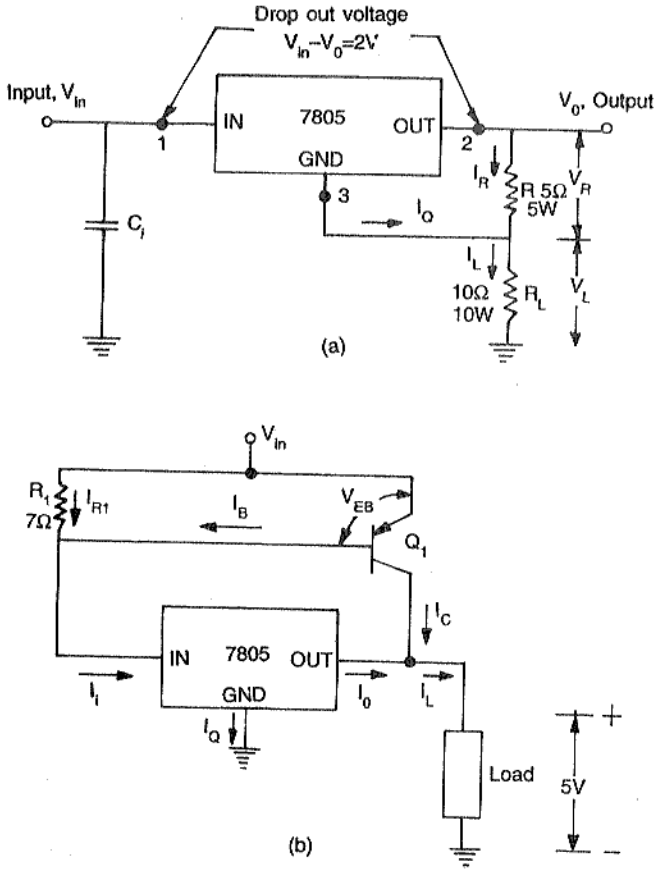


Fig. 6.4 (a) IC 7805 as a current source
(b) Boosting a three terminal regulator

So the value of R required is

$$R = 5\text{V}/1\text{A} = 5\Omega \tag{6.5}$$

Thus choose R = 5 Ω to deliver 1A current to a load of 10 Ω.

Boosting IC Regulator Output Current

It is possible to boost the output current of a three terminal regulator simply by connecting an external pass transistor in parallel with the regulator as shown in Fig. 6.4(b).

Let us now see how the circuit works. For low load currents, the voltage drop across R_1 is insufficient (< 0.7 V) to turn on transistor Q_1 and the regulator itself is able to supply the load current. However, as I_L increases, the voltage drop across R_1 increases. When this voltage drop is approximately 0.7V, the transistor Q_1 turns on. It can be easily seen that if I_L = 100 mA, the voltage drop across R_1 is equal to 7Ω × 100 mA = 0.7V. Thus, if I_L increases more than 100 mA, the transistor Q_1 turns on and supplies the extra current required. Since V_{EB} (ON) remains fairly constant, the excess current comes from Q_1's base after amplification by β. The regulator adjusts I_B so that

$$I_L = I_c + I_o \tag{6.6}$$

and $$I_c = \beta I_B \tag{6.7}$$

For the regulator,

$$I_o = I_i - I_Q \simeq I_i \text{ (as } I_Q \text{ is small)} \tag{6.8}$$

Also $$I_B = I_i - I_{R1} \simeq I_o - \frac{V_{EB\,(ON)}}{R_1} \tag{6.9}$$

Simplifying we get

$$I_L = (\beta + 1)\, I_o - \beta \frac{V_{EB\,(ON)}}{R_1} \tag{6.10}$$

The maximum current $I_{o\,(max)}$ for a 7805 regulator is 1A from the data sheet. Assuming $V_{EB\,(ON)}$ = 1V and β = 15 we get from Eq. (6.10)

$$I_L = 16 \times 1 - 15 \times (1/7) = 13.8 \text{ A} \tag{6.11}$$

Example 6.1

In Fig. 6.4(b), let $V_{EB\,(ON)}$ = 1 V and β = 15. Calculate the output current coming from 7805 and I_c coming from transistor Q_1 for loads 100Ω, 5Ω, 1Ω.

Solution

Load = 100Ω

For 7805, the output voltage across the load will be 5V.

$$I_L = 5V/100\Omega = 0.05A = 50 \text{ mA}$$

The voltage across R_1 is $7\Omega \times 50$ mA = 350 mV which is less than 0.7V. Hence Q_1 is ***off***.

So, $I_L = I_o = I_i = 50$ mA

and $I_c = 0$

Load = 5Ω

$$I_L = 5V/5\Omega = 1A$$

Assume that the entire current comes through regulator and that Q_1 is ***off***. Now the voltage drop across R_1 is equal to $7\Omega \times 1A = 7V$. Thus our assumption is wrong and Q_1 is ***on***. Putting the values in Eq. (6.10), it can be found that

$$I_o = 196 \text{ mA}$$

$$I_c = 904 \text{ mA}$$

Load = 1Ω

$$I_L = 5V/1\Omega = 5A$$

Here also Q_1 is ***on***. Solving Eq. (6.10) for I_o, we get

$$I_o = 446 \text{ mA}$$

so, $I_c = 4.55$ A

Fixed Regulator used as Adjustable Regulator

In the laboratory, one may need variable regulated voltages or a voltage that is not available as standard fixed voltage regulator. This can be achieved by using a fixed three terminal regulator as shown in Fig. 6.5. Note that the ground (GND) terminal of the fixed three terminal regulator is floating. The output voltage

$$V_o = V_R + V_{pot}$$

$$= V_R + (I_Q + I_{R1})\, R_2$$

$$= V_R + I_Q R_2 + \frac{V_R}{R_1} R_2$$

or, $$V_o = (1 + R_2/R_1)\, V_R + R_2 I_Q \qquad (6.12)$$

where V_R is the regulated voltage difference between the OUT and GND terminals. The effect of I_Q is minimized by choosing R_2 small enough to minimize the term $I_Q R_2$. The minimum output voltage is the value of the fixed voltage available from the regulator. The LM117,

217, 317 positive regulators and LM137, 237, 337 negative regulators have been specially designed to be used for obtaining adjustable output voltages. It is possible to adjust output voltage from 1.2 V to 40 V and current upto 1.5 A.

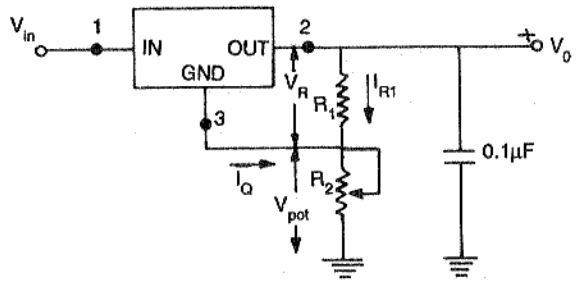


Fig. 6.5 Adjustable regulator

Example 6.2

Specify suitable component values to get $V_o = 7.5$V in the circuit of Fig. 6.5 using a 7805 regulator.

Solution

From the data sheet of 7805, $I_Q = 4.2$ mA. Say we choose $I_{R1} = 25$ mA.

As $V_R = 5$V for 7805,

$$R_1 = 5V/25 \text{ mA} = 200\,\Omega$$

We have to choose R_2 so as to develop a voltage of 2.5V across it. So,

$$R_2 = 2.5V/(I_{R1} + I_Q) = 2.5/(4.2 + 25) = 85.6\,\Omega$$

Choose $R_2 = 85\,\Omega$

Dual Voltage Supply

Many discrete and IC circuits (such as op-amp) require bipolar (dual or ± V) supplies. This can be easily done with two three-terminal regulators. Figure 6.6 shows a bipolar ± 15V supply that can give 1A from both (+) and (–) terminals. LM 340–15 is a +15V regulator with load current capability upto 1.5 A. The LM 320–15 is a –15V regulator. It may be noted that the pin configuration of LM 340 and LM 320 is different. The diodes D_1 and D_2 in the circuit protect the regulator against short circuit occurring at its input terminals. Diodes D_3 and D_4 provide protection against the situation when both the regulators may not turn on simultaneously. If there is a load between the two outputs, the faster one will try to reverse the polarity of the other and cause it to latch up unless it is properly clamped. This clamping function is done by the diodes. Once the regulator start operating

properly, both diodes will be reverse biased and will no longer have any effect on the circuit.

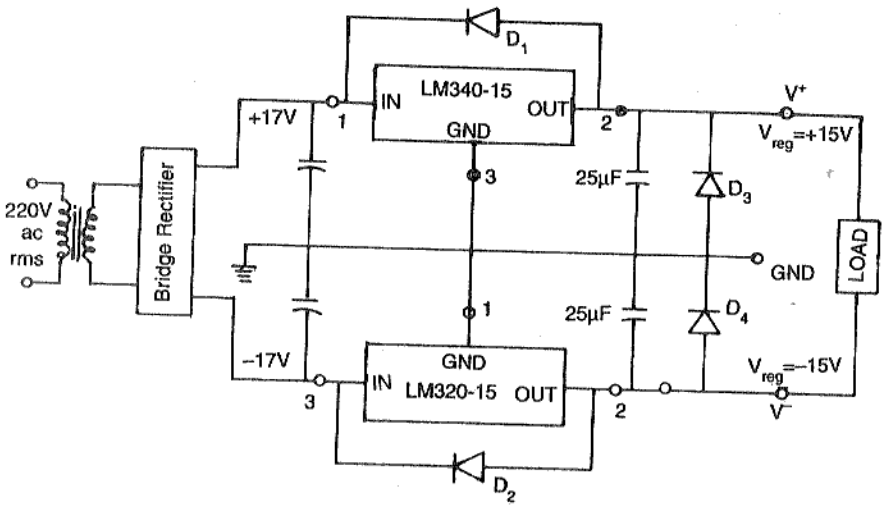


Fig. 6.6 A dual voltage (± 15V) supply

An op-amp draws less than 5 mA current, so a 100 mA supply can be used to drive a circuit consisting of 20 op-amps. LM 325H is a dual tracking ± 15V supply and is available in a 10-pin metal-can package and can furnish current upto 100 mA.

6.4 723 GENERAL PURPOSE REGULATOR

The three terminal regulators discussed earlier have the following limitations:

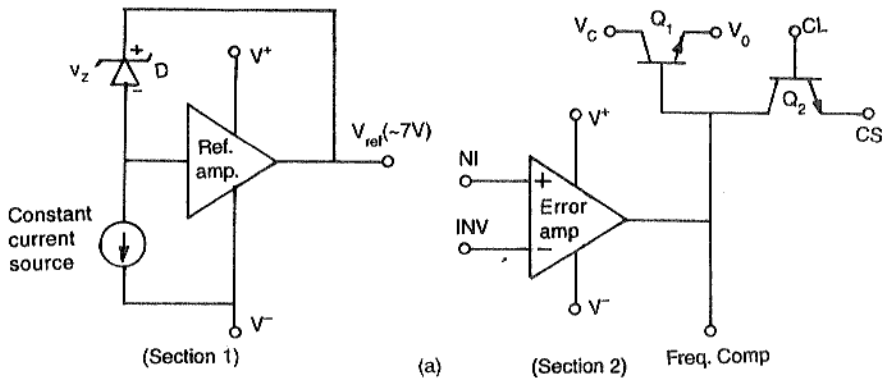
1. Not short circuit protection
2. Output voltage (positive or negative) is fixed.

These limitations have been overcome in the 723 general purpose regulator, which can be adjusted over a wide range of both positive or negative regulated voltage. This IC is inherently low current device, but can be boosted to provide 5 amps or more current by connecting external components. The limitation of 723 is that it has no in-built thermal protection. It also has no short circuit current limits.

Figure 6.7 (a) shows the functional block diagram of a 723 regulator IC. It has two separate sections. The zener diode, a constant current source and reference amplifier produce a fixed voltage of about 7 volts at the terminal V_{ref}. The constant current source forces the zener to operate at a fixed point so that the zener outputs a fixed voltage.

The other section of the IC consists of an error amplifier, a series pass transistor Q_1 and a current limit transistor Q_2. The error amplifier compares a sample of the output voltage applied at the INV input terminal to the reference voltage V_{ref} applied at the NI input terminal.

The error signal controls the conduction of Q_1. These two sections are not internally connected but the various points are brought out on the IC package. 723 regulated IC is available in a 14-pin dual-in-line package or 10-pin metal-can as shown in Fig. 6.7(b). The important features and electrical characteristics are given in Table 6.2.



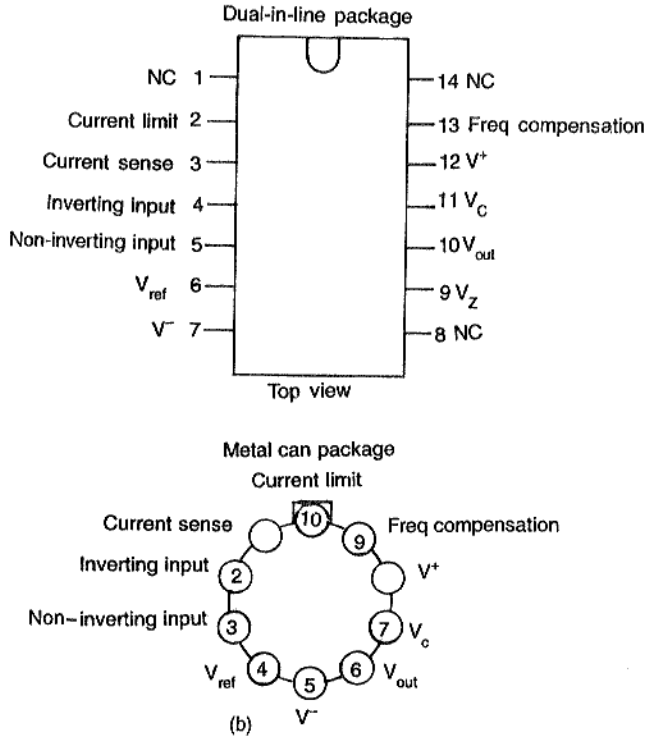


Fig. 6.7 (a) Functional block diagram of 723 regulator
(b) Pin diagram for 14-pin DIP and 10-pin metal can

Table 6.2 723 IC regulator electrical characteristics

723 Voltage Regulator								
Important Features:								
*Input voltage 40V max								
*Output voltage adjustable from 2V to 37V								
*150 mA output current without external pass transistor								
*Output currents in excess of 10A possible by adding external transistors								
*Can be used as either a linear or a switching regulator								
Parameter	*Conditions*	*LM723*			*LM723C*			*Units*
		Min	*Typ*	*Max*	*Min*	*Typ*	*Max*	
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		.01	0.1		.01	0.1	% V_o
	$-55°C \le T_A \le +125°C$			0.3				% V_o
	$0°C \le T_A \le +70°C$						0.3	% V_o
	V_{IN} = 12V to V_{IN} = 40V		.02	0.2		0.1	0.5	% V_o
Load Regulation	I_L = 1 mA to I_L = 50 mA		.03	0.15		.03	0.2	% V_o
	$-55°C \le T_A \le +125°C$			0.6				% V_o
	$0°C \le T_A \le +70°C$						0.6	% V_o
Ripple Rejection	f = 50Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5μF	86			86			dB
Average Temperature Coefficient of Output Voltage	$-55°C \le T_A \le +125°C$		.002	.015				%/°C
	$0°C \le T_A \le +70°C$					.003	.015	%/°C
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μV_{rms}
	BW = 100 Hz to 10 Khz, C_{REF} = 5μF	2.5			2.5			μV_{rms}
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{in} = 30 V		1.3	3.5		1.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	V
Input Output Voltage Differential		3.0		38	3.0		38	V

A simple positive low-voltage (2V to 7V) regulator can be made using 723 as shown in the schematic of Fig. 6.8(a). In order to understand the circuit operation, consider the detailed circuit of Fig. 6.8 (b). The voltage at the NI terminal of the error amplifier due to R_1R_2 divider is,

$$V_{NI} = V_{ref} \frac{R_2}{R_1 + R_2} \tag{6.13}$$

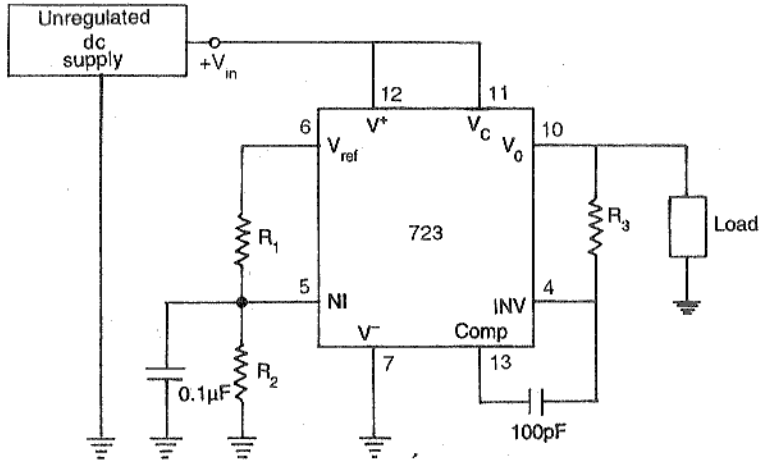


Fig. 6.8 (a) A low voltage regulator using 723 IC

The difference between V_{NI} and the output voltage V_o which is directly fed back to the INV terminal is amplified by the error amplifier. The output of the error amplifier drives the pass transistor Q_1 so as to minimize the difference between the NI and INV inputs of error amplifier. Since Q_1 is operating as an emitter follower

$$V_o = V_{ref} \frac{R_2}{R_1 + R_2} \tag{6.14}$$

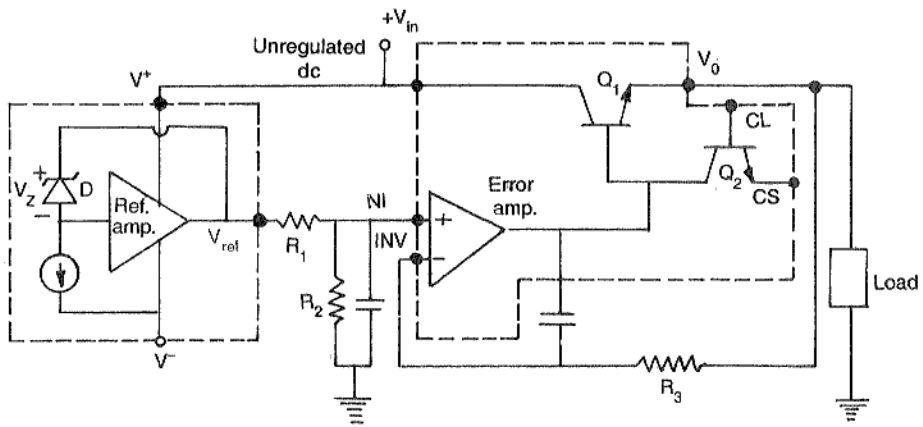


Fig. 6.8 (b) Functional diagram for a low voltage regulator
$V_{ref} \simeq 7V$, $V_o = V_{NI} = 7R_2/(R_1 + R_2)$, $V^+ = +V_{cc}$, $R_3 = R_1||R_2$ (minimum drift), $V^- = Gnd$

If the output voltage becomes low, the voltage at the INV terminal of error amplifier also goes down. This makes the output of the error

amp to become more positive, thereby driving transistor Q_1 more into conduction. This reduces the voltage across Q_1 and drives more current into the load causing voltage across load to increase. So the initial drop in the load voltage has been compensated. Similarly, any increase in load voltage, or changes in the input voltage get regulated.

The reference voltage is typically 7.15V. So the output voltage V_o is

$$V_o = 7.15 \times \frac{R_2}{R_1 + R_2} \tag{6.15}$$

which will always be less than 7.15V. So the circuit of Fig. 6.8(a) is used as low voltage (< 7V) 723 regulator.

If it is desired to produce regulated output voltage greater than 7V, then the circuit of Fig. 6.8(c) can be used. The NI terminal is connected directly to V_{ref} through R_3. So the voltage at the NI terminal is V_{ref}. The error amplifier operates as a non-inverting amplifier with a voltage gain of

$$A_v = 1 + \frac{R_1}{R_2} \tag{6.16}$$

So the output voltage for the circuit is

$$V_o = 7.15\left(1 + \frac{R_1}{R_2}\right) \tag{6.17}$$

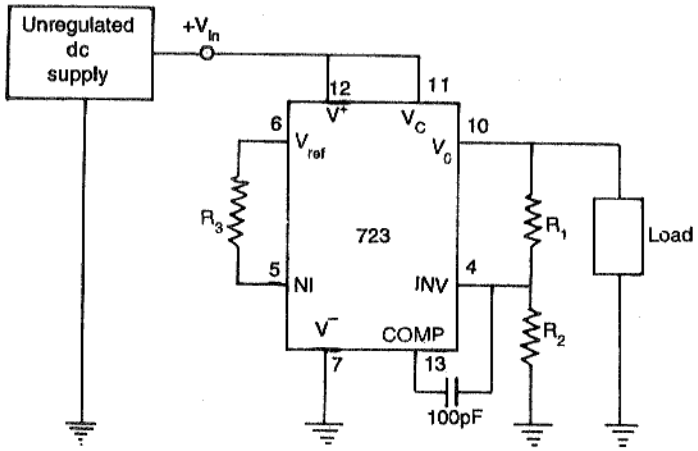


Fig. 6.8 (c) Basic high voltage 723 regulator
$V_{ref} = 7V$, $V_o = 7(1 + R_1/R_2)$, $R_3 = R_1R_2$, $V^+ = +V_{cc}$, $V^- = Gnd$

Current Limit Protection

The circuits of Fig. 6.8 have no protection. If the load demands more current e.g. under short circuit conditions, the IC tries to provide it

at a constant output voltage getting hotter all the time. This may ultimately burn the IC.

The IC is, therefore, provided with a current limit facility. Current limiting refers to the ability of a regulator to prevent the load current from increasing above a present value. The characteristic curve of a current limited power supply is shown in Fig. 6.9 (a). The output voltage remains constant for load current below I_{limit}. As current approaches the limit, the output voltage drops. The current limit I_{limit} is set by connecting an external resistor R_{sc} between the terminals *CL* and *CS* terminals as shown in Fig. 6.9(b). The *CL* terminal is also connected to the output terminal V_o and *CS* terminal to the load.

The load current produces a small voltage drop V_{sense} across R_{sc}. This voltage V_{sense} is applied directly across the base emitter junction of Q_2. When this voltage is approximately 0.5 volt, transistor Q_2 begins to turn ON. Now a part of the current from error amplifier goes to the collector of Q_2, thereby decreasing the base current of Q_1. This in turn, reduces the emitter current of Q_1. So any increase in the load current will get nullified. Similarly, if the load current decreases, V_{BE} of Q_2 drops, repeating the cycle in such a manner that the load current is held constant to produce a voltage across R_{sc} sufficient to turn ON Q_2. This voltage is typically 0.5 V.

So, $$I_{limit} = \frac{V_{sense}}{R_{sc}} \approx \frac{0.5\ V}{R_{sc}} \tag{6.18}$$

This method of current limiting is also referred to as current sensing technique.

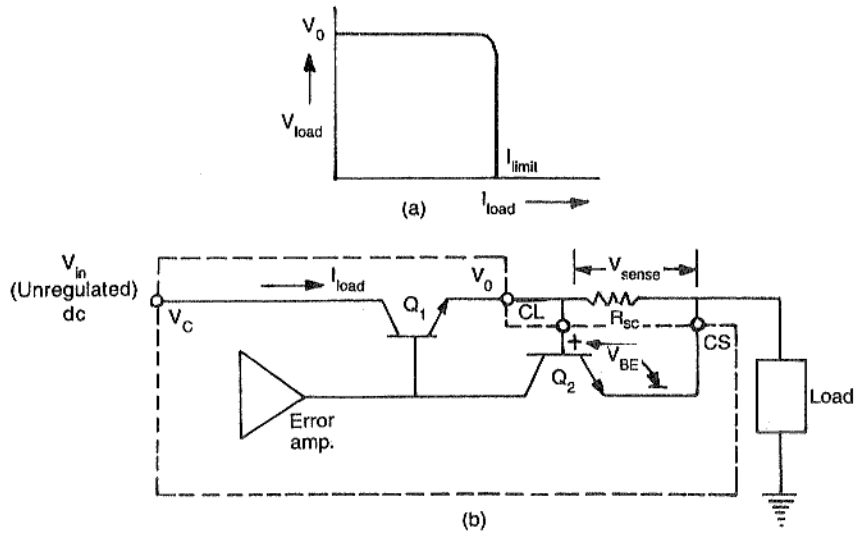


Fig. 6.9 (a) Characteristic curve for a current limited regulator
(b) Current limit protection circuit

Current Foldback

In current limiting technique, the load current is maintained at a present value and when overload condition occurs, the output voltage V_o drops to zero. However, if the load is short circuited, maximum current does flow through the regulator. To protect the regulator, one must devise a method which will limit the short circuit current and yet allow higher currents to the load.

Current foldback is the method used for this. Figure 6.10(a) shows the current foldback characteristic curve. As current demand increases, the output voltage is held constant till a present current level (I_{knee}) is reached. If the current demand exceeds this level, both output voltage and output current decrease. The circuit in Fig. 6.10(b) shows the method of applying current foldback. In order to understand the operation of the circuit, consider the circuit of Fig. 6.10(c). The voltage at terminal CL is divided by $R_3 - R_4$ network. The current limit transistor Q_2 conducts only when the drop across the resistance R_{sc} is large enough to produce a base-emitter voltage of Q_2 to be at least

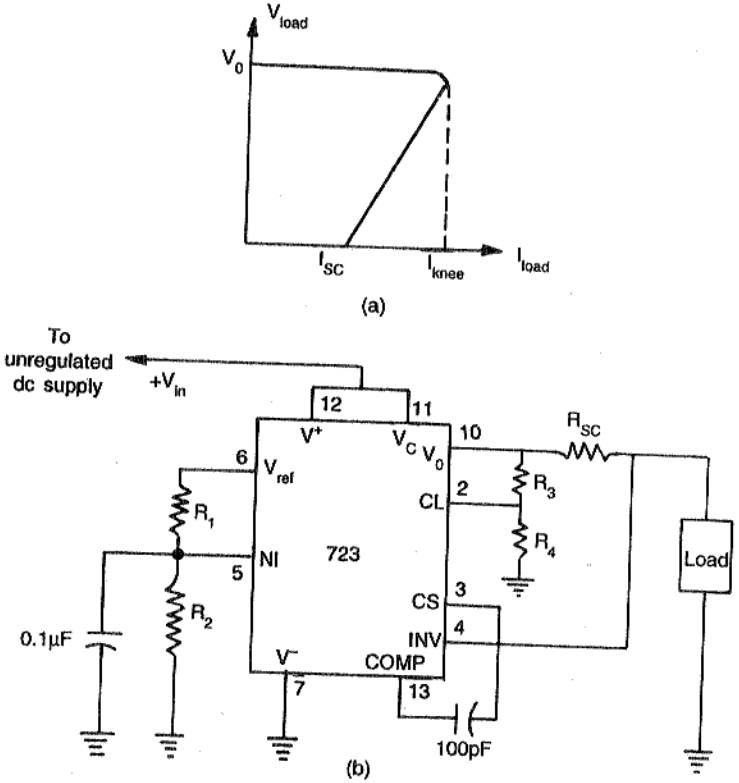


Fig. 6.10 (a) Current fold back characteristic curve (b) A low voltage regulator using current fold back

0.5 V. As Q_2 starts conducting, transistor Q_1 begins to turn off and the current I_L decreases. This reduces the voltage V_1 at the emitter of Q_1 and also the output voltage V_o. The voltage at the base of Q_2 (CL) will be $V_1R_4/(R_3 + R_4)$. Thus the voltage at the CL terminal drops by a smaller amount compared to the drop in voltage at CS terminal. This increases V_{BE} of Q_2 thereby increasing the conduction of Q_2, which in turn reduces the conduction of Q_1. That is, the current I_L further reduces. This process continues till $V_o = 0$V and V_1 is just large enough to keep 0.5V between CL and CS terminal. This point is I_{sc} and has been reduced by lowering both I_L and V_o.

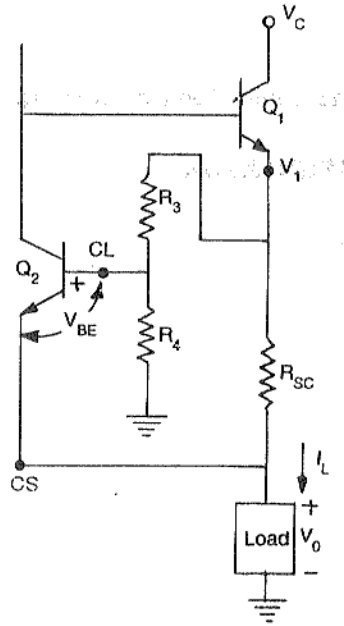


Fig. 6.10 (c) Current fold back (partial schematic)

Current Boosting

The maximum current that 723 IC regulator can provide is 140 mA. For many applications, this is not sufficient. It is possible to boost the current level simply by adding a boost transistor Q_1 to the voltage regulator as shown in Fig. 6.11. The collector current of the pass transistor Q_1 comes from the unregulated dc supply. The output current from V_o terminal drives the base of the pass transistor Q_1. This base current gets multiplied by the beta of the pass transistor, so that 723 has to provide only the base current. So,

$$I_{load} = \beta_{pass\ transistor} \times I_{o\ (723)} \qquad (6.19)$$

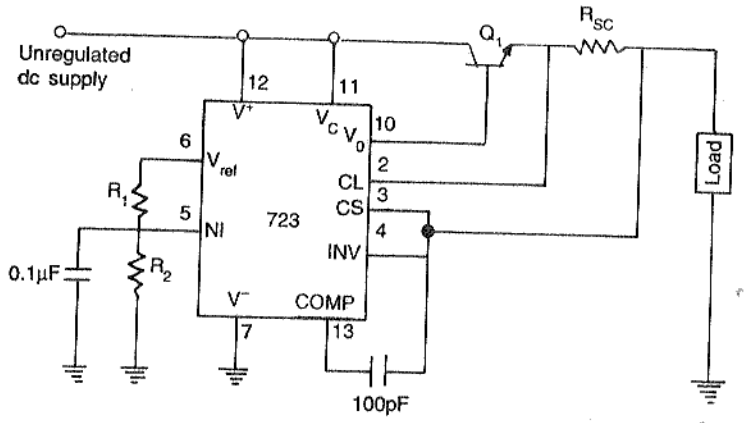


Fig. 6.11 Current boosted low voltage regulator

6.5 SWITCHING REGULATOR

The regulated power supplies discussed so far are referred to as linear voltage regulator, since the series pass transistor operates in the linear region. The linear voltage regulator has the following limitations.

The input stepdown transformer is bulky and the most expensive component of the linear regulated power supply mainly because of low line frequency (50 Hz). Because of the low line frequency, large values of filter capacitors are required to decrease the ripple. The efficiency of a series regulator is usually very low (typically 50 percent). The input voltage must be greater than the output voltage. The greater the difference in input-output voltage, more will be the power dissipated in the series pass transistor which is always in the active region. A TTL system regulator (V_o = 5V) when operated at 10V dc input gives 50 percent efficiency and only 25 percent for 20V dc input. Another limitation is that in a system with one dc supply voltage (such as + 5V for TTL) if there is need for ± 15V for op-amp operation, it may not be economically and practically feasible to achieve this.

Switched mode power supplies overcome these difficulties. The switching regulator, also called switched mode regulator operate in a significantly different way from that of a conventional series regulator circuit discussed earlier. In series regulator, the pass transistor is operated in its linear region to provide a controlled voltage drop across it with a steady dc current flow. Whereas, in the case of switched-mode regulator, the pass transistor is used as a "controlled switch" and is operated at either cutoff or saturated state. Hence the power transmitted across the pass device is in discrete pulses rather than as a steady current flow. Greater efficiency is achieved since the pass device is operated as a low impedance switch. When the pass device is at cutoff, there is no current and dissipates no power. Again when

the pass device is in saturation, a negligible voltage drop appears across it and thus dissipates only a small amount of average power, providing maximum current to the load. In either case, the power wasted in the pass device is very little and almost all the power is transmitted to the load. Thus efficiency in switched mode power supply is remarkably high–in the range of 70–90%.

Switched mode regulators rely on pulse width modulation to control the average value of the output voltage. The average value of a repetitive pulse waveform depends on the area under the waveform. If the duty cycle is varied as shown in Fig. 6.12, the average value of the voltage changes proportionally.

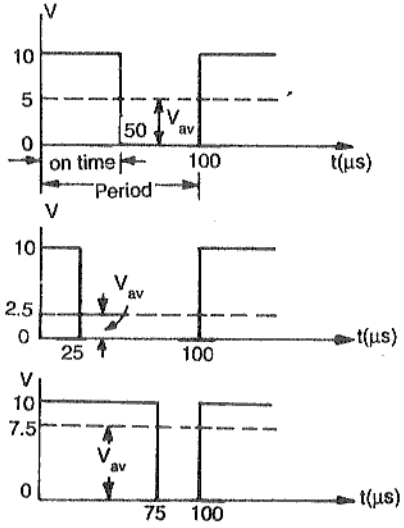


Fig. 6.12 Pulse width modulation and average value

A switching power supply is shown in Fig. 6.13. The bridge rectifier and capacitor filters are connected directly to the ac line to give unregulated dc input. The thermistor R_t limits the high initial capacitor charge current. The reference regulator is a series pass regulator of the type shown in Fig. 6.1. Its output is a regulated reference voltage V_{ref} which serves as a power supply voltage for all other circuits. The current drawn from V_{ref} is usually very small (~ 10 mA), so the power loss in the series pass regulator does not affect the overall efficiency of the switched mode power supply (SMPS). Transistors Q_1 and Q_2 are alternately switched ***off*** and ***on*** at 20 kHz. These transistors are either fully ***on*** ($V_{CE\ sat}$ ~ 0.2V) or cut-off, so they dissipate very little power. These transistors drive the primary of the main transformer. The secondary is centre-tapped and full wave rectification is achieved by diodes D_1 and D_2. This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage V_o.

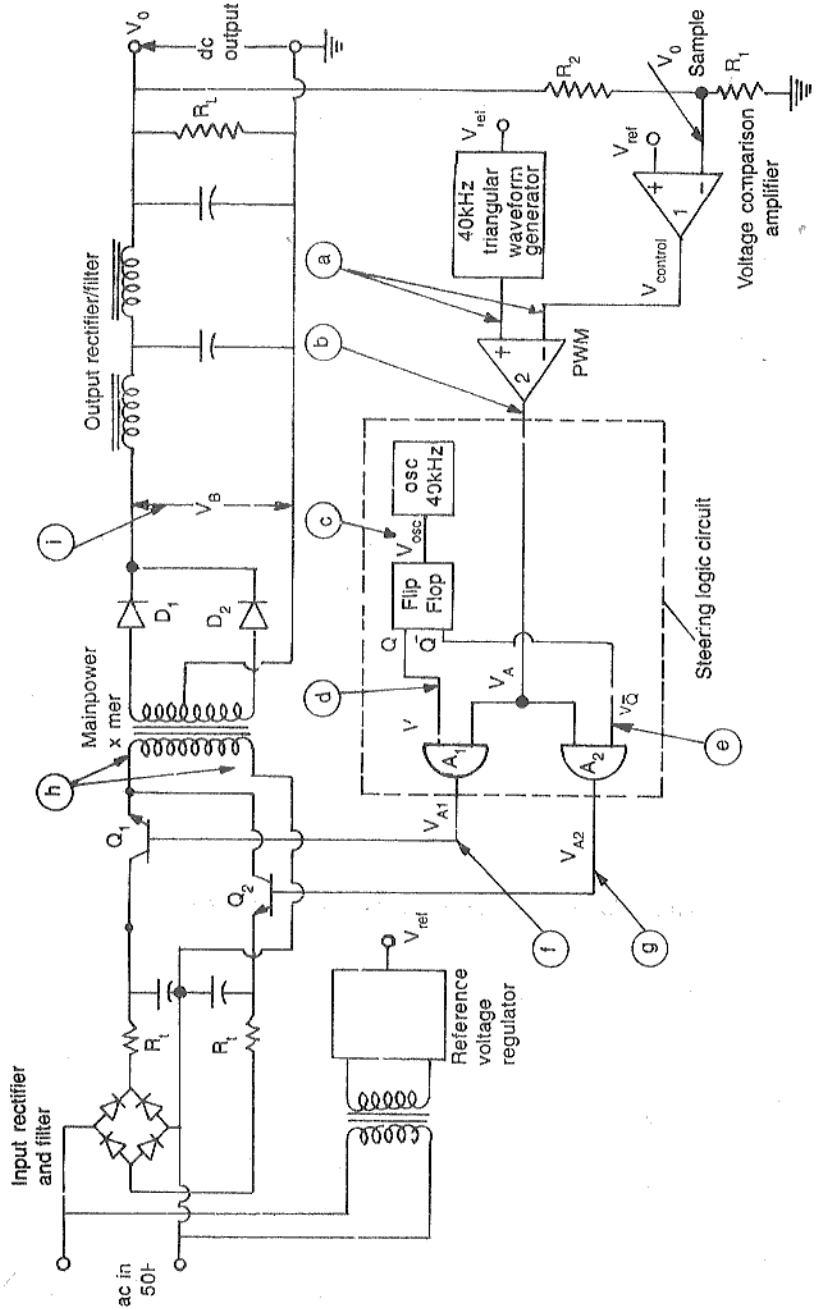


Fig. 6.13 A switched mode power supply

The regulation of V_o is achieved by the feedback circuit consisting of a pulse-width modulator and steering logic circuit. The output voltage V_o is sampled by a R_1R_2 divider and a fraction $R_1/(R_1+R_2)$ is compared with a fixed reference voltage V_{ref} in comparator 1. The output of this voltage comparison amplifier is called $V_{control}$ and is shown in Fig. 6.14 (a). $V_{control}$ is applied to the (–) input terminal of comparator 2 and a triangular waveform of frequency 40 kHz (also shown in Fig. 6.14 (a)) is applied at the (+) input terminal. It may be noted that a high frequency triangular waveform is being used to reduce the ripple. The comparator 2 functions as a pulse width modulator and its output is a square wave v_A (Fig. 6.14 (b)) of period $T(f = 40$ kHz). The duty cycle of the square wave is $T_1/(T_1 + T_2)$ and varies with $V_{control}$ which in turn varies with the variation of v_o. The output v_A drives a steering logic circuit shown in the dashed block. It consists of a 40 kHz oscillator cascaded with a flip-flop to produce two complementary outputs v_Q and $v_{\bar{Q}}$ shown in Fig. 6.14 (d) and (e). The output v_{A1} and v_{A2} of AND gates A_1 and A_2 are shown in Fig. 6.10 (f) and (g). These waveforms are applied at the base of transistor Q_1 and Q_2. Depending upon whether transistor Q_1 or Q_2 is ***on***, the waveform at the input of the transformer will be a square wave as shown in Fig. 6.14 (h). The rectified output v_B is shown in Fig. 6.14 (i).

An inspection of Fig. 6.13 shows that the output current passes through the power switch consisting of transistors Q_1 and Q_2, inductor having low resistance and the load. Hence using a switch with low losses (transistor with small $V_{CE\,(sat)}$ and high switching speed) and a filter with high quality factor, the conversion efficiency can easily exceed 90%.

If there is a rise in dc output voltage V_o, the voltage control $V_{control}$ of the comparator 1 also rises. This changes the intersection of the $V_{control}$ with the triangular waveform and in this case decreases the time period T_1 in the waveform of Fig. 6.14 (b). This in turn decreases the pulse width of the waveform driving the main power transformer. Reduction in pulse width lowers the average value of the dc output V_o. Thus the initial rise in the dc output voltage V_o has been nullified.

So far we have discussed the operation of the SMPS. Now we shall be able to justify why SMPS has better efficiency than linear regulated power supply. We have noted that very high frequency signals (about 40 kHz or more) are being applied. The transistors Q_1 and Q_2 are acting as the switches and become alternately ***on*** and ***off*** at a frequency of 20 kHz (Fig. 6.14 (a)). Again the transistor Q_1 or Q_2 is ***on*** for very small duration and consumes negligibly small power since $V_{CE\,(sat)}$ (0.2V) is small. It may also be noted that the high operating frequency used for the switching transistors allows the use of smaller transformers, capacitors and inductors. This allows a decrease in size and cost.

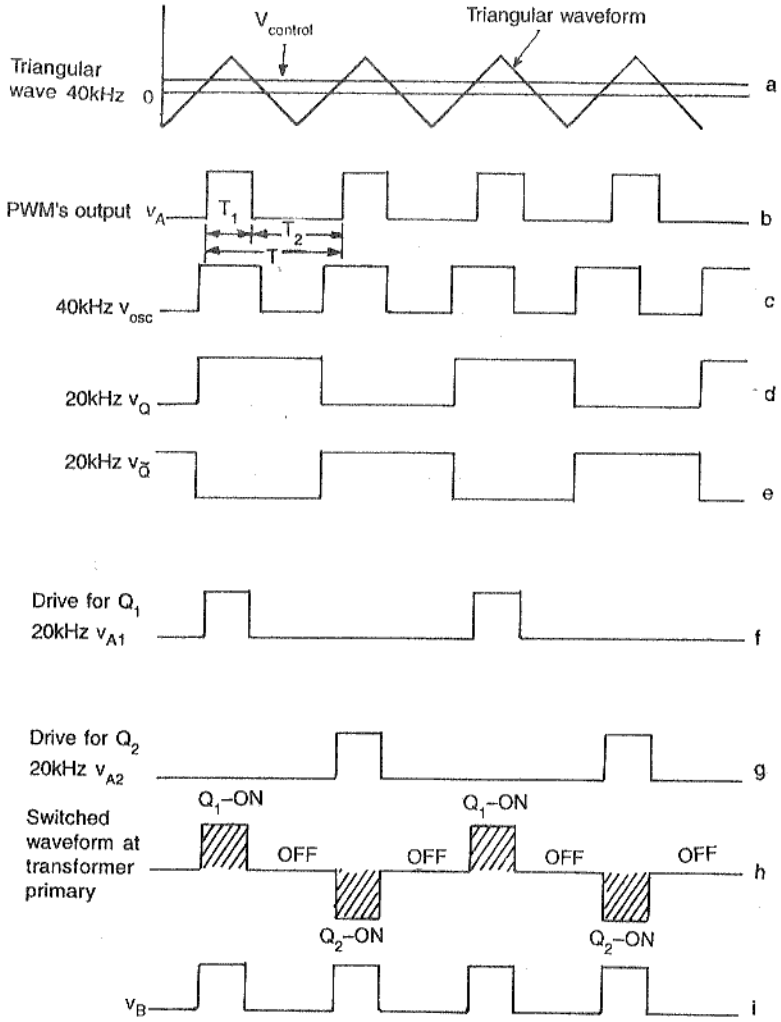


Fig. 6.14 Switching power supply waveforms

There are some limitations and precautions to be taken with switching power supplies. Since the rectifier is tied directly to the ac line voltage, the rectifiers, capacitors and switching transistors must be able to withstand the peak line voltage (310 V for 220 V ac rms line). The resistor R_t must be provided to prevent the uncharged capacitors from shorting out the line when initially turned on. A switched mode power supply is more complex and requires external components like inductors and transformers. It is slow in responding to transient load changes compared to the conventional series regulator. One should be careful about the electromagnetic and radio-frequency interference while using switched mode power supply.

As can be seen, the switching regulator system is quite a complex one. However, with modern microelectronics, quite a few packages are available. The Motorola MC 3420/3520 is a pulse width modulator IC chip. The Silicon General SG 1524 produces an IC package containing reference regulator, pulse width modulator (consisting of saw tooth oscillator and comparator), comparator 1, transistors Q_1 and Q_2, the steering flip-flop and two AND gates.

Summary

1. A regulated power supply provides a dc voltage independent of the load current, temperature and ac line voltage variations.
2. A regulated power supply has four parts: reference voltage circuit, error amplifier, a series-pass transistor and a feed back network.
3. There are several IC regulators available. 78 XX/79 XX series are three terminal positive and negative fixed voltage regulators.
4. The IC regulators combine the reference voltage source, error op-amp, pass transistor with short circuit current limiting and thermal overload protection.
5. The 723 regulator can give adjustable output voltage in a wide range. It provides short circuit protection and current foldback using external components. The basic regulator can be current boosted with an external pass transistor.
6. The switching power supply allows a decrease in size and cost. The pass transistors here are switched ON and OFF at 20 kHz or faster. The output level is controlled by varying the pulse width of the switching waveform. Operating at this frequency allows the use of smaller transformers, capacitors and inductors.

Review Questions

6.1. What is the function of a voltage regulator?
6.2. Give the important parts of a series regulated power supply using discrete components.
6.3. What is a voltage reference? Why is it needed?
6.4. What is the function of a series pass transistor?
6.5. What voltage options are available in 78XX and 79XX voltage regulators?
6.6. Show the standard representation of IC voltage regulator.
6.7. List and explain the characteristics of three terminal IC regulators.
6.8. Explain the important parameters listed in the data sheet of 78XX.
6.9. Explain the protections used in 78XX.
6.10. What are the limitations of three terminal regulator?
6.11. Draw the functional diagram of 723 regulator.
6.12. Explain the current limiting feature of 723 regulator.
6.13. Explain current foldback characteristics.

6.14. How is current boosting achieved in a 723 IC?
6.15. Discuss the limitations of linear voltage regulators.
6.16. What is the principle of switch-mode power supplies? Discuss its advantages and disadvantages.

PROBLEMS

6.1. Using 7805 design a current source to deliver 0.2 A current to a 22 Ω, 10 W load.
6.2. Design a voltage regulator using 723 to get a voltage output of 3V.

(Hint: See Fig. 6.8 (a), calculate R_1 and R_2)

6.3. Calculate the values of R_1 and R_2 for a high voltage 723 regulator of Fig. 6.8 (c) so as to get an output voltage of 28 volts.
6.4. Design a current limit circuit for a 723 regulator to limit the current to 60 mA.
6.5. Design an adjustable voltage regulator (3 volts to 28 volts) with a short circuit limit of 60 mA using a 723 regulator.
6.6. Design an adjustable regulator from the 7810 regulator to get an output voltage of 15V.

Experiment

(a) To study a fixed three terminal voltage regulator.
(b) To study the operation of 723 regulator *IC*.
(c) To study current foldback circuit.

Procedure (a)

(i) Connect a 7805 voltage regulator as shown in Fig. E. 6.1 (a)
(ii) Set the power supply voltage V_{in} to + 10 V dc. Measure and record the load current I_L and load voltage V_L for R_L: 220 Ω (1/4 W); 100 Ω (1/2 W); 22Ω (1 W); 22 Ω || 22 Ω = 11 Ω (each resistor 2 W). Calculate percent load regulation as the change in the load voltage V_L over some limited range of load current. Compare with the manufacturer's data.

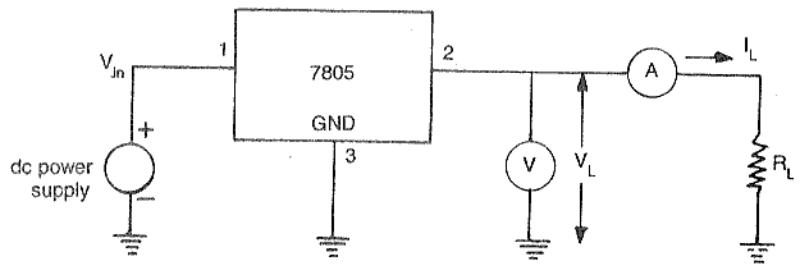


Fig. E. 6.1 (a) 7805 voltage regulator

(iii) To measure line regulation, connect the two 22Ω parallel resistors as load and measure the load voltage V_L for V_{in}: +7V dc, +12V dc, + 18V dc. Calculate line regulation as the percent change in output voltage for a change in the input voltage.
(iv) With V_{in} set to + 10V dc, short the output terminal of the regulator to ground with a piece of heavy wire just for moment. Observe the short circuit current. After removing the short circuit verify that the regulator still operates properly and gives a stable output voltage.

Procedure (b)

(i) Connect the 723 regulator as shown in Fig. E. 6.1. (b)

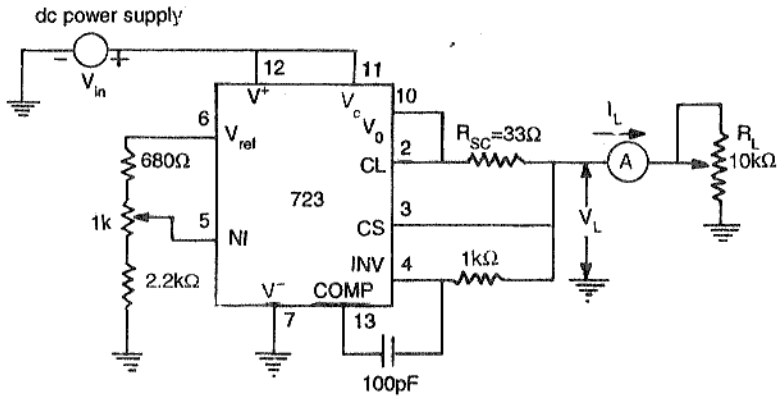


Fig. E. 6.1 (b) 723 voltage regulator

(ii) Set the dc power supply voltage V_{in} to + 10V. Measure and record V_{ref} with respect to ground. With load R_L (10 kΩ-pot) removed from the circuit (output open) measure the minimum and maximum output voltages by rotating the 1 kΩ-pot through its full range.
(iii) Now adjust the 1 kΩ-pot so that V_o is + 5V dc. Measure the voltage between the wiper arm of the 1 kΩ-pot and ground.
(iv) Adjust the load R_L (10 kΩ-pot) until the load current I_L = 1 mA. Record V_L. Repeat for different values of load currents; 5 mA, 10 mA, 15 mA and 18 mA. Calculate load regulation and compare with the manufacturer's specifications.
(v) Gradually increase the load current above 18 mA. You will see that the load voltage suddenly decreases when the load current is about 18 to 20 mA. Now the voltage across R_{sc} is enough to begin current limiting. Measure and record a few values of load current and load voltage below and above the current limiting point. Plot a graph of V_L versus I_L from the data obtained in steps (iv) and (v).

(vi) Replace R_L with a short circuit and measure the load current. This gives I_{sc}.

(vii) Make $R_{sc} = 0$. With $V_{in} = 10V$, measure and record I_L and V_L for I_L: 5 mA, 10 mA, upto $I_{L\,(max)}$ where $I_{L\,(max)}$ is 5 mA greater than the value of I_{sc} measured in step (vi).
Caution: Do not short circuit the output of the regulator. It is better to connect a 100 Ω resistor in series with R_L to avoid accidental short circuit.

(viii) With $R_{sc} = 0$, adjust R_L for a load current I_L of 1 mA. To determine line regulation, measure and record V_L for V_{in}: 10V, 15V, ... upto 35V in 5V increments. Calculate percent line regulation.

Procedure (c)

(i) Connect the current foldback circuit shown in Fig. E. 6.1. (c).

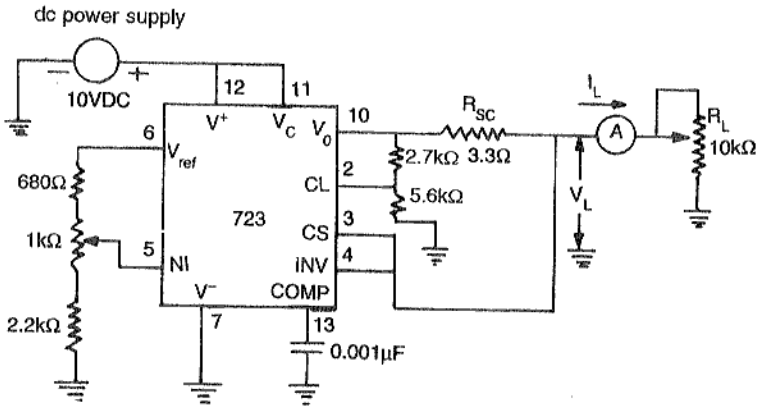


Fig. E. 6.1 (c) Current foldback circuit

(ii) Adjust R_L (10 kΩ-pot) and gradually increase the load current I_L until you observe a sudden reduction in V_L and I_L. The point at which this drop begins is the knee of the current foldback. By adjusting R_L, measure and record I_L and V_L in the vicinity of the knee and plot the current foldback characteristic. Measure V_{sc} across R_{sc} at the knee.

(iii) Replace R_L with a short circuit and record the short circuit load current.

7

Active Filters

7.1 INTRODUCTION

Electric filters are used in circuits which require the separation of signals according to their frequencies. Filters are widely used in communication and signal processing and in one form or another in almost all sophisticated electronic instruments. Such filters can be built from, (i) passive RLC components, (ii) crystals or (iii) resistors, capacitors and op-amps (active filters). In this chapter, we are discussing (i) RC active filters and (ii) switched capacitor filters. Further, active filters in its low-pass, high-pass, band-pass, band elimination configuration and state variable filter have been discussed.

7.2 RC ACTIVE FILTERS

A frequency selective electric circuit that passes electric signals of specified band of frequencies and attenuates the signals of frequencies outside the band is called an electric filter. Filters may be analog or digital. Our point of discussion, in this chapter, will be analog filters.

The simplest way to make a filter is by using passive components (resistors, capacitors, inductors). This works well for high frequencies, that is, radio frequencies. However, at audio frequencies, inductors become problematic, as the inductors become large, heavy and expensive. For low frequency application, more number of turns of wire must be used which in turn adds to the series resistance degrading inductor's performance, i.e. low Q, resulting in high power dissipation.

The active filters overcome the aforementioned problems of the passive filters. They use op-amp as the active element, and resistors and capacitors as the passive elements. The active filters, by enclosing a capacitor in the feedback loop, avoid using inductors. In this way, inductorless active RC filters can be obtained. Also, as op-amp is used in non-inverting configuration, it offers high input impedance and low output impedance. This will improve the load drive capacity and the

load is isolated from the frequency determining network. Because of the high input impedance of the op-amp, large value resistors can be used, thereby reducing the value (size and cost) of the capacitors required in the design.

The active filters have their limitation too. High frequency response is limited by the gain-bandwidth (GBW) product and slew rate of the op-amp. Moreover, the high frequency active filters are more expensive than the passive filters. The passive filter in high frequency range is a more economic choice for applications.

The most commonly used filters are:

Low Pass Filter	(LPF)
High Pass Filter	(HPF)
Band Pass Filter	(BPF)
Band Reject Filter	(also called Band Stop Filter) (BSF)

The frequency response of these filters is shown in Fig. 7.1, where dashed curve indicates the ideal response and solid curve shows the

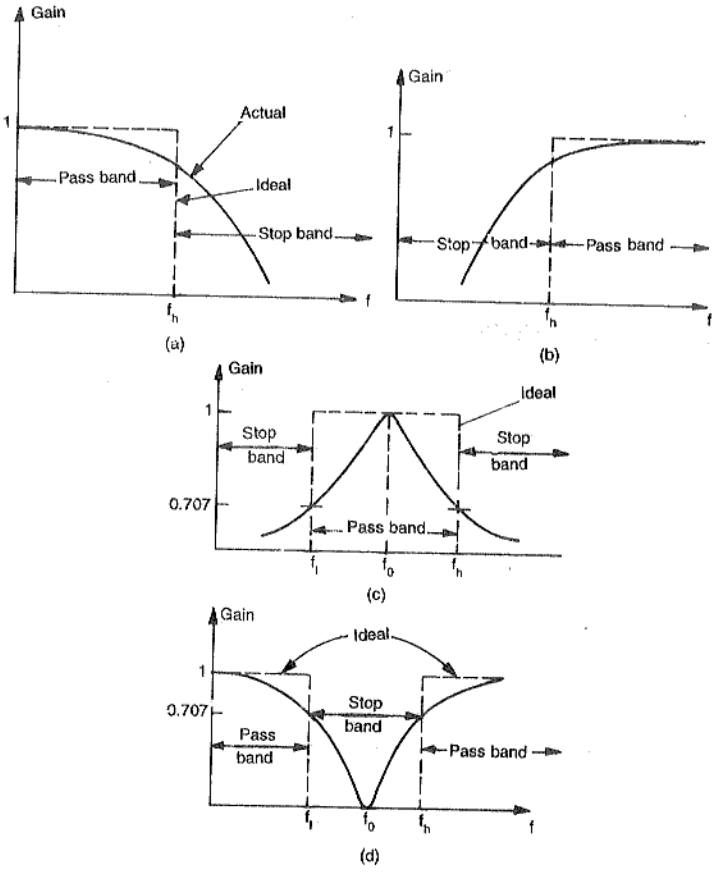


Fig. 7.1 Frequency response of filters (a) low-pass (b) high-pass (c) band pass (d) band reject

practical filter response. It is not possible to achieve ideal characteristics. However, with special design techniques it is possible to closely approximate the ideal response.

Active filters are typically specified by the voltage transfer function,

$$H(s) = \frac{V_o(s)}{V_i(s)}$$

Under steady state conditions, (i.e., $s = j\omega$)

$$H(j\omega) = |H(j\omega)| e^{j\phi(\omega)} \qquad (7.1)$$

where $|H(j\omega)|$ is the magnitude or the gain function and $\phi(\omega)$ is the phase function. Usually the magnitude response is given in dB as

$$20 \log |H(j\omega)| \qquad (7.2)$$

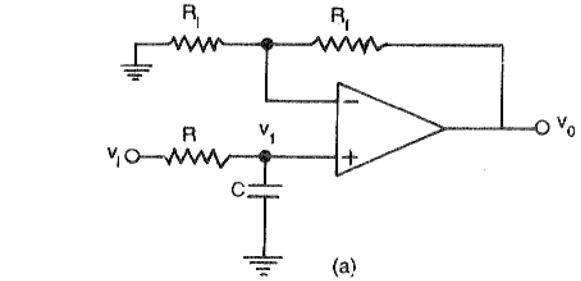
and the phase response is given in degrees as

$$-\phi(\omega) \times 57.296 \text{ degrees} \qquad (7.3)$$

Sometimes, active filters are specified by a loss function $V_i(s)/V_o(s)$. The use of loss function is a carry over from passive filter design.

7.2.1 First Order Low Pass Filter

Active filters may be of different orders and types. A first order filter consists of a single RC network connected to the (+) input terminal of a non-inverting op-amp amplifier and is shown in Fig. 7.2 (a). Resistors R_i and R_f determine the gain of the filter in the pass band.



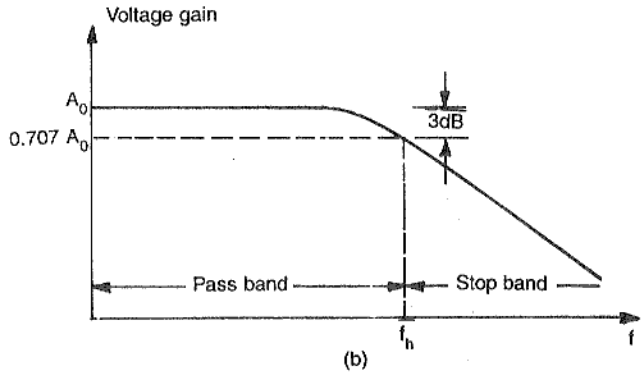


Fig. 7.2 (a) First order low-pass filter (b) Frequency response

The voltage v_1 across the capacitor C in the s-domain is

$$V_1(s) = \frac{\frac{1}{sC}}{R + \frac{1}{sC}} V_i(s)$$

so,
$$\frac{V_1(s)}{V_i(s)} = \frac{1}{RCs + 1} \tag{7.4}$$

where $V(s)$ is the Laplace transform of v in time domain.

The closed loop gain A_o of the op-amp is,

$$A_o = \frac{V_o(s)}{V_1(s)} = \left(1 + \frac{R_f}{R_i}\right) \tag{7.5}$$

So, the overall transfer function from Eq. (7.4) and (7.5) is

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{V_o(s)}{V_1(s)} \cdot \frac{V_1(s)}{V_i(s)} = \frac{A_o}{RCs + 1} \tag{7.6}$$

Let
$$\omega_h = \frac{1}{RC} \tag{7.7}$$

Therefore,
$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o}{\frac{s}{\omega_h} + 1} = \frac{A_o \omega_h}{s + \omega_h} \tag{7.8}$$

This is the standard form of the transfer function of a first order low-pass system.

To determine the frequency response, put $s = j\omega$ in Eq. (7.8). Therefore, we get

$$H(j\omega) = \frac{A_o}{1 + j\omega RC} = \frac{A_o}{1 + j(f/f_h)} \tag{7.9}$$

where
$$f_h = \frac{1}{2\pi RC} \text{ and } f = \frac{\omega}{2\pi}$$

At very low frequency, i.e. $f << f_h$

$$|H(j\omega)| \simeq A_o \tag{7.10}$$

At $f = f_h$,

$$|H(j\omega)| = \frac{A_o}{\sqrt{2}} = 0.707\, A_o \tag{7.11}$$

At very high frequency i.e. $f >> f_h$

$$|H(j\omega)| << A_o \simeq 0 \tag{7.12}$$

The frequency response of the first order low pass filter is shown in Fig. 7.2 (b). It has the maximum gain, A_o at $f = 0$ Hz. At f_h the gain falls to 0.707 time (i.e. –3 dB down) the maximum gain (A_o). The frequency range from 0 to f_h is called the pass band. For $f > f_h$ the gain decreases at a constant rate of –20 dB/decade. That is, when the frequency is increased ten times (one decade), the voltage gain is divided by ten or in terms of dBs, the gain decreases by 20 dB (= 20 log 10). Hence, gain rolls off at the rate of 20 dB/decade or 6 dB/octave after frequency, f_h. The frequency range $f > f_h$ is called the stop band. Obviously, the low pass filter characteristics obtained is not an ideal one as the rate of decay is small for the first order filter.

7.2.2 Second Order Active Filter

An improved filter response can be obtained by using a second order active filter. A second order filter consists of two RC pairs and has a roll-off rate of – 40 dB/decade. A general second order filter (Sallen-Key filter) is shown in Fig. 7.3. The results derived here can be used for analysing low pass and high pass filters.

The op-amp is connected as non-inverting amplifier and hence,

$$v_o = \left(1 + \frac{R_f}{R_i}\right) v_B = A_o v_B \tag{7.13}$$

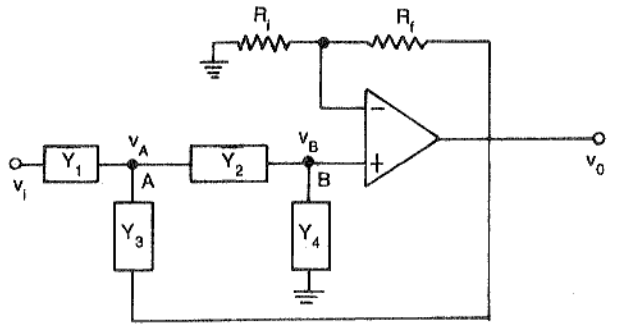


Fig. 7.3 Sallen-Key filter (General second order filter)

where
$$A_o = 1 + \frac{R_f}{R_i} \tag{7.14}$$

and v_B is the voltage at node B.

Kirchhoff's current law (KCL) at node A gives

$$v_i Y_1 = v_A(Y_1 + Y_2 + Y_3) - v_o Y_3 - v_B Y_2$$

$$= v_A (Y_1 + Y_2 + Y_3) - v_o Y_3 - \frac{v_o Y_2}{A_o} \tag{7.15}$$

where v_A is the voltage at node A.

KCL at node B gives,

$$v_A Y_2 = v_B(Y_2 + Y_4) = \frac{v_o(Y_2 + Y_4)}{A_o}$$

$$v_A = \frac{v_o(Y_2 + Y_4)}{A_o Y_2} \tag{7.16}$$

Substituting Eq. (7.16) in Eq. (7.15) and after simplification, we get the voltage gain as

$$\frac{v_o}{v_i} = \frac{A_o Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3 (1 - A_o)} \tag{7.17}$$

To make a low pass filter, choose, $Y_1 = Y_2 = 1/R$ and $Y_3 = Y_4 = sC$ as shown in Fig. 7.4. For simplicity, equal components have been used.

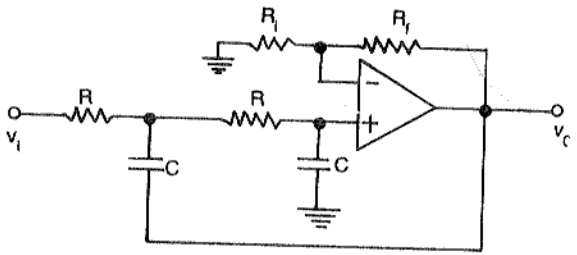


Fig. 7.4 Second order low-pass filter

From Eq. (7.17), we get the transfer function $H(s)$ of a low pass filter as,

$$H(s) = \frac{A_o}{s^2 C^2 R^2 + sCR(3 - A_o) + 1} \tag{7.18}$$

This is to note that from Eq. (7.18), $H(0) = A_o$ for $s = 0$ and $H(\infty) = 0$ for $s = \infty$ and obviously the configuration is for low pass active filter. It may be noted that for minimum dc offset $R_i R_f/(R_f + R_i) = R + R = 2R$ should be satisfied.

Second order physical systems have been studied extensively since long back and their step response, damping coefficient and its cause and effect relationship are known. We shall exploit those ideas in case of second order RC active filter. The transfer function of low pass second order system (electrical, mechanical, hydraulic or chemical) can be written as,

$$H(s) = \frac{A_o \omega_h^2}{s^2 + a\omega_h s + \omega_h^2} \tag{7.19}$$

where A_o = the gain
ω_h = upper cut-off frequency in radians/second
α = damping coefficient

Comparing Eq. (7.18) and Eq. (7.19) we get,

$$\omega_h = \frac{1}{RC} \tag{7.20}$$

$$\alpha = (3 - A_o) \tag{7.21}$$

That is, the value of the damping coefficient α for low pass active RC filter can be determined by the value of A_o chosen.

Putting $s = j\omega$ in Eq. (7.19) we get

$$H(j\omega) = \frac{A_o}{(j\omega/\omega_h)^2 + j\alpha(\omega/\omega_h) + 1} \tag{7.22}$$

the normalized expression for low pass filter is

$$H(j\omega) = \frac{A_o}{s^2 + \alpha s + 1} \tag{7.23}$$

where normalized frequency $s = j\left(\frac{\omega}{\omega_h}\right)$

The expression of magnitude in dB of the transfer function is,

$$20 \log |H(j\omega)| = 20 \log \left| \frac{A_o}{1 + j\alpha(\omega/\omega_h) + (j\omega/\omega_h)^2} \right|$$

$$= 20 \log \frac{A_o}{\sqrt{\left(1 - \frac{\omega^2}{\omega_h^2}\right)^2 + \left(\alpha \frac{\omega}{\omega_h}\right)^2}} \tag{7.24}$$

The frequency response for different values of α is shown in Fig. 7.5. It may be seen that for a heavily damped filter ($\alpha > 1.7$), the response is stable. However, the roll-off begins very early to the pass band. As α is reduced, the response exhibits overshoot and ripple begins to appear at the early stage of pass band. If α is reduced too much, the filter may become oscillatory. The flattest pass band occurs for damping coefficient of 1.414. This is called a Butterworth filter. Audio filters are usually Butterworth. The Chebyshev filters are more lightly damped, that is, the damping coefficient α is 1.06. However, this increases overshoot and ringing occurs deteriorating the pulse response. The advantage, however, is a faster initial roll-off compared to Butterworth. A Bessel filter is heavily damped and has a damping

coefficient of 1.73. This gives better pulse response, however, causes attenuation in the upper end of the pass band.

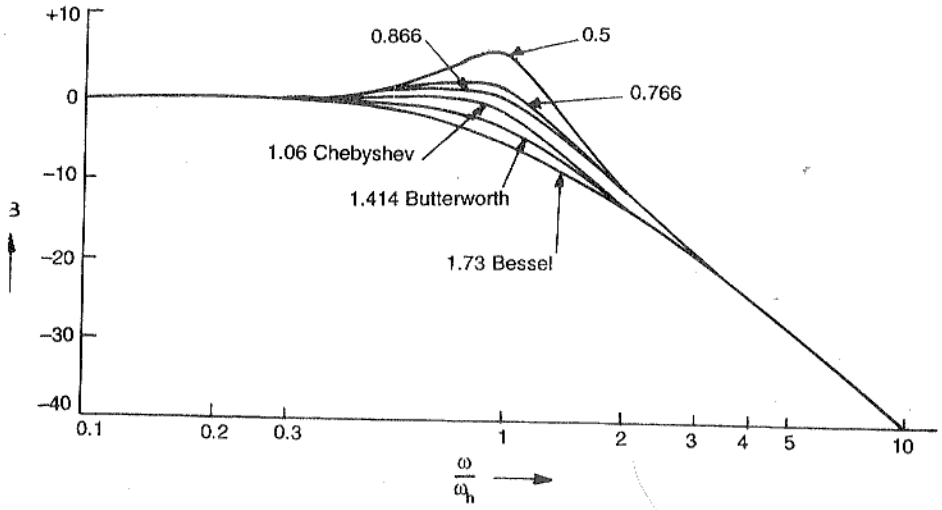


Fig. 7.5 Second order low-pass active filter response for different damping (unity gain $A_o = 1$)

We shall discuss only Butterworth filter in this text as it has maximally flat response with damping coefficient $\alpha = 1.414$. From Eq. (7.24), with $\alpha = 1.414$, we get

$$20 \log \left| H(j\omega) \right| = 20 \log \left| \frac{V_o}{V_i} \right| = 20 \log \frac{A_o}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^4}} \qquad (7.25)$$

Hence for n-th order generalized low-pass Butterworth filter, the normalized transfer function for maximally flat filter can be written as

$$\left| \frac{H(j\omega)}{A_o} \right| = \frac{1}{\sqrt{1 + \left(\frac{\omega}{\omega_h} \right)^{2n}}} \qquad (7.26)$$

7.2.3 Higher Order Low-Pass Filter

A second order filter can provide – 40 dB/decade roll-off rate in the stop band. To match with ideal characteristics, the roll-off rate should be increased by increasing the order of the filter. Each increase in order will produce – 20 dB/decade additional increase in roll-off rate,

as shown in Fig. 7.6. For n-th order filter the roll-off rate will be $-n \times 20$ dB/decade.

Higher order filters can be built by cascading a proper number of first and second order filters. The transfer function will be of the type,

$$H(s) = \underbrace{\frac{A_{o1}}{s^2 + \alpha_1 s + 1}}_{\text{second order section}} \cdot \underbrace{\frac{A_{o2}}{s^2 + \alpha_2 s + 1}}_{\text{another second order section}} \cdot \underbrace{\frac{A_o}{s + 1}}_{\text{first order section}}$$

Each term in the denominator has its own damping coefficient and critical frequency. Table 7.1 shows the denominator polynomials upto 8-th order Butterworth filter (see Appendix 7.1).

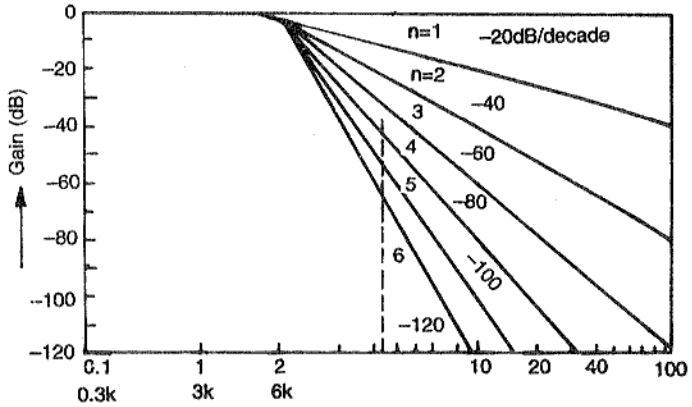


Fig. 7.6 Roll-off rate for different values of n

Table 7.1 Normalized Butterworth Polynomial

Order n	*Factors of polynomials*
1.	$s + 1$
2.	$s^2 + 1.414\ s + 1$
3.	$(s + 1)\ (s^2 + s + 1)$
4.	$(s^2 + 0.765\ s + 1)\ (s^2 + 1.848\ s + 1)$
5.	$(s + 1)\ (s^2 + 0.618\ s + 1)\ (s^2 + 1.618\ s + 1)$
6.	$(s^2 + 0.518\ s + 1)\ (s^2 + 1.414\ s + 1)\ (s^2 + 1.932\ s + 1)$
7.	$(s + 1)\ (s^2 + 0.445\ s + 1)\ (s^2 + 1.247\ s + 1)\ (s^2 + 1.802\ s + 1)$
8.	$(s^2 + 0.390 s + 1)\ (s^2 + 1.111\ s + 1)\ (s^2 + 1.663\ s + 1)\ (s^2 + 1.962\ s + 1)$

Example 7.1

Design a second order Butterworth low-pass filter having upper cut-off frequency 1 kHz. Then determine its frequency response.

Solution

Given f_h = 1 kHz = 1/2 π RC. Let C = 0.1 μF, gives the choice of R = 1.6 kΩ. From Table 7.1, for n = 2, the damping factor α = 1.414. Then the pass band gain A_o = 3 − α = 3 − 1.414 = 1.586. The transfer function of second order low-pass Butterworth filter is

$$\frac{1.586}{s^2 + 1.414\,s + 1}$$

Now $A_o = 1 + R_f/R_i = 1.586 = 1 + 0.586$. Let R_f = 5.86 kΩ and R_i = 10 kΩ. Then we get A_o = 1.586. The circuit realized is as in Fig. 7.4 with component values as R = 1.6 kΩ, C = 0.1 μF, R_f = 5.86 kΩ and R_i = 10 kΩ.

For minimum dc offset $R_i \parallel R_f = 2R$ (at dc condition, capacitors are open) which has not been taken into consideration here, otherwise, we would have to modify the values of R and C accordingly which comes out to be R = 1.85 kΩ, C = 0.086 μF, R_f = 5.86 kΩ, R_i = 10 kΩ.

The frequency response data is shown below using Eq. (7.25) and the frequency range is taken from 0.1 f_h to 10 f_h i.e., 100 Hz to 10 kHz as f_h = 1 kHz.

Frequency, f in Hz	Gain magnitude in dB $20 \log (v_o/v_i)$
100	4.00
200	4.00
500	3.74
1000	1.00
5000	−23.95
10000	−35.99

Example 7.2

Design a fourth order Butterworth low-pass filter having upper cut-off frequency 1 kHz.

Solution

The upper cut-off frequency, f_h = 1 kHz = 1/2π RC. Let C = 0.1 μF gives the choice of R = 1.6 kΩ. From Table 7.1, for n = 4, we get two damping factors namely, α_1 = 0.765 and α_2 = 1.848. Then the pass band gain of two quadratic factors are

$$A_{o1} = 3 - \alpha_1 = 3 - 0.765 = 2.235$$

$$A_{o2} = 3 - \alpha_2 = 3 - 1.848 = 1.152$$

The transfer function of fourth order low-pass Butterworth filter is

$$\frac{2.235}{s^2 + 0.765s + 1} \cdot \frac{1.152}{s^2 + 1.848s + 1}$$

Now, $$A_{o1} = 1 + \frac{R_{f1}}{R_{i1}} = 2.235 = (1 + 1.235)$$

Let R_{f1} = 12.35 kΩ and R_{i1} = 10 kΩ, then we get A_{o1} = 2.235
Similarly,

$$A_{o2} = 1.152 = 1 + 0.152 = 1 + \frac{R_{f2}}{R_{i2}}$$

Let R_{f2} = 15.2 kΩ and R_{i2} = 100 kΩ, which gives A_{o2} = 1.152.
The circuit realization is shown in Fig. 7.7.

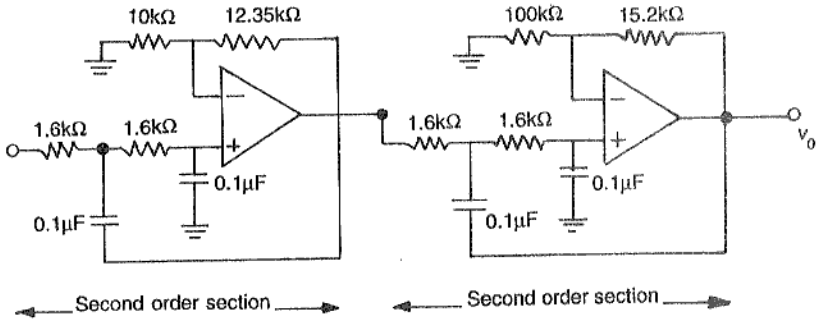


Fig. 7.7 Realization of 4-th order Butterworth low-pass filter

Example 7.3

Determine the order of a low-pas Butterworth filter that is to provide 40 dB attenuation at ω/ω_h = 2.

Solution

Use Eq. (7.26), then

$$20 \log \frac{H(j\omega)}{A_o} = -40 \text{ dB}$$

gives $$\frac{H(j\omega)}{A_o} = 0.01$$

so $$(0.01)^2 = \frac{1}{1 + 2^{2n}}$$

or, $$2^{2n} = 10^4 - 1$$

Solving for n, we get n = 6.64
Since the order of the filter must be an integer so, n = 7.

7.2.4 High Pass Active Filter

High pass filter is the complement of the low pass filter and can be obtained simply by interchanging R and C in the low pass configuration and is shown in Fig. 7.8. Putting $Y_1 = Y_2 = sC$ and $Y_3 = Y_4 = G = 1/R$ in the general Eq. (7.17), the transfer function becomes,

$$H(s) = \frac{A_0 s^2}{s^2 + (3 - A_0)\omega_\ell s + \omega_\ell^2} \qquad (7.27)$$

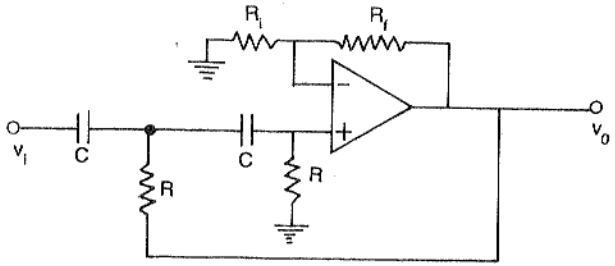


Fig. 7.8 Second order high pass filter

where $$\omega_\ell = \frac{1}{RC}$$

or, $$H(s) = \frac{A_0}{1 + \frac{\omega_\ell}{s}(3 - A_0) + \left(\frac{\omega_\ell}{s}\right)^2} \qquad (7.28)$$

From Eq. (7.28), for $\omega = 0$ we get $H = 0$ and for $\omega = \infty$, we get $H = A_0$. So the circuit indeed acts like high pass filter. The lower cut-off frequency

$$f_\ell = f_{3dB} = \frac{1}{2\pi RC}$$

and is same as in the low pass filter.

Putting $s = j\omega$ in Eq. (7.28) and $3 - A_0 = \alpha = 1.414$, the voltage gain magnitude equation of the second order Butterworth high pass filter can be obtained as

$$|H(j\omega)| = \left|\frac{V_o}{V_i}\right| = \frac{A_0}{\sqrt{1 + (f_\ell/f)^4}} \qquad (7.29)$$

Hence

$$\left|\frac{H(j\omega)}{A_0}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_\ell}{f}\right)^4}} \qquad (7.30)$$

As in the case of low pass filter, the generalized expression for n-th order maximally flat Butterworth ($\alpha = 1.414$) filter can be written as

$$\left|\frac{H(j\omega)}{A_0}\right| = \frac{1}{\sqrt{1 + \left(\frac{f_\ell}{f}\right)^{2n}}} \qquad (7.31)$$

Example 7.4

Design a second order Butterworth high pass filter having lower cut-off frequency 1 kHz.

Solution

Refer Example 7.1. The same data for cut-off frequency for Butterworth LPF has been taken so the vale of R and C will be the same. Also the values of R_f and R_i are as calculated in Example 7.1. Only the frequency response will have to be calculated using Eq. (7.29). The circuit configuration is as in Fig. 7.8 with component values $R = 1.6$. kΩ, $C = 0.1$ μF, $R_f = 5.86$ kΩ, $R_i = 10$ kΩ.

7.2.5 Band Pass Filter

There are two types of band pass filters which are classified as per the figure of merit or quality factor Q.

(i) Narrow band pass filter ($Q > 10$)
(ii) Wide band pass filter ($Q < 10$)

The following relationship are important

$$Q = f_o/BW = f_o/(f_h - f_\ell)$$

and $$f_o = \sqrt{f_h f_\ell}$$

where f_h = upper cut-off frequency
f_ℓ = lower cut-off frequency
f_o = the central frequency

Narrow Band Pass Filter

The important parameters in a band pass filter (BPF) are upper and lower cut-off frequencies (f_h and f_ℓ). the band width (BW), the central frequency (f_o), the central frequency gain A_o and selectivity Q. Consider the circuit of Fig. 7.9(a). The circuit has two feedback paths and the op-amp is used in inverting mode of operation.

The node voltage equation at node A is

$$v_i Y_1 + v_o Y_3 = v_A (Y_1 + Y_2 + Y_3 + Y_4) \qquad (7.32)$$

Assuming, $v_B = 0$ (virtual ground), the node voltage equation at node B is,

$$v_A Y_2 = -v_o Y_5$$

$$v_A = -v_o\,(Y_5/Y_2) \tag{7.33}$$

Putting v_A in Eq. (7.32), we get

$$v_i Y_1 + v_o Y_3 = -\frac{v_o Y_5 (Y_1 + Y_2 + Y_3 + Y_4)}{Y_2}$$

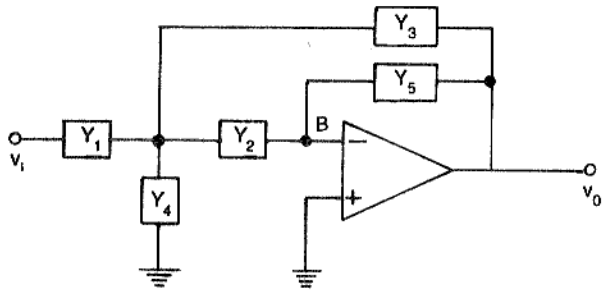


Fig. 7.9 (a) Band-pass configuration

or,
$$v_i Y_1 = v_o\left[-\frac{Y_2Y_3 + Y_1Y_5 + Y_2Y_5 + Y_3Y_5 + Y_4Y_5}{Y_2}\right]$$

Hence

$$\frac{v_o}{v_i} = -\frac{Y_1Y_2}{Y_2Y_3 + Y_1Y_5 + Y_2Y_5 + Y_3Y_5 + Y_4Y_5} \tag{7.34}$$

For this circuit to be band pass filter, put $Y_1 = G_1$, $Y_2 = sC_2$, $Y_3 = sC_3$, $Y_4 = G_4$ and $Y_5 = G_5$ as in Fig. 7.9 (b). Then the transfer function becomes,

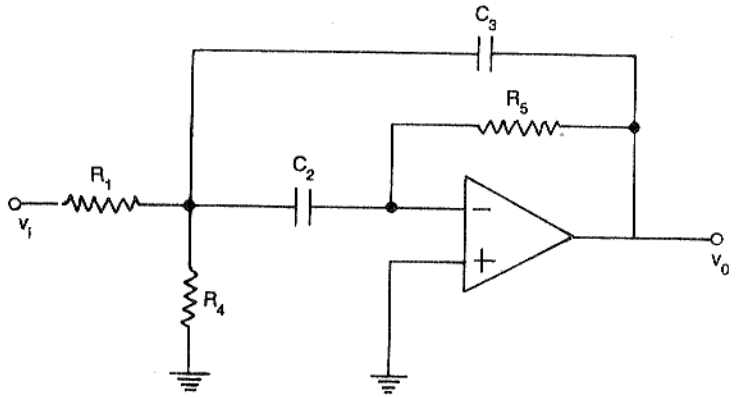


Fig. 7.9 (b) Second order band-pass filter

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{-sG_1C_2}{s^2C_2C_3 + s(C_2 + C_3)G_5 + G_5(G_1 + G_4)}$$

or,
$$H(s) = \frac{-G_1}{sC_3 + G_5(C_2 + C_3)/C_2 + (G_1 + G_4)G_5/sC_2} \tag{7.35}$$

The transfer function of Eq. (7.35) is equivalent to the gain expression of a parallel RLC circuit of Fig. 7.10(a) driven by a current source $G'v_i$ and with band pass characteristics as shown in Fig. 7.10 (b). The gain expression is,

$$\frac{V_o(s)}{V_i(s)} = -\frac{G'}{Y} = \frac{-G'}{sC + G + 1/sL} \tag{7.36}$$

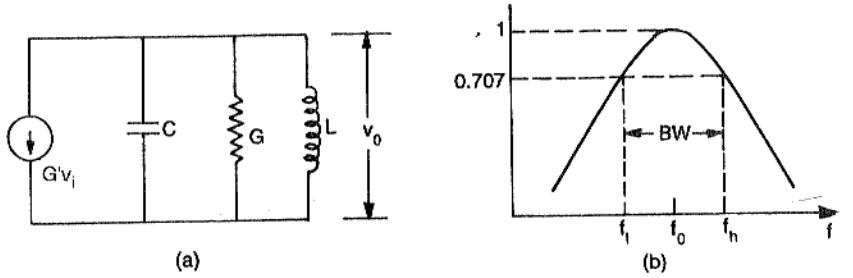


Fig. 7.10 (a) A parallel RLC circuit (b) Band-pass characteristics

Comparing the gain expression of Eq. (7.35) and Eq. (7.36), we get,

$$G' = G_1 \tag{7.37}$$

$$L = \frac{C_2}{G_5(G_1 + G_4)} \tag{7.38}$$

$$G = \frac{G_5(C_2 + C_3)}{C_2} \tag{7.39}$$

and
$$C = C_3 \tag{7.40}$$

At resonance, the circuit of Fig. 7.10(a) has unity power factor, i.e. imaginary part is zero which gives the resonant frequency ω_o as,

$$\omega_o^2 = \frac{1}{LC} = G_5\frac{(G_1 + G_4)}{C_2C_3} \tag{7.41}$$

The gain at resonance is,

$$\left.\frac{v_o}{v_i}\right|_{\omega = \omega_o} = -\frac{G'}{G} = -\frac{G_1}{G} = -\frac{(G_1/G_5)C_2}{C_2 + C_3}$$

$$= -\frac{(R_5/R_1)C_2}{C_2 + C_3} \tag{7.42}$$

The Q factor at resonance is,

$$Q_o = \frac{\omega_o L}{R} = \omega_o RC = \frac{\omega_o C}{G} = \frac{\omega_o C_2 C_3}{(C_2 + C_3) G_5} \tag{7.43}$$

The bandwidth BW is given by,

$$BW = f_h - f_\ell = \frac{f_o}{Q_o} = \frac{\omega_o}{2\pi Q_o} = \frac{\omega_o}{2\pi R \omega_o C}$$

$$= \frac{1}{2\pi RC} = \frac{G}{2\pi C} = \frac{G_5 (C_2 + C_3)}{2\pi C_2 C_3} \tag{7.44}$$

and the centre frequency $f_o = \sqrt{f_h f_\ell}$

Now for $C_2 = C_3 = C$, the gain at resonant frequency from Eq. (7.42) is,

$$\left.\frac{v_o}{v_i}\right|_{\omega = \omega_o} = -\frac{R_5}{2R_1} = -A_o \tag{7.45}$$

$$\omega_o = \frac{\sqrt{G_5 (G_1 + G_4)}}{C} \tag{7.46}$$

$$BW = \frac{G_5}{\pi C} = \frac{1}{\pi R_5 C} \tag{7.47}$$

We have three independent design parameter Eqs. (7.45), (7.46) and (7.47) for gain at resonance, resonant frequency and bandwidth. But there are four unknown parameters of the circuit such as C, G_1, G_4 and G_5. So we have to choose any one parameter arbitrarily.

Figure 7.11 shows a plot of frequency response for different values of Q. The higher the Q, the sharper the filter. Below 0.5 f_o and above 2 f_o, all filters roll-off at – 20 dB/decade independent of the value of Q. This is limited by the two RC pairs in the circuit. To obtain sharper roll-off rate away from the center frequency, one should cascade several filters.

It may further be noted that using Eqs. (7.43, 7.45, 7.46) in Eq. (7.35), the standard transfer function of a bandpass filter is obtained as,

$$H(s) = \frac{-A_o (\omega_o / Q) s}{s^2 + (\omega_o / Q)\, s + \omega_o^2} = \frac{-A_o \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2} \tag{7.48}$$

or, in dB, we get, $20 \log |H(s)| = 20 \log \left| \frac{A_o \alpha \omega_o s}{s^2 + \alpha\, \omega_o s + \omega_o^2} \right|$ (7.49)

where the damping factor $\alpha = \frac{1}{Q}$

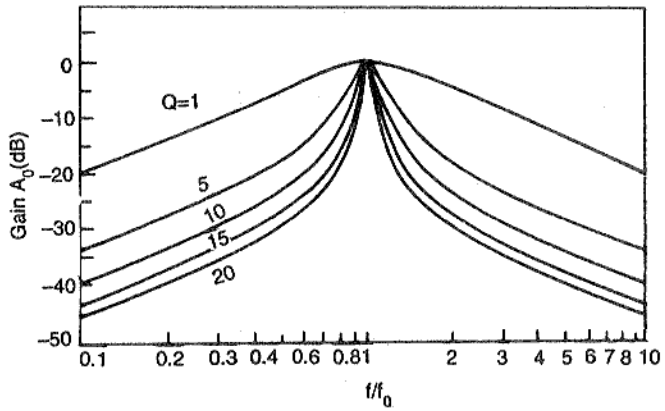


Fig. 7.11 Single op-amp band-pass filter response

It is obvious from Eq. (7.25) that for $\omega << \omega_o$ and $\omega >> \omega_o$ the gain is zero and for $\omega = \omega_o$ the gain is A_o. It may be noted that A_o is negative.

Wide Band-Pass Filter

A wide band-pass filter can be formed by cascading a HPF and LPF section. If the HPF and LPF are of the first order, then the band-pass filter (BPF) will have a roll-off rate of – 20 dB/decade.

For the high pass section of Fig. 7.12 the magnitude of gain is

$$|H_{HP}| = \left| \left(1 + \frac{R_f}{R_i}\right) \frac{j\, 2\pi f R_2 C_2}{1 + j 2\pi f R_2 C_2} \right|$$

$$= \left| A_{01} \frac{j(f/f_\ell))}{1 + j(f/f_\ell)} \right|$$

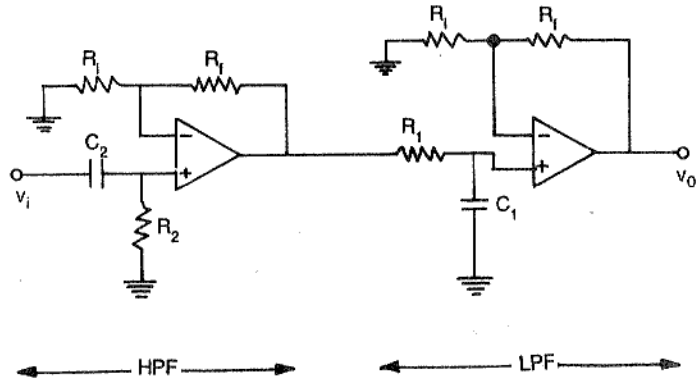


Fig. 7.12 First order band-pas filter

$$= \frac{A_{o1}\,(f/f_\ell)}{\sqrt{1+(f/f_\ell)^2}} \tag{7.50}$$

where $$f_\ell = \frac{1}{2\pi R_2 C_2} \tag{7.51}$$

Similarly, for the low-pass section of Fig. 7.12, the magnitude of gain is

$$|H_{LP}| = \frac{A_{o2}}{\sqrt{1+(f/f_h)^2}} \tag{7.52}$$

where $$f_h = \frac{1}{2\pi R_1 C_1} \tag{7.53}$$

The voltage gain magnitude of the wide band pass filter is the product of that of LPF and HPF. One can calculate the frequency response from the equation

$$\left|\frac{v_o}{v_i}\right| = \left|\frac{A_o\,(f/f_1)}{\sqrt{\left[1+(f/f_\ell)^2\right]\left[1+(f/f_h)^2\right]}}\right| \tag{7.54}$$

where the total pass band gain $A_o = A_{o1} \times A_{o2}$

In a similar fashion, to obtain BPF of – 40 dB/decade fall-off rate, second order HPF and LPF sections are to be cascaded.

Example 7.6

Design a wide-band pass filter having $f_\ell = 400$ Hz, $f_h = 2$ kHz and pass band gain of 4. Find the value of Q of the filter.

Solution

The pass band gain is 4. The LPF and HPF sections each of Fig. 7.12 may be designed to give gain of 2, that is, $A_o = 1 + R_f/R_i = 2$. So R_f and R_i should be equal. Let $R_f = R_i = 10$ kΩ for each of LPF and HPF sections.

For LPF, $f_h = 2$ kHz $= 1/2\,\pi\, R_1 C_1$. Let $C_1 = 0.01$ μF gives $R_1 = 7.9$ kΩ. For HPF, $f_\ell = 400$ Hz $= 1/2\,\pi\, R_2 C_2$. Let $C_2 = 0.01$ μF gives $R_2 = 39.8$ kΩ.

Again $f_o = \sqrt{f_h f_\ell} = \sqrt{2000 \times 400} = 894.4$

$$Q = f_o/BW = f_o/(f_h - f_\ell) = 894.4/(2000 - 400) = 0.56$$

Obviously, for wide band pass filter, Q is very low, i.e., $Q < 10$.

7.2.6 Band Reject Filter

A band reject filter (also called a band stop or band elimination) can be either (i) Narrow band reject or (ii) Wide band reject filter. The narrow band reject filter is commonly called a notch filter and is useful for the rejection of a single frequency, such as 50 Hz power line frequency hum.

There are several ways to make notch filters. One simple technique is to subtract the band pass filter output from its input. This principle is illustrated in Fig. 7.13 (a).

The band pass filter discussed earlier has an inverted output as the gain or transfer Eq. (7.35) is negative. Therefore, while implementing Fig. 7.13 (a), we must use a summer instead of a subtractor. Also, the band pass filter has a gain of A_o, so that output at the centre frequency will be $-A_o \times v_i$. To completely subtract this output, the input of the summer must be precisely $A_o v_i$. Thus, a gain of A_o must be added between the input signal and the summer as shown in Fig. 7.13(b). The output, of the circuit in the s domain is,

$$V_o(s) = A_o V_i(s) + \left(\frac{-A_o\,\alpha\,\omega_o s\, V_i(s)}{s^2 + \alpha\,\omega_o s + \omega_o^2}\right) \tag{7.55}$$

$$\frac{V_o(s)}{V_i(s)} = A_o - \frac{A_o\,\alpha\,\omega_o s}{s^2 + \alpha\,\omega_o s + \omega_o^2}$$

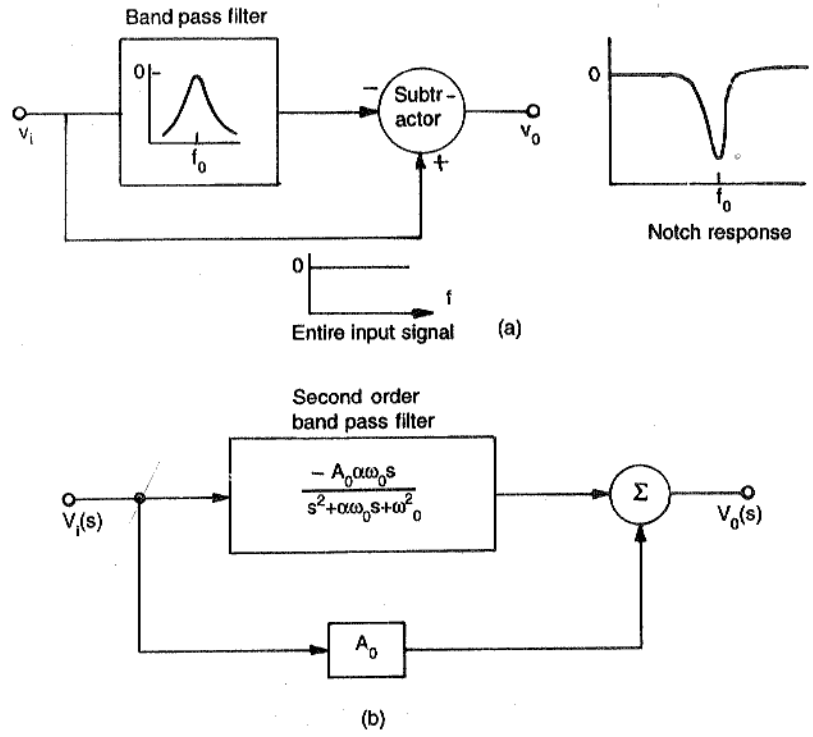


Fig. 7.13 (a) Notch filter block diagram (b) Practical notch filter block diagram

$$= A_0\left(1 - \frac{\alpha\,\omega_0 s}{s^2 + \alpha\,\omega_0 s + \omega_0^2}\right)$$

$$= \frac{A_0(s^2 + \omega_0^2)}{s^2 + \alpha\,\omega_0 s + \omega_0^2} \qquad (7.56)$$

This is the transfer function for a second order notch filter and the circuit schematic is shown in Fig. 7.14. It is evident from Eq. (7.56), that for $\omega << \omega_0$ and for $\omega >> \omega_0$ the pass band gain is $|A_0|$ and at frequency $\omega = \omega_0$ the gain is zero.

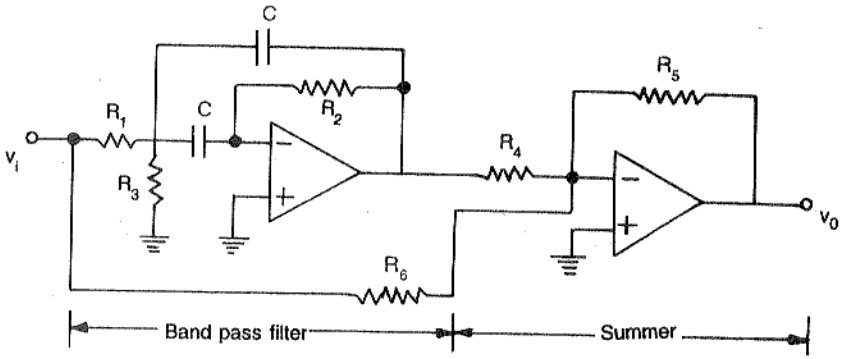


Fig. 7.14 Notch filter schematic

Another commonly used notch filter is the twin-T network as shown in Fig. 7.15(a). We will determine the notch frequency, Q factor and bandwidth for this configuration.

Node voltage equations in s-domain (by KCL) for the active filter circuit of Fig. 7.15(a) can be written as,

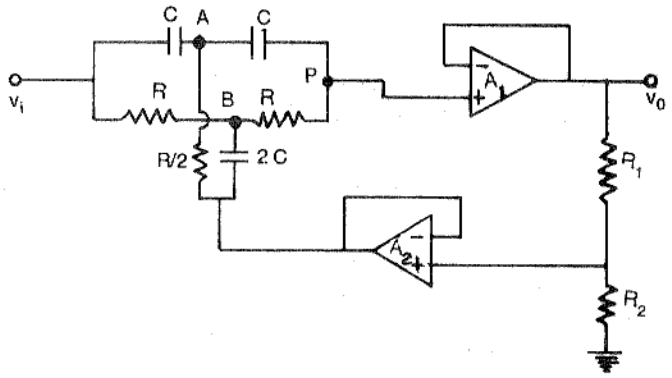


Fig. 7.15 (a) Twin-T notch filter

At node A: $(V_i - V_A)\,sC + (V_o - V_A)\,sC + (KV_o - V_A)2G = 0$

or, $$sC\,V_i + (sC + 2KG)\,V_o = 2\,(sC + G)\,V_A \qquad (7.57)$$

where V_A is the Laplace transform of the voltage at node A. Similarly V_i and V_o are transformed input and output. The s in the parenthesis has been dropped in the Laplace transform for simplicity.

At node B: $(V_i - V_B)G + (V_o - V_B)G + 2\,(KV_o - V_B)sC = 0$

or, $$GV_i + (G + 2\,KsC)\,V_o = 2(G + sC)V_B \qquad (7.58)$$

where V_B is the Laplace transform of the voltage at node B.

At node P: $(V_A - V_o)\,sC + (V_B - V_o)G = 0$

or, $$sC\,V_A + GV_B = (G + sC)V_o \qquad (7.59)$$

where, $K = R_2/(R_1 + R_2)$ and $G = 1/R$

From these node voltage equations, the transfer function can be written as,

$$H(s) = \frac{V_o}{V_i} = \frac{G^2 + s^2\,C^2}{G^2 + s^2C^2 + 4(1 - K)s\,CG}$$

$$= \frac{s^2 + (G/C)^2}{s^2 + (G/C)^2 + 4(1 - K)s\,(G/C)} \qquad (7.60)$$

In the steady state (i.e. $s = j\omega$),

$$H(j\omega) = \frac{\omega^2 - \omega_0^2}{\omega^2 - \omega_0^2 - j\,4\,(1 - K)\,\omega\,\omega_0} \qquad (7.61)$$

where, $\omega_0 = G/C = 1/RC$

i.e., $$f_o = \frac{1}{2\pi\,RC} \qquad (7.62)$$

From Eq. (7.61), $H(j\omega)$ becomes zero for $\omega = \omega_0$ and approaches unity as $\omega << \omega_0$ and for $\omega >> \omega_0$. In practice the high frequency response will be limited by the high frequency response of the op-amp. At 3-dB points, $|H| = 1/\sqrt{2}$

i.e. $$\omega^2 - \omega_0^2 = \pm\,4(1 - K)\,\omega\,\omega_0$$

or $$(\omega/\omega_0)^2 \pm 4(1 - K)\,(\omega/\omega_0) - 1 = 0 \qquad (7.63)$$

Solving the quadratic equation, we get the upper and lower half power frequencies as,

$$f_h = f_0\left[\sqrt{1 + 4(1 - K)^2} + 2\,(1 - K)\right] \qquad (7.64)$$

and $$f_\ell = f_0\left[\sqrt{1 + 4\,(1 - K)^2} - 2(1 - K)\right] \qquad (7.65)$$

The 3-dB bandwidth,

$$BW = f_h - f_\ell = 4(1 - K)f_o \tag{7.66}$$

$$Q = \frac{f_o}{BW} = \frac{1}{4(1-K)} \tag{7.67}$$

As K approaches unity, Q factor becomes very large and BW approaches 0. In fact, mismatches between resistors and capacitors limit the Q-factor and BW to practically realizable value. It is advisable to use the components of 0.1 percent tolerance resistors and 1 percent tolerance capacitors for very high value of Q-factor. The frequency response is shown in Fig. 7.15(b).

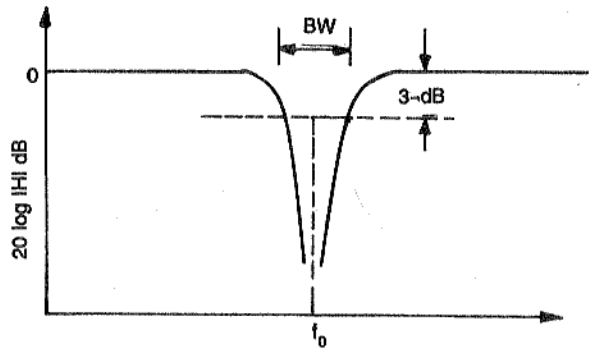


Fig. 7.15 (b) Frequency response of notch filter

Example 7.7

Design a 50 Hz active notch filter.

Solution

Given f_o = 50 Hz. Let C = 0.1 μF then from Eq. (7.62), we get R = $1/2\,\pi f_o C$ = 1/2 (3.14) (50) (10^{-7}) = 31.8 kΩ.

For $R/2$,. take two resistors of 31.8 kΩ in parallel and for $2C$, take two 0.1 μF capacitors in parallel to make the twin-T notch filter as shown in Fig. 7.15(a) where resistors R_1 and R_2 are for adjustment of gain.

Wide Band-Reject Filter

A wide band-reject filter (Q < 10) can be made using a LPF, HPF and a summer. It is of course necessary that (i) the lower cut off-frequency f_ℓ of the HPF should be much greater than the upper cut-off frequency f_h of the LPF and (ii) the pass band gain of LPF and HPF should be same.

Example 7.8

Design a wide band reject filter having f_h = 400 Hz and f_ℓ = 2 kHz having pass band gain as 2.

Solution

For HPF, f_ℓ = 2 kHz = $1/2\,\pi R_2 C_2$. Letting C_2 = 0.1 μF gives R_2 = 795 Ω (≈ 800 Ω). Again $A_o = A_{o2} = 2 = (1 + R_f/R_i)$ gives $R_f = R_i$ = 10 kΩ (say). For LPF, f_h = 400 Hz = $1/2\,\pi R_1 C_1$. Letting C_1 = 0.1 μF gives R_1 = 3978 Ω (choose 4 kΩ). Further $A_o = A_{o1} = 2 = (1 + R_f/R_i)$ gives $R_i = R_f$ = 10 kΩ (say). The schematic arrangement and the frequency response is shown in Figs. 7.16 (a, b).

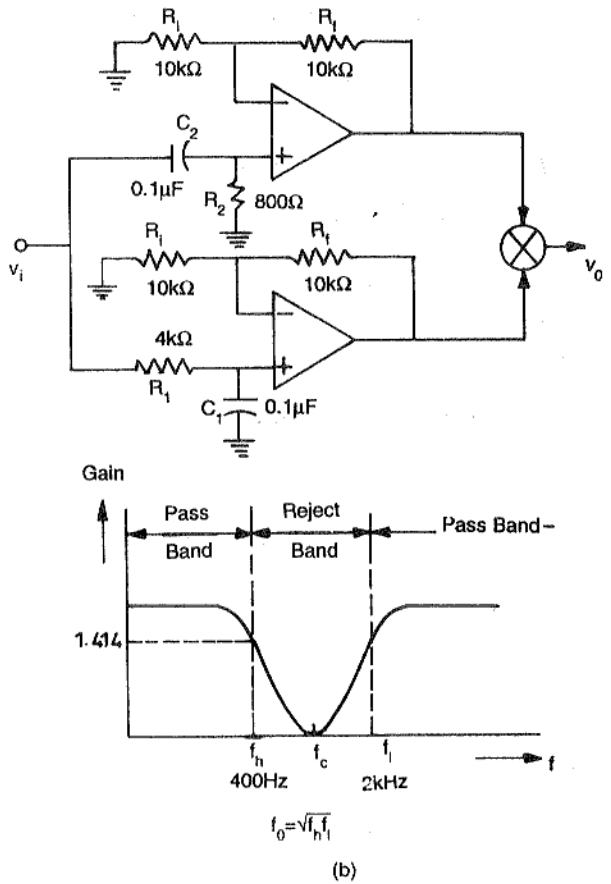


Fig. 7.16 (a) Wide band-reject filter (b) Frequency response

7.6 TRANSFORMATION

We shall now show that a high-pass, band-pass or band-reject filter can be obtained using an ideal low-pass transfer function by simple frequency transformation. For simplicity, let us normalize the frequency such that the cut-off frequency of the low pass function is unity. Let 'p' be the frequency domain of the low pass and 's' the frequency domain of interest.

Low-pass to High-pass Transformation

We get the high-pass characteristics by the following low-pass to high-pass transformation $p = 1/s$. For example, a third order Butterworth low-pass transfer function in p-domain given as

$$H(p) = \frac{A_o}{p^3 + 2p^2 + 2p + 1} \tag{7.68}$$

can be transformed to high-pass by the transformation $p = 1/s$ as

$$H(s) = \frac{A_o s^3}{s^3 + 2s^2 + 2s + 1} \tag{7.69}$$

The high-pass filter has the same pass band flatness as that of the Butterworth low-pass filter.

A low-pass filter can be transformed to a high-pass filter simply by interchanging R and C components and vice versa. A simple $RC : CR$ transformation is shown in Fig. 7.4 and Fig. 7.8. This is to note that the 3-dB (cut-off) frequency is the same for both the original low-pass and the transformed high-pass filter i.e., $f_{3\text{-dB}} = 1/2\,\pi RC$.

Low-pass to Band-pass Transformation

Consider a first order Butterworth low-pass transfer function in p-domain as

$$H(p) = \frac{A_o}{p + 1} \tag{7.70}$$

Let the transformation

$$p = \frac{s^2 + \omega_o^2}{(\omega_h - \omega_\ell)s} \tag{7.71}$$

In order to normalize, put

$$s_n = s/\omega_o \tag{7.72}$$

and quality factor, $$Q = \frac{\omega_o}{\omega_h - \omega_\ell}$$

Then Eq. (7.71) can be rewritten as

$$p = \frac{Q(s_n^2 + 1)}{s_n} \tag{7.73}$$

Substituting the transformation from Eq. (7.73) to Eq. (7.70), we get

$$H(s_n) = \frac{(A_o/Q)s_n}{s_n^2 + (1/Q)s_n + 1} \tag{7.74}$$

This is identical with Eq. (7.48) of band pass filter. The quality factor Q is an important parameter. If Q is very high, i.e $Q >> 1$, the filter is called narrow band filter (i.e., $\omega_o >> (\omega_h - \omega_\ell)$) and the response is symmetric about the central frequency ω_o.

Low-pass to Band-reject Transformation

The transformation is given by

$$p = \frac{(\omega_h - \omega_\ell)s}{s^2 + \omega_o^2} = \frac{s_n}{Q(s_n^2 + 1)} \tag{7.75}$$

where $s_n = s/\omega_o$

The band-reject transfer function corresponding to first order low-pass of Eq. (7.70) and is given by

$$H(S_n) = \frac{A_o(s_n^2 + 1)}{s_n^2 + (1/Q)s_n + 1} \tag{7 76}$$

Note at $s_n = j1$, $|H(j1)| = 0$. Such filters are called 'notch filter' with normalized null frequency as $\omega_o = 1$.

7.4 STATE VARIABLE FILTER

The state variable configuration uses two op-amp integrators and one op-amp adder to provide simultaneous second order low-pass, band-pass and high-pass filter responses. The circuit can be viewed as analog computer simulation of biquadratic transfer function. Although, in general, all component values are different, imposing equal value simplifies algebra without diminishing versatality.

A simple state variable configuration has been shown in Fig. 7.17 (a). It uses two op-amp integrators and one op-amp summer. The outputs v_{HP}, v_{BP}, v_{LP} of high-pass, band-pass and low-pass filters are obtained at the output of op-amp A_1, A_2 and A_3 respectively. For simplification, it is assumed that V is the Laplace transform of the corresponding v in time domain.

The op-amp A_2 works as an inverting integrator, so the Laplace transformed output V_{BP} is given by

$$V_{BP} = -\frac{1}{RCs} V_{HP} \tag{7.77}$$

If $R = 1$ MΩ and $C = 1$ μF, so that $RC = 1$, we get,

$$V_{BP} = -\frac{1}{s} V_{HP} \tag{7.78}$$

Also for the inverting integrator A_3, we may write

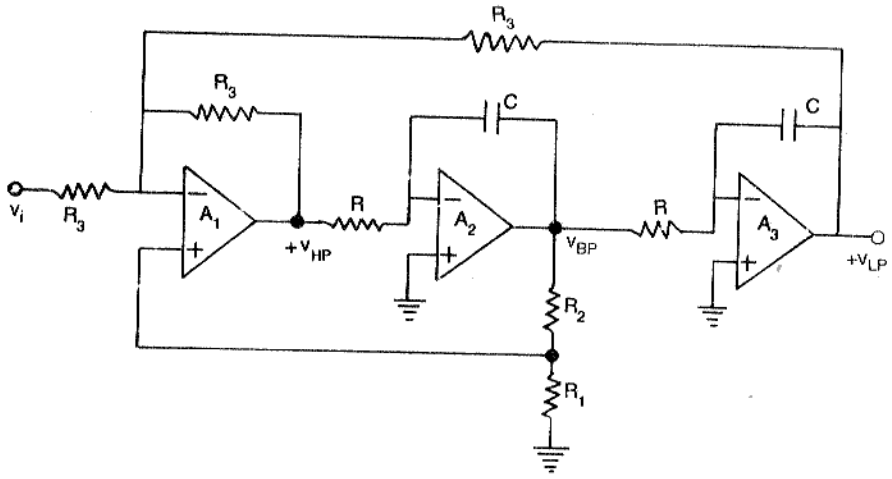


Fig. 7.17 (a) State variable filter

$$V_{LP} = \frac{1}{s} V_{BP}$$

$$= \frac{1}{s^2} V_{HP} \qquad (7.79)$$

Op-amp A_1 is a three input summer. The output V_{HP} can be written using superposition theorem. That is,

$$V_{HP} = -\left(\frac{R_3}{R_3}\right)V_i - \left(\frac{R_3}{R_3}\right)V_{LP} + \left(1 + \frac{R_3}{R_3 \| R_3}\right)\left(\frac{R_1}{R_1 + R_2}\right)V_{BP}$$

$$= -V_i - V_{LP} + 3\left(\frac{R_1}{R_1 + R_2}\right)V_{BP}$$

Put $$\alpha = 3\left(\frac{R_1}{R_1 + R_2}\right)$$

Then $$V_{HP} = -V_i - V_{LP} + \alpha V_{BP} \qquad (7.80)$$

Eliminating V_{BP} and V_{LP} using Eqs. (7.78) and (7.79), we get

$$V_{HP} = -V_i - \frac{V_{HP}}{s^2} - \frac{\alpha}{s} V_{HP}$$

$$V_{HP}\left(1 + \frac{\alpha}{s} + \frac{1}{s^2}\right) = -V_i$$

So, the high pass transfer function H_{HP} is

$$H_{HP} = \frac{V_{HP}}{V_i} = \frac{-s^2}{s^2 + \alpha s + 1} \qquad (7.81)$$

The damping factor α can be set by R_1 and R_2 for Bessel, Butterworth or Chebyshev response.

Compare Eq. (7.81) to the standard high-pass transfer function of Eq. (7.27) as

$$\frac{A_o s^2}{s^2 + \alpha\omega_1 s + \omega_\ell^2} \qquad (7.82)$$

So for the high-pass filter of the state variable filter,

$$A_o = -1 \text{ and } \omega_\ell = 1$$

The low-pass transfer function is obtained by eliminating V_{HP} and V_{BP} from Eq. (7.80) as

$$H_{LP} = \frac{V_{LP}}{V_i} = \frac{-1}{s^2 + \alpha s + 1} \qquad (7.83)$$

As in High-pass filter, the low-pass filter has

$$A_o = -1, \ \omega_h = 1$$

and $$\alpha = 3\left(\frac{R_1}{R_1 + R_2}\right)$$

Finally the band-pass impulse response is obtained from Eq. (7.80) by eliminating V_{HP} and V_{LP} as

$$H_{BP} = \frac{V_{BP}}{V_i} = \frac{s}{s^2 + \alpha s + 1} \qquad (7.84)$$

The standard band-pass transfer function as given in Eq. (7.48) is

$$\frac{A_o \alpha \omega_o s}{s^2 + \alpha \omega_o s + \omega_o^2} \qquad (7.85)$$

Comparing Eq. (7.84) and Eq. (7.85), we get

$$A_o \alpha \omega_o = 1$$

$$\omega_o = \frac{1}{RC} = 1, \ (RC \text{ has been assumed to be } 1) \qquad (7.87)$$

therefore, $$A_o = \frac{1}{\alpha} = \frac{R_1 + R_2}{3R_1} \qquad (7.88)$$

From the analysis, we found that the band-pass response can be generated by integrating the high-pass response and that the low-pass is generated by integrating the band-pass.

The circuit of Fig. 7.17(a) can be modified to that of Fig. 7.17(b) where a fourth op-amp has been used to get a notch filter response. The op-amp A_4 provides the notch filter response by combining the low-pass and high-pass output. The notch filter output V_N is written as

$$V_N = -\left(\frac{R_4}{R_4}\right)V_{HP} - \left(\frac{R_4}{R_4}\right)V_{LP}$$

$$= -V_{HP} - V_{LP} \qquad (7.89)$$

Putting the values of V_{HP} and V_{LP}, the transfer function of notch filter is obtained as

$$H_N = \frac{V_N}{V_i} = \frac{s^2+1}{s^2+\alpha s+1} \qquad (7.90)$$

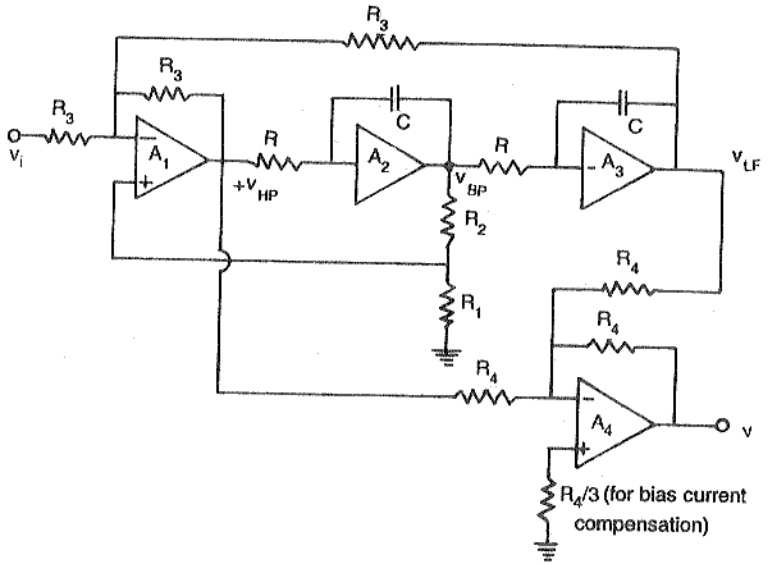


Fig. 7.17 (b) Four op-amp state variable filter with notch response

Thus it is possible to obtain LP, BP, HP and notch filter outputs from a state variable filter and therefore these are also known as universal filters. Quad op-amps such as LF347, TL074 and TLC274, FET input device are especially suited for these applications. With the advancement of IC technology, universal filters are available in single IC chip form. Datel's FLT-U2 and AF100 of National Semiconductor are the typical examples of IC universal filters.

State Variable Formulation

It may be noted that this filter is called state variable filter because the analog simulation can be made after the state variable formulation of the proper transfer function.

The band-pass filter transfer function of Eq. (7.48) can be rewritten for $A_0 = -1$, $\omega_0 = 1$, $\alpha = 1$ and assuming a dummy variable $X_1 = \mathcal{L}x_1(t)$, as

$$\frac{V_{BP}}{X_1}\cdot\frac{X_1}{V_i} = s\frac{1}{s^2+s+1} \qquad (7.91)$$

Let $$\frac{X_1}{V_i} = \frac{1}{s^2+s+1} \qquad (7.92)$$

which can written in time domain as

$$\ddot{x}_1 + \dot{x}_1 + x_1 = v_i$$

Let $$\dot{x}_1 = x_2$$

then $$\dot{x}_2 = -x_1 - x_2 + v_i$$

These can be written in matrix form as

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}0 & 1\\ -1 & -1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}0\\ 1\end{bmatrix}v_i \qquad (7.93)$$

and $$\frac{V_{BP}}{X_1} = s \qquad (7.94)$$

leads to the output in time domain as $v_{BP} = \dot{x}_1 = x_2$

or, $$v_{BP} = \begin{bmatrix}0 & 1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} \qquad (7.95)$$

Similarly the high-pass transfer function H_{HP} of Eq. (7.81) with $\alpha = 1$ can be rewritten assuming another dummy variable $Y = \mathcal{L}y(t)$ as

$$H_{HP} = \frac{V_{HP}}{V_i} = -1 + \frac{s+1}{s^2+s+1} = -1 + \frac{Y}{V_i} \qquad (7.96)$$

where $$\frac{Y}{V_i} = \frac{Y}{X_1}\cdot\frac{X_1}{V_i} = (s+1)\cdot\frac{1}{s^2+s+1} \qquad (7.97)$$

Let $$\frac{X_1}{V_i} = \frac{1}{s^2+s+1} \qquad (7.98)$$

It leads to

$$\begin{bmatrix}\dot{x}_1\\ \dot{x}_2\end{bmatrix} = \begin{bmatrix}0 & 1\\ -1 & -1\end{bmatrix}\begin{bmatrix}x_1\\ x_2\end{bmatrix} + \begin{bmatrix}0\\ 1\end{bmatrix}v_i \qquad (7.99)$$

and $$\frac{Y}{X_1} = (s+1) \qquad (7.100)$$

leads to in time domain $y = \dot{x}_1 + x_1 = x_2 + x_1$